Triple Adjustable Output TFT-LCD DC-DC Converters

DESCRIPTION

The EUP2618 triple-output DC-DC converter provides the regulated voltages required by active-matrix, thin-film transistor (TFT) liquid-crystal displays (LCDs). One high-power DC-DC converter and two low-power charge pumps convert the 3.3V to 5V input supply voltage into three independent output voltages.

The primary 1.2MHz DC-DC converter generates a boosted output voltage (V_{MAIN}) up to 18V using ultra-small inductors and ceramic capacitors. The low-power control circuitry and the low on-resistance (0.2Ω) of the integrated power MOSFET allows efficiency up to 92%.

The dual charge pumps independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages to regulate output voltages up to 40V and down to -40V.

For EUP2618, the supply sequence is V_{MAIN} first, V_{NEG} next, and finally V_{POS}. The EUP2618 soft-starts each supply as soon as the previous supply finishes.

The EUP2618 are available in the ultra-thin TSSOP-16 package.

FEATURES

- 1.2MHz Current-Mode PWM Boost Regulator
  Up to 18V Main High-Power Output
  2.1A, 0.2Ω Power MOSFET
  92% High Efficiency
- Dual Adjustable Charge-Pump Outputs
  Up to 40V Positive Output
  Down to -40V Negative Output
- Internal Power-up Sequencing
- 2.5V to 5.5V Input Range
- 0.1μA Shutdown Current
- 0.7mA Quiescent Current
- Internal Soft-Start
- Power-Ready Output
- Ultra-Small External Components
- Thin TSSOP-16 Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- TFT Active-Matrix LCD Displays
- Passive-Matrix LCD Displays
- PDAs
- Digital Still Cameras

Typical Application Circuit

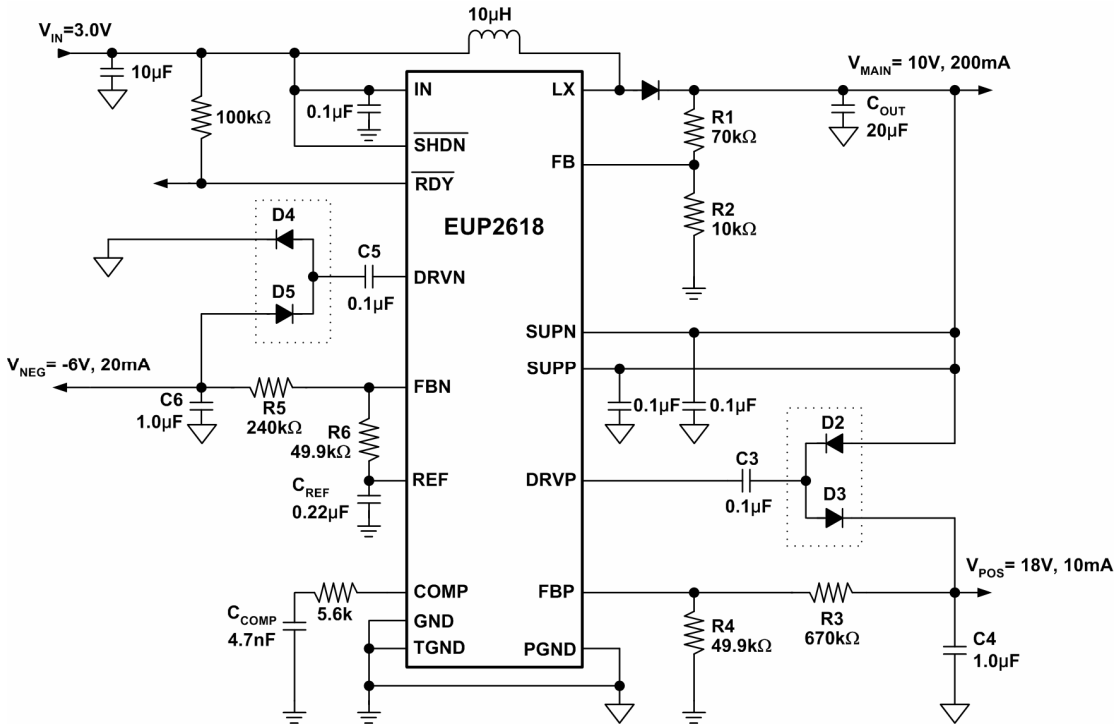


Figure 1.

Block Diagram

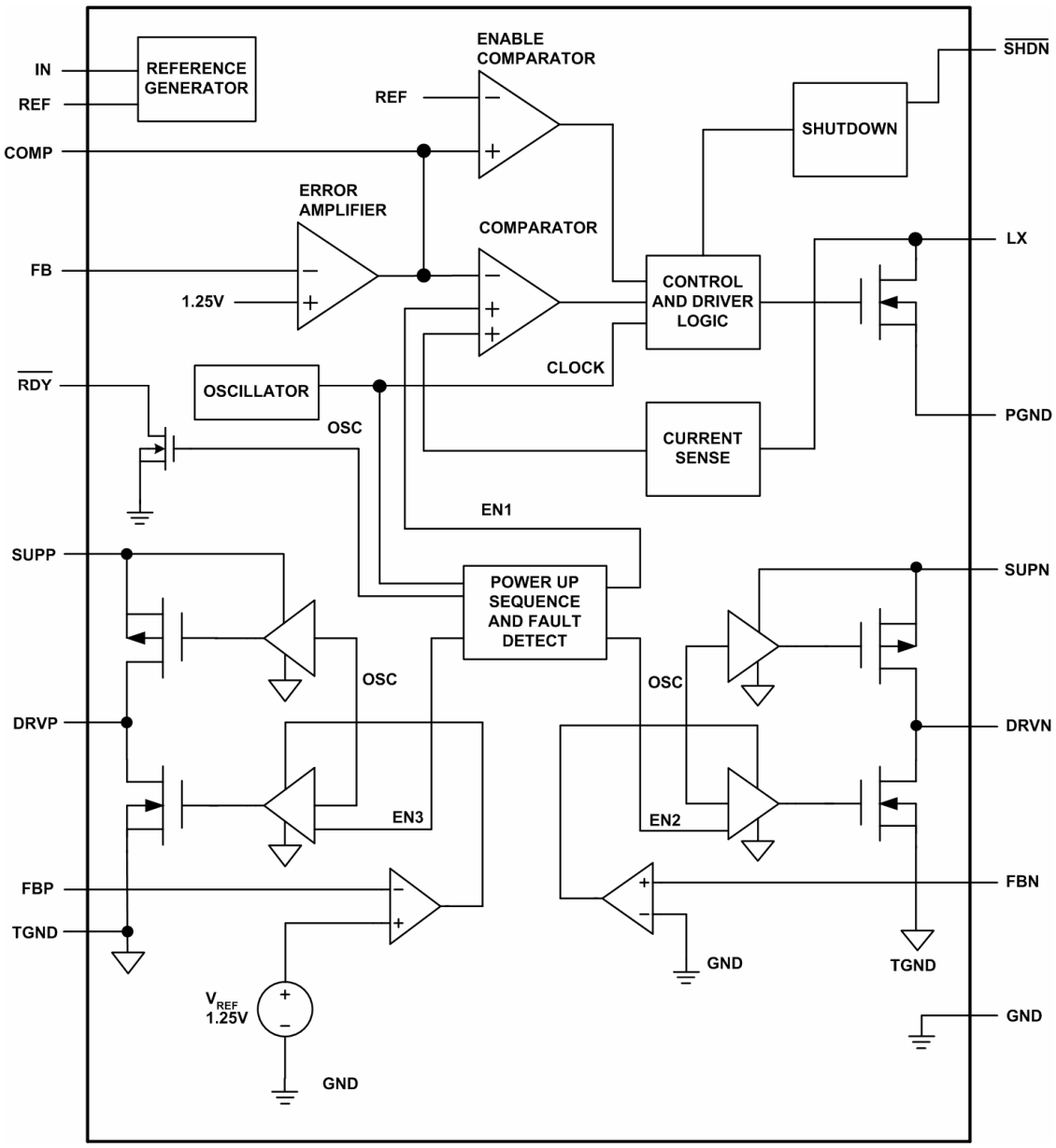
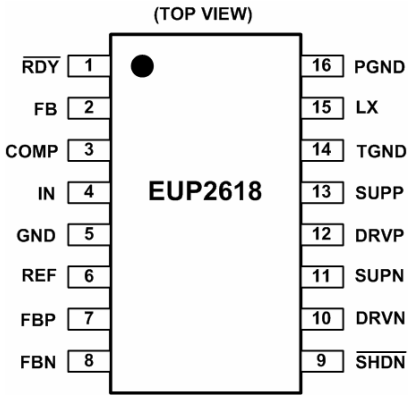


Figure 2.

Pin Configurations

Package Type	Pin Configurations
TSSOP-16	

Pin Description

PIN	NAME	DESCRIPTION
1	$\overline{\text{RDY}}$	Active-Low, Open-Drain Output. Indicates all outputs are ready. The on-resistance is 125Ω (typ).
2	FB	Main Boost Regulator Feedback Input. Regulates to 1.25V nominal. Connect feedback resistive divider to analog ground (GND).
3	COMP	Main Boost Compensation Network Connection.
4	IN	Supply Input. 2.5V to 5.5V input range. Bypass with a 0.1µF capacitor between IN and GND, as close to the pins as possible.
5	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
6	REF	Internal Reference Bypass Terminal. Connect a 0.22µF capacitor from this terminal to analog ground (GND). External load capability to 100µA.
7	FBP	Positive Charge-Pump Regulator Feedback Input. Regulates to 1.25V nominal. Connect feedback resistive divider to analog ground (GND).
8	FBN	Negative Charge-Pump Regulator Feedback Input. Regulates to 0V nominal.
9	$\overline{\text{SHDN}}$	Active-Low Logic-Level Shutdown Input. Connect $\overline{\text{SHDN}}$ to IN for normal operation.
10	DRVN	Negative Charge-Pump Driver Output. Output high level is V_{SUPN}, and low level is TGND.
11	SUPN	Negative Charge-Pump Driver Supply Voltage. Bypass to TGND with a 0.1µF capacitor.
12	DRVP	Positive Charge-Pump Driver Output. Output high level is V_{SUPP}, and low level is TGND.
13	SUPP	Positive Charge-Pump Driver Supply Voltage. Bypass to TGND with a 0.1µF capacitor.
14	TGND	Power Ground of Charge-Pumps.
15	LX	Main Boost Regulator Power MOSFET n-Channel Drain. Connect output diode and output capacitor as close to PGND as possible.
16	PGND	Power Ground of Main Boost.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUP2618QIR1	TSSOP-16	xxxxx EUP2618	-40 °C to 85°C

EUP2618 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
Q: TSSOP

Absolute Maximum Ratings

- IN to GND ---------- -0.3V to 6V
- DRVN to GND ---------- -0.3V to (V_{SUPN} +0.3V)
- DRVP to GND ---------- -0.3V to (V_{SUPP} +0.3V)
- PGND ,TGND to GND ---------- ±0.3V
- $\overline{RDY}$,SUPP,SUPN to GND ---------- -0.3V to 14V
- LX to GND ---------- -0.3V to 19V
- COMP, $\overline{SHDN}$,REF, FB ,FBN, FBP to GND ---------- -0.3V to (V_{IN} +0.3V)
- Operating Temperature ---------- -40°C to 85°C
- Junction Temperature ---------- 150°C
- Storage Temperature ---------- -65°C to150°C
- Lead Temp (Soldering, 10sec) --- ---------- 260°C

Electrical Characteristics

(Specfications in standard type face are for T_A =25℃ and those with **boldface type** apply over the full **Operating Temperature Range (T_A=-40℃ to 85℃).** V_{IN}=3.3V, V_{SUPP}=V_{SUPN}=10V ,GND=PGND=TGND=0, unless otherwise noted.)

Parameter	Conditions	EUP2618			Unit
		Min.	Typ.	Max.	
Operating Power					
Input Supply Voltage Range		**2.5**		**5.5**	V
VIN Under Voltage Lockout	Falling	**1.9**	2.13	**2.35**	V
	Rising	**2**	2.23	**2.45**	V
Quiescent Current	V_{FB}=V_{FBP}=1.4V, V_{FBN}=0V , not switching		0.7	**1**	mA
	V_{FB}=1.1V, V_{FBP}=1.4V, V_{FBN}=0V switching		2.1	**4**	mA
Shutdown Current	$V_{\overline{SHDN}}$ =GND		0.1	**10**	uA
Thermal Shutdown	15℃ Hysteresis		165		℃
Reference					
Reference Voltage	IV_{REF}=100uA	**1.22**	1.25	**1.28**	V
Line Regulation	IV_{REF}=100uA, V_{IN}=2.5~5V		2	**5**	mV
Load Regulation	IV_{REF}=0~100uA		1	**5**	mV
EA (Error Amplifier)					
Feedback Voltage		**1.22**	1.25	**1.28**	V
Input Bias Current	V_{FB}=1.25V		100	**200**	nA
Feedback Voltage Line Regulation	2.5V<V_{DD}<5.5V		0.07	**0.15**	%/V
Error Amp Transconductance	ΔI=2uA	**30**	60	**90**	umho
Error Amp Voltage Gain	FB to COMP		853		V/V
Oscillator					
Operating Frequency		**1000**	1200	**1500**	kHz
Maximum Duty		**85**	96		%
N-Channel Switch					
Switch Current Limit	65% Duty Cycle	**1.5**	2.1	**2.8**	A

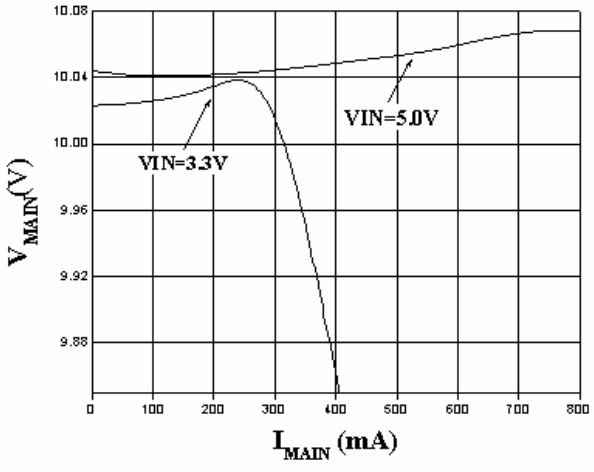
Electrical Characteristics (continued)

(Specfications in standard type face are for T_A =25℃ and those with **boldface type** apply over the full **Operating Temperature Range (T_A=-40℃ to 85℃)**. V_{IN}=3.3V, V_{SUPP}=V_{SUPN}=10V ,GND=PGND=TGND=0, unless otherwise noted.)

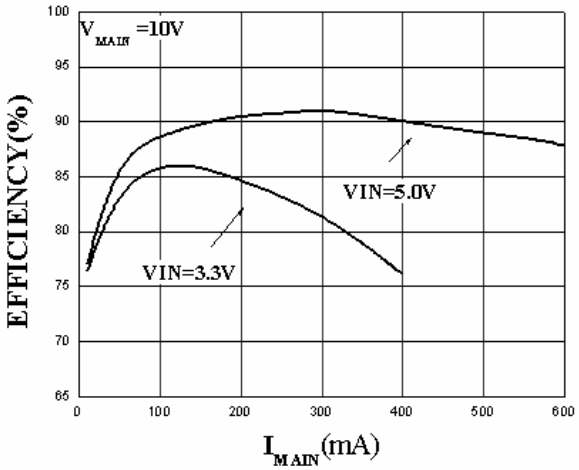
Parameter	Conditions		EUP2618			Unit
			Min.	Typ.	Max.	
Switch R_{DSON}	I_{LX}=200mA			0.2	**0.4**	Ω
Switch Leakage Current	V_{LX}=18V			0.01	**20**	uA
Control Inputs Characteristics (SHDN)						
SHDN Low Threshold					**0.8**	V
SHDN High Threshold			**1.8**			V
SHDN Pin Pull Up Current	SHDN=GND			0.001	**1**	uA
Soft Start & Fault Detect Time						
Channel 1 Soft Start Time				14		ms
Channel 2 Soft Start Time				3.5		ms
Channel 3 Soft Start Time				3.5		ms
Channel 1 Fault Protect Trigger Time				55		ms
Channel 2 Fault Protect Trigger Time				14		ms
Channel 3 Fault Protect Trigger Time				14		ms
FB Fault Protection Voltage			**1**	1.1	**1.2**	V
FBN Fault Protection Voltage			**0.08**	0.13	**0.18**	V
FBP Fault Protection Voltage			**1**	1.1	**1.2**	V
Charge Pump Regulator Characteristics						
V_{SUPP} Input Supply Range			**5**		**13.5**	V
V_{SUPN} Input Supply Range			**5**		**13.5**	V
FBN Threshold Voltage			**-50**		**50**	mV
FBP Threshold Voltage			**1.208**	1.258	**1.308**	V
FBN Input Bias Current	V_{FBN}=-0.05V		**-50**		**50**	nA
FBP Input Bias Current	V_{FBP}=-1.5V		**-50**		**50**	nA
Charge Pump Frequency				f_{OSC}/2		kHz
OUT2 Switch R-on	PMOS	I_{OUT2}=10mA		3	**20**	Ω
	NMOS	I_{OUT2}=-10mA		3	**20**	Ω
OUT3 Switch R-on	PMOS	I_{OUT3}=10mA		3	**20**	Ω
	NMOS	I_{OUT3}=-10mA		3	**20**	Ω
Continuous Output Current	Test Condition T_A=25℃				**30**	mA

Typical Characteristics

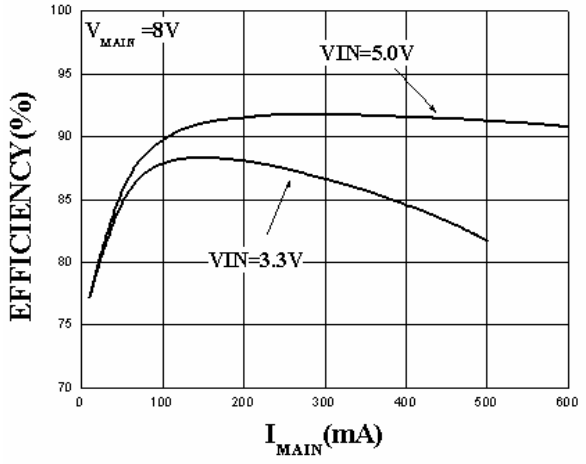
MAIN OUTPUT VOLTAGE
VS. LOAD CURRENT



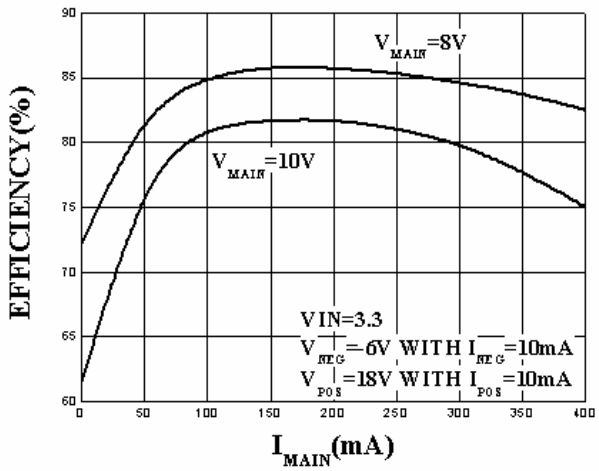
MAIN STEP-UP CONVERTER
EFFICIENCY VS. LOAD CURRENT
(BOOST ONLY)



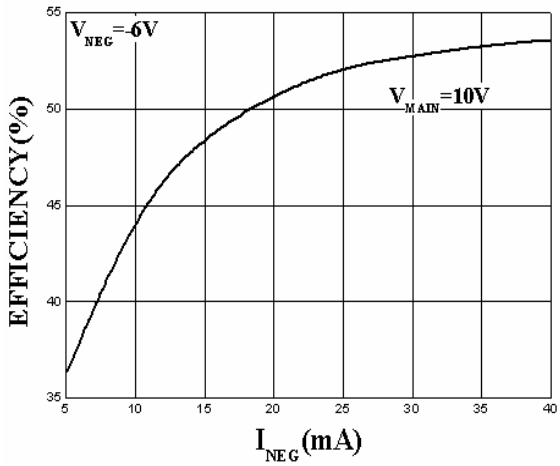
MAIN STEP-UP CONVERTER
EFFICIENCY VS. LOAD CURRENT
(BOOST ONLY)



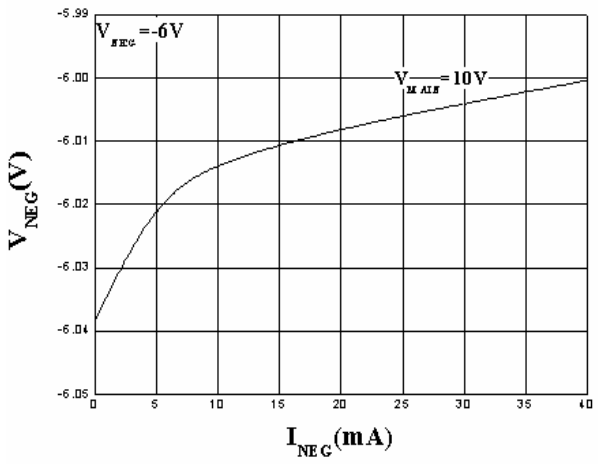
EFFICIENCY VS.LOAD CURRENT
(BOOST CONVERTER AND CHARGE PUMPS)



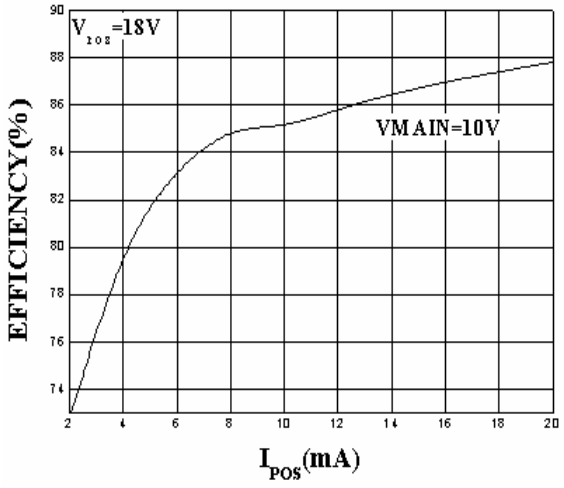
VOLTAGE VS. LOAD CURRENT



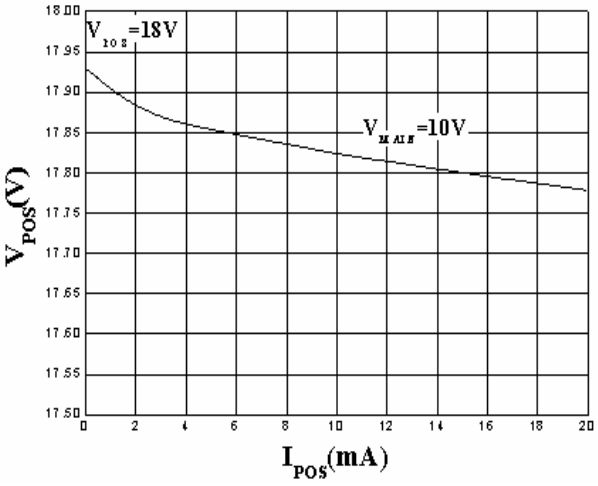
EFFICIENCY VS. LOAD CURRENT



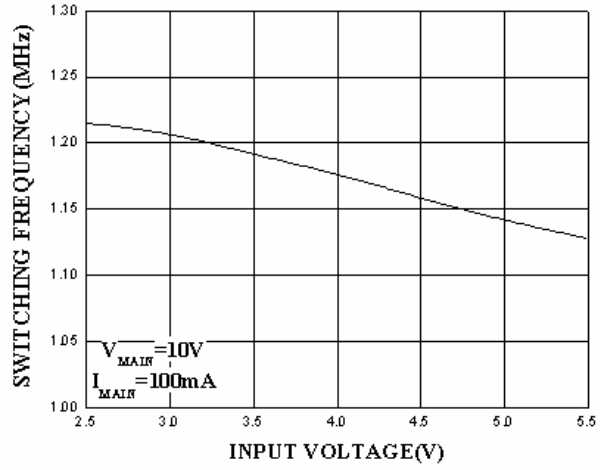
VOLTAGE VS. LOAD CURRENT



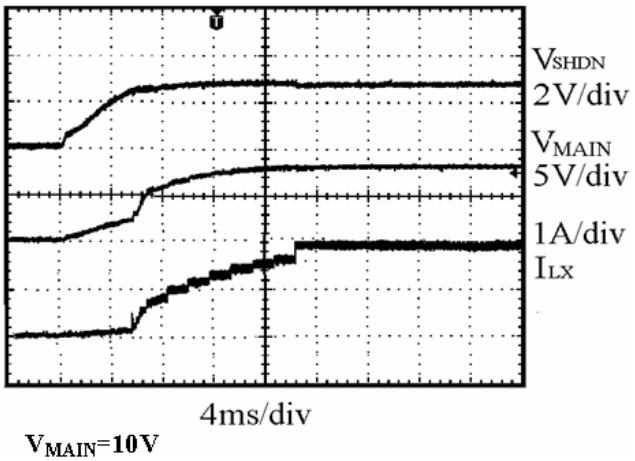
EFFICIENCY VS. CURRENT



SWITCHING FREQUENCY VS. INPUT VOLTAGE

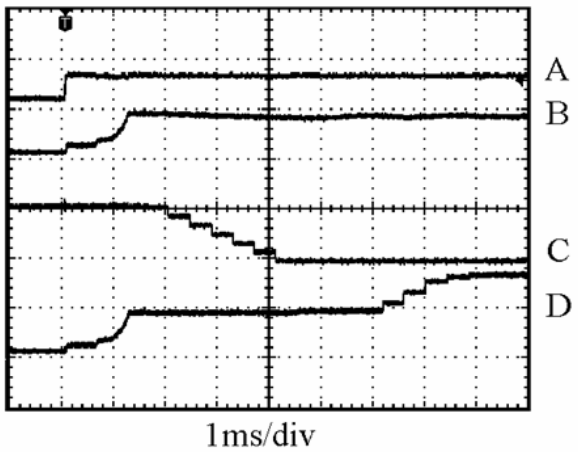


MAIN BOOST STARTUP WAVEFORM WITH LOAD



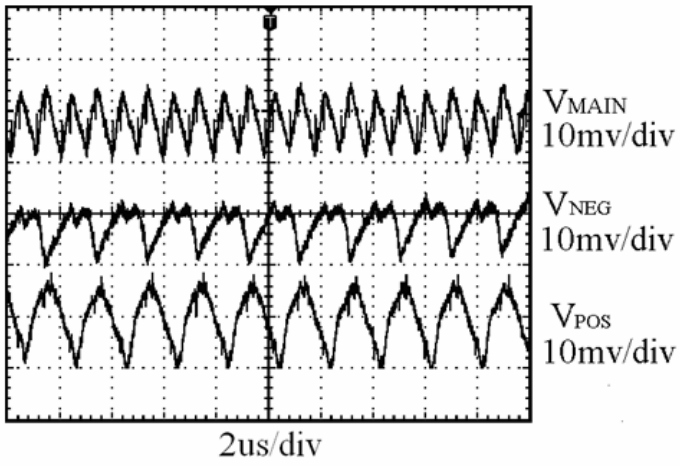
V_{MAIN}=10V

POWER-UP SEQUENCING



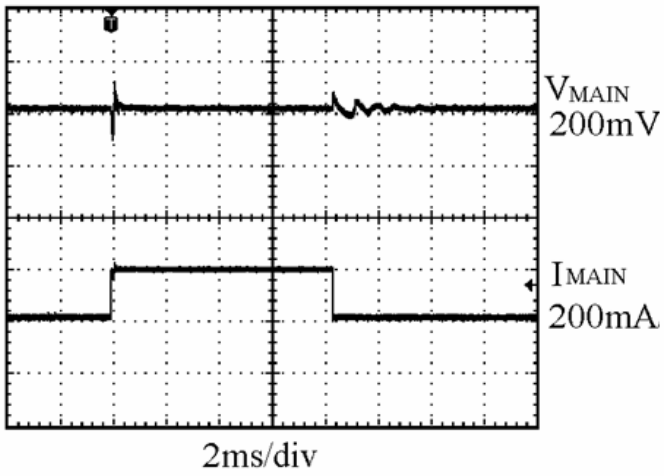
A: V_{SHDN} 5V/div B: V_{MAIN} 10V/div
C: V_{NEG} 5V/div D: V_{POS} 10V/div

RIPPLE WAVEFORMS



V_{MAIN}=10V I_{MAIN}=200mA
V_{NEG}=-6V I_{NEG}=10mA
V_{POS}=18V I_{POS}=10mA

LOAD TRANSIENT RESPONSE



VIN=3.3, V_{MAIN}=10V I_{MAIN}(20mAto200mA)

Detailed Description

Main Boost Converter Operations

In steady state operating and continuous conduction mode where the inductor current is continuous, the boost converter operates in two cycles. During the first cycle, the internal power FET turns on and the Schottky diode is reverse biased and cuts off the current flow to the output. The output current is supplied from the output capacitor. The voltage across the inductor is VIN and the inductor current ramps up in a rate of VIN/L, L is the inductance. The inductance is magnetized and energy is stored in the inductor. The change in inductor current is:

$$\Delta I_L = \Delta T2 \times \frac{V_{IN} - V_{MAIN}}{L}$$

$$\Delta T2 = \frac{1 - D}{F_{LX}}$$

For stable operation, the same amount of energy stored in the inductor must be taken out. The change in inductor current during the two cycles must be the same.

$\Delta I1+\Delta I2=0$

$$\frac{D}{F_{LX}} \times \frac{V_{IN}}{L} + \frac{1-D}{F_{LX}} \times \frac{V_{IN} - V_{MAIN}}{L} = 0$$

$$\frac{V_{MAIN}}{V_{IN}} = \frac{1}{1-D}$$

Output Voltage

An external feedback resistor divider is required to divide the output voltage down to the nominal 1.25V reference voltage. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. Selecting R_2 in the range of 10kΩ to 50 kΩ. The boost converter output voltage s determined by the relationship:

$$V_{MAIN} = V_{FB} \times \left[1 + \frac{R_1}{R_2}\right]$$

The nominal VFB voltage is 1.25V

Dual Charge-Pump Regulator

The EUP2618 contain two individual low-power charge pumps. One charge pump inverts the supply voltage (SUPN) and provides a regulated negative output voltage. The second charge pump doubles the supply voltage (SUPP) and provides a regulated positive output voltage. The EUP2618 contain internal p-channel and n-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant 600kHz (0.5 x f_{OSC}).

Negative Charge Pump

During the first half-cycle, the p-channel MOSFET turns on and the flying capacitor C5 charges to V_{SUPN} minus a diode drop. During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting C5. This connects C5 in parallel with the reservoir capacitor C6. If the voltage across C6 minus a diode drop is lower than the voltage across C5, charge flows from C5 to C6 until the diode (D5) turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance.

Positive Charge Pump

During the first half-cycle, the n-channel MOSFET turns on and charges the flying capacitor C3. This initial charge is controlled by the variable n-channel on resistance. During the second half-cycle, the n-channel MOSFET turns off and the p-channel MOSFET turns on, level shifting C3 by V_{SUPP} volts. This connects C3 in parallel with the reservoir capacitor C4. If the voltage across C4 plus a diode drop (V_{POS} + V_{DIODE}) is smaller than the level-shifted flying capacitor voltage (V_{C3} + V_{SUPP}), charge flows from C3 to C4 until the diode (D3) turns off.

Shutdown

A logic-low level on $\overline{SHDN}$ disables all three EUP2618 converters and the reference. When shut down, supply current drops to 0.1μA to maximize battery life and the reference is pulled to ground. The output capacitance and load current determine the rate at which each output voltage will decay. A logic-level high on $\overline{SHDN}$ power activates the EUP2618 (see the *Power-Up Sequencing* section). Do not leave $\overline{SHDN}$ floating. If unused, connect $\overline{SHDN}$ to GND.

Power-Up Sequencing

Upon power-up or exiting shutdown, the EUP2618 start their respective power-up sequences.

The reference powers up first, then the main DC-DC step-up converter powers up with softstart enabled. Once the main step-up converter reaches regulation, the negative charge pump turns on. The positive charge pump starts up. Finally, when the positive output voltage reaches 88% of its nominal value (V_{FBP} > 1.1V), the active-low ready signal ($\overline{RDY}$) goes low (see the *Power Ready* section).

Power Ready
Power ready is an open-drain output. When the power up sequence is properly completed, the MOSFET turns on and pulls $\overline{RDY}$ low with a typical 125Ω on-resistance. If a fault is detected, the internal open-drain MOSFET appears as a high impedance. Connect a 100kΩ pullup resistor between RDY and IN for a logic level output.

Fault Detection
Once $\overline{RDY}$ is low and if any output falls below its fault-detection threshold, $\overline{RDY}$ goes high impedance.

For the main boost converter, the fault threshold is 88% of its nominal value (V_{FB} < 1.1V). For the negative charge pump, the fault threshold is approximately 90% of its nominal value (V_{FBN} < 130mV). For the positive charge pump, the fault threshold is 88% of its nominal value (V_{FBP} < 1.1V).

Once an output faults, all outputs later in the power sequence shut down until the faulted output rises above its power-up threshold.

Inductor Selection
The inductor selection determines the output ripple voltage, transient response, output current capability, and efficiency. Its selection depends on the input voltage, output voltage, switching frequency, and maximum output current. For most applications, a 4.7µH to 10uH inductor is recommended for 1.2MHz application. The inductor maximum DC current specification must be greater than the peak inductor current required by the regulator. The peak inductor current can be calculated:

$$I_{L(PEAK)} = \frac{I_{MAIN} \times V_{MAIN}}{V_{IN}} + 1/2 \times \frac{V_{IN} \times (V_{MAIN} - V_{IN})}{L \times V_{MAIN} \times FREQ}$$

Output Capacitor
Low ESR capacitors should be used to minimized the output voltage ripple. Multilayer ceramic capacitors (X5R and X7R) are preferred for the output capacitors because of their lower ESR and small packages. Tantalum capacitors with higher ESR can also be used. The output ripple can be calculated as:

$$\Delta V_O = \frac{I_{MAIN} \times D}{F_{LX} \times C_O} + I_{MAIN} \times ESR$$

Choose an output capacitor to satisfy the output ripple and load transient requirement. A 10µF to 22µF ceramic capacitor is suitable for most application.
For noise sensitive application, a 0.1µF placed in parallel with the larger output capacitor is recommended to reduce the switching noise coupled from the LX switching node.

Input Capacitor
The value of the input capacitor depends the input and output voltages, the maximum output current, the inductor value and the noise allowed to put back on the input line. For most applications, a minimum 10µF is required. For applications that run close to the maximum output current limit, input capacitor in the range of 22µF to 47µF is recommended. The EUP2618 is powered from the VIN. High frequency 0.1µF by-pass cap is recommended to be close to the VIN pin to reduce supply line noise and ensure stable operation.

Rectifier Diode
Use a Schottky diode with an average current rating equal to or greater than the peak inductor current, and a voltage rating at least 1.5 times the main output voltage (V_{MAIN}).

Charge Pump
Efficiency Considerations
The efficiency characteristics of the EUP2618 regulated charge pumps are similar to a linear regulator. They are dominated by quiescent current at low output currents and by the input voltage at higher output currents (see the Typical Operating Characteristics). So the maximum efficiency can be approximated by:

$$\text{Efficiency} \cong V_{NEG}/[V_{SUPN} \times N];$$

for the negative charge pump

$$\text{Efficiency} \cong V_{POS}/[V_{SUPP} \times (N+1)];$$

for the positive charge pump

where N is the number of charge-pump stages.

Output Voltage Selection
Adjust the positive output voltage by connecting a voltage-divider from the output (V_{POS}) to FBP to GND (see the Typical Operating Circuit). Adjust the negative output voltage by connecting a voltage-divider from the output (V_{NEG}) to FBN to REF. Select R4 and R6 in the 50kΩ to 100kΩ range. Higher resistor values improve efficiency at low output current but increase output-voltage error due to the feedback input bias current. Calculate the remaining resistors with the following equations:

$$R3 = R4[(V_{POS}/V_{REF}) - 1]$$

$$R5 = R6(V_{POS}/V_{REF})$$

where V_{REF} = 1.25V. V_{POS} can range from V_{SUPP} to 40V, and V_{NEG} can range from 0 to -40V.

Flying Capacitor
Increasing the flying capacitor's value reduces the output current capability. Above a certain point, increasing the capacitance has a negligible effect because the output current capability becomes dominated by the internal switch resistance and the diode impedance. Start with 0.1µF ceramic capacitors. Smaller values can be used for low-current applications.

Charge-Pump Output Capacitor
Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq [I_{OUT} / (600kHz \times V_{RIPPLE})]$$

Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect directly to TGND.

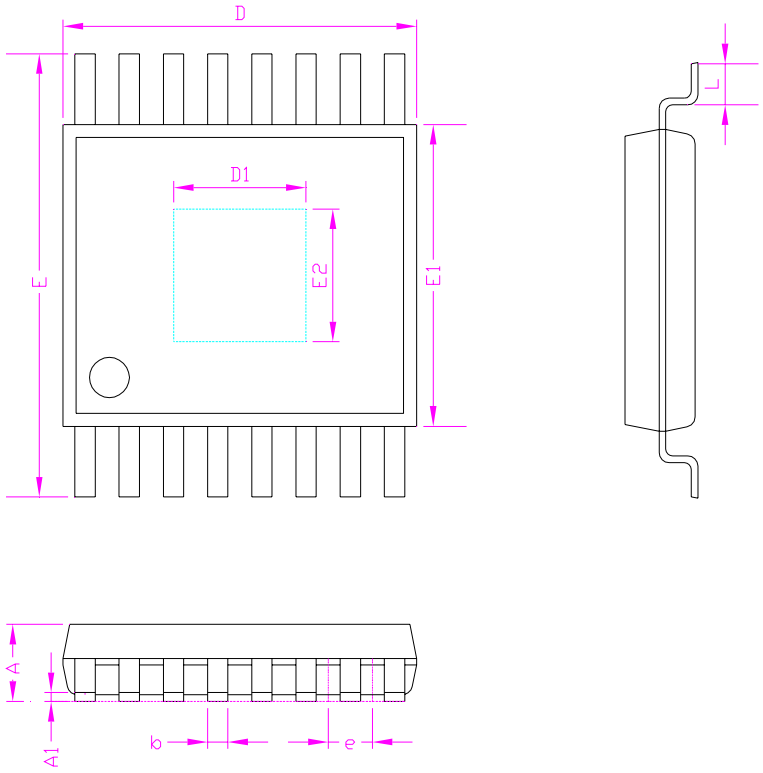
Charge-Pump Input Capacitor
Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect directly to GND.

Rectifier Diode
Use Schottky diodes with a current rating equal to or greater than 4 times the average output current, and a voltage rating at least 1.5 times V_{SUPP} for the positive charge pump and V_{SUPN} for the negative charge pump.

PC Board Layout and Grounding
Careful printed circuit layout is extremely important to minimize ground bounce and noise. First, place the main boost-converter output diode and output capacitor less than 0.2in (5mm) from the LX and PGND pins with wide traces and no vias. Then place 0.1µF ceramic bypass capacitors near the charge-pump input pins (SUPP and SUPN) to the PGND pin. Keep the charge pump circuitry as close to the IC as possible, using wide traces and avoiding vias when possible. Locate all feedback resistive dividers as close to their respective feedback pins as possible. The PC board should feature separate GND and PGND areas connected at only one point under the IC. To maximize output power and efficiency and to minimize output-power ripple voltage, use extra wide power ground traces and solder the IC's power ground pin directly to it. Avoid having sensitive traces near the switching nodes and high-current lines.

Packaging Information

TSSOP-16



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40		0.173	
D	5.00		0.197	
E	6.20	6.60	0.244	0.260
e	0.65		0.026	
L	0.45	0.75	0.018	0.030