FAIRCHILD SEMICONDUCTOR®

January 2010

FAN6791 / FAN6793
Highly Integrated, Dual-PWM Combination Controller

Features

- High-Voltage Startup
- Low Operating Current
- Interleaved Stand-by PWM / Forward PWM Switching
- Green Mode Stand-by PWM / Forward PWM
- Linearly Decreasing Stand-by PWM Frequency to 20kHz
- Remote On / Off
- AC Brownout Protection
- Forward PWM with Soft-Start
- Frequency Hopping to Reduce EMI Emissions
- Cycle-by-Cycle Current Limiting for Stand-by PWM / Forward PWM
- Leading-Edge Blanking for Stand-by PWM / Forward PWM
- Synchronized Slope Compensation for Stand-by PWM / Forward PWM
- GATE Output Maximum Voltage Clamp
- V_{DD} Over-Voltage Protection (OVP)
- V_{DD} Under-Voltage Lockout (UVLO)
- Internal Open-Loop Protection for Stand-by PWM / Forward PWM
- Constant Power Limit for Stand-by PWM / Forward PWM

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- PC-ATX Power Supplies

Description

The highly integrated FAN6791/3 dual PWM combination controller provides several features to enhance the performance of converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 20kHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, FAN6791/3 is manufactured using the CMOS process, which allows an operating current of only 6mA.

FAN6791/3 integrates a frequency-jittering function internally to reduce EMI emissions of a power supply with minimum line filters. The built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit.

FAN6791/3 provides many protection functions, including brownout protection, cycle-by-cycle current limiting, and an internal open-loop protection circuit to ensure safety should an open-loop or output short-circuit failure occur. PWM output is disabled until V_{DD} drops below the UVLO lower limit when the controller restarts. As long as V_{DD} exceeds ~24.5V, the internal OVP circuit is triggered.

Ordering Information

Part Number	OPWM Maximum Duty	Operating Temperature Range	Eco Status	Package	Packing Method
FAN6791NY	48%	-40°C to +105°C	Green	16-Pin Dual In-Line Package (DIP)	Tube
FAN6793NY	65%	-40°C to +105°C	Green	16-Pin Dual In-Line Package (DIP))	Tube
FAN6791MY	48%	-40°C to +105°C	Green	16-Pin Small Outline Integrated Circuit Package (SOIC)	Tape & Reel
FAN6793MY	65%	-40°C to +105°C	Green	16-Pin Small Outline Integrated Circuit Package (SOIC)	Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

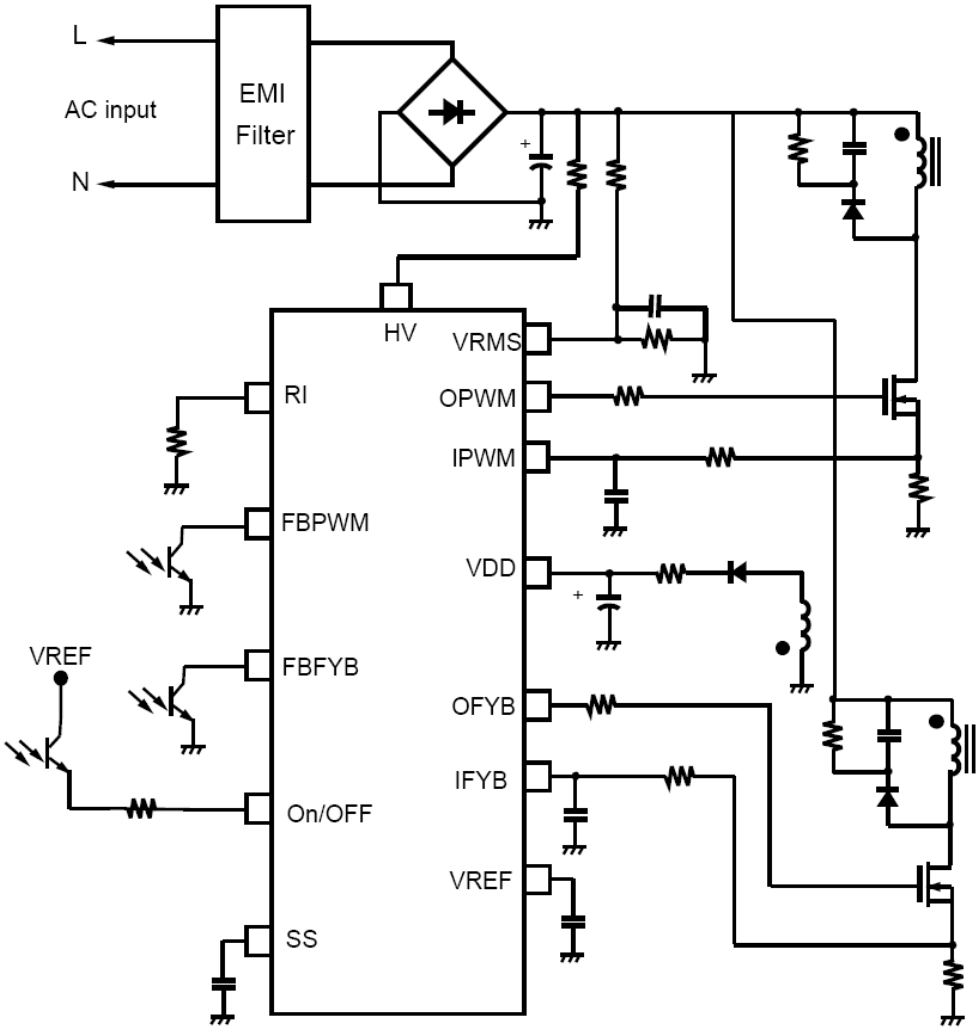


Figure 1. Typical Application

Block Diagram

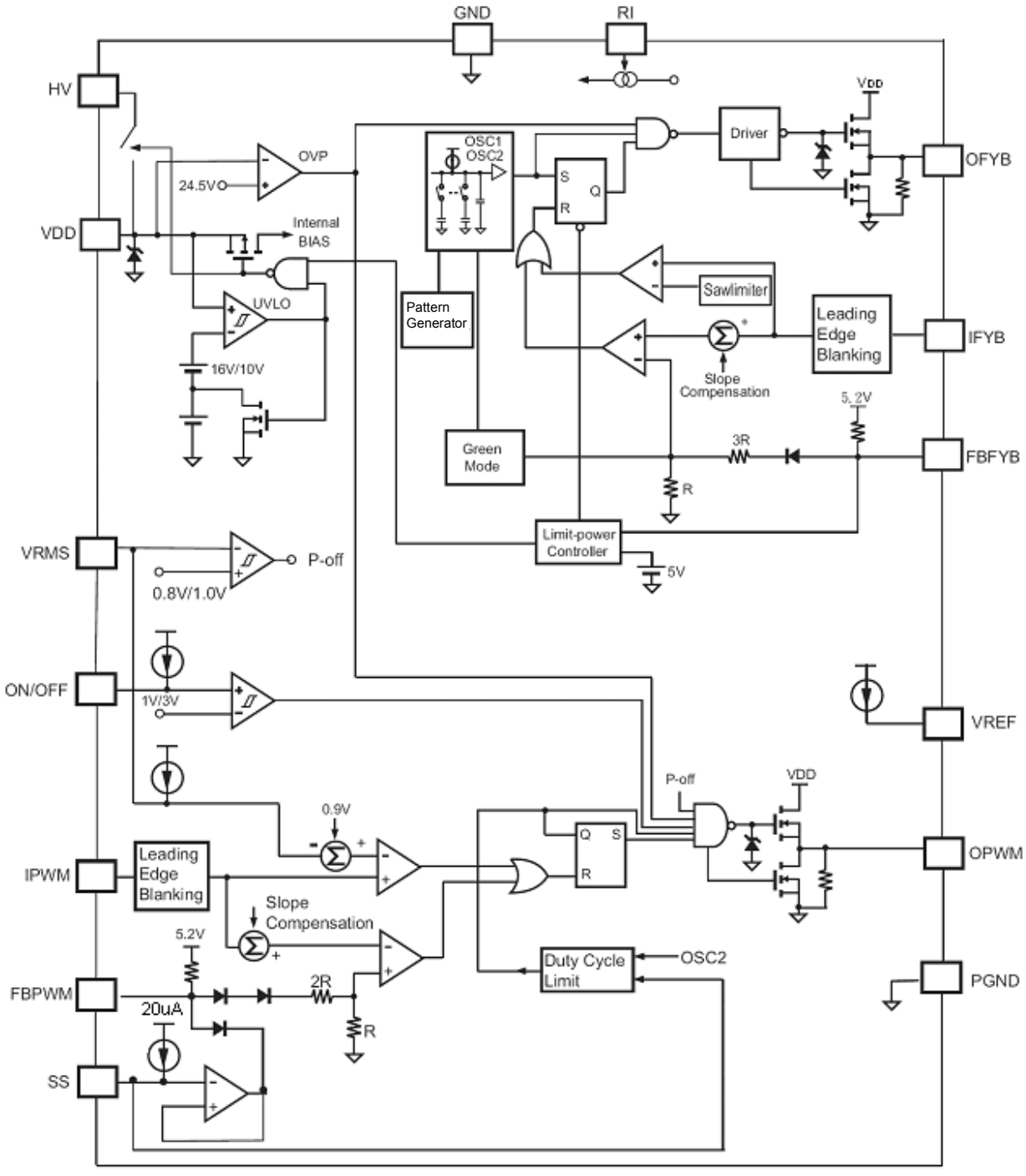
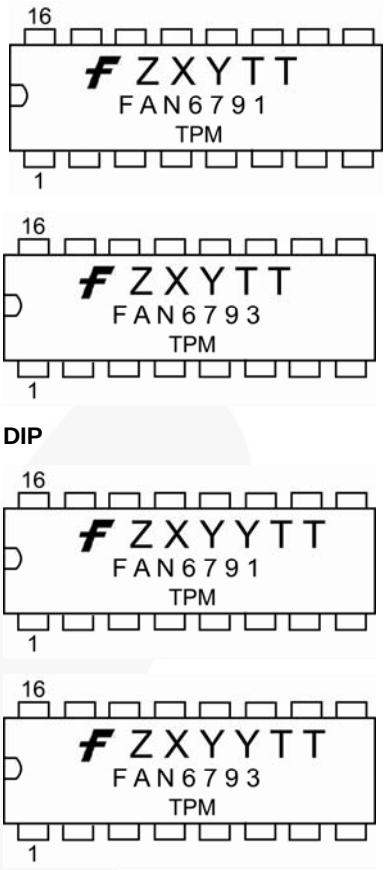


Figure 2. Function Block Diagram

Marking Information

SOIC



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die Run Code
T – Package Type (M:SOIC)
P – Y: Green Package
M – Manufacture Flow Code

DIP

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Figure 3. Top Mark

Pin Configuration

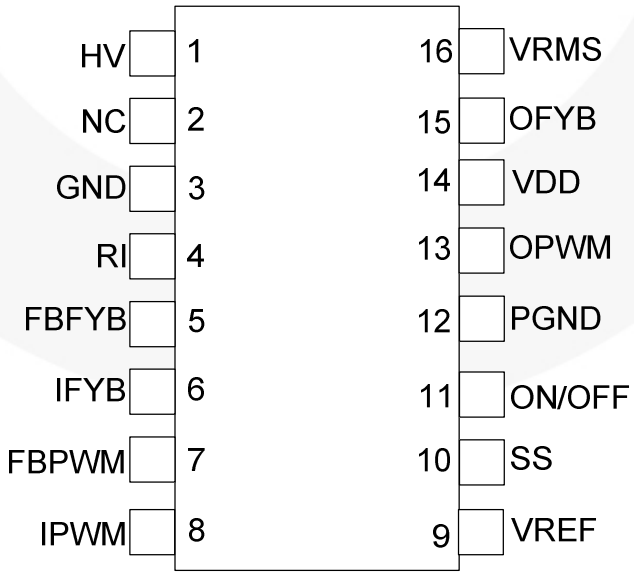

Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	HV	For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.
2	NC	No connection.
3	GND	**Ground**.
4	RI	**Oscillator Setting**. One resistor connected between RI and ground pins determines the switching frequency (resistance between 12 ~ 47kΩ is recommended). The switching frequency is equal to [1560 / RI]kHz, where RI is in kΩ. For example, if RI is equal to 24kΩ, then the switching frequency is 65kHz.
5	FBFYB	**Voltage Feedback for Flyback PWM Stage**. It is internally pulled HIGH through a 6.5kΩ resistor. An external opto-coupler from secondary feedback circuit is usually connected to this pin.
6	IFYB	**PWM Current Sense for Flyback PWM Stage**. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	FBPWM	**Voltage Feedback for Forward PWM Stage**. It is internally pulled HIGH through a 6.5kΩ resistor. An external opto-coupler from secondary feedback circuit is usually connected to this pin.
8	IPWM	**PWM Current Sense for Forward PWM Stage**. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
9	VREF	**Reference Voltage**. This pin can provide a reference voltage 5V.
10	SS	**PWM Soft-Start**. During startup, the SS pin charges an external capacitor with a 20μA constant current source. The voltage on FBPWM is clamped by SS during startup. In the event of a protection condition occurring and/or forward PWM being disabled, the SS pin quickly discharges.
11	ON/OFF	**PWM Remote ON/OFF**. Active HIGH. The forward PWM is disabled whenever the voltage at this pin is lower than 0.8V or the pin is open.
12	PGND	**Ground**. The power ground.
13	OPWM	**Forward PWM Gate Drive**. The totem-pole output drive for the forward PWM MOSFET. This pin is internally clamped under 16V to protect the MOSFET.
14	VDD	**Power Supply**. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
15	OFYB	**Flyback PWM Gate Drive**. The totem-pole output drive for the forward PWM MOSFET. This pin is internally clamped under 16V to protect the MOSFET.
16	VRMS	**Line-Voltage Detection**. The pin is used for line compensation, for forward, and brownout protection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltage, are given with respect to GND pin. Stresses beyond those listed under “absolute maximum ratings “may cause permanent damage to the device.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			27	V
V_{HV}	Input Voltage to HV Pin			500	V
V_{HIGH}	OPWM, OFYB, ON/OFF		-0.3	27.0	V
V_{LOW}	Others		-0.3	7.0	V
P_D	Power Dissipation (T_A < 50°C)			800	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
$R_{\Theta j\text{-}a}$	Thermal Resistance (Junction-to-Case)	DIP		82.5	°C/W
		SOIC		70.0	
T_L	Lead Temperature (Wave Soldering, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22-A114 (All Pins Except HV Pin)		3.5	kV
		Charged Device Model, JEDEC:JESD22-C101 (All Pins Except HV Pin)		1.5	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD}=18V; R_I=24kΩ;T_A=25°C, unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				22	V
$I_{DD\ ST}$	Startup Current	V_{DD} – 0.16V		10	50	μA
I_{DD-OP1}	Operating Current 1	V_{DD}=15V; GATE Open		6	10	mA
I_{DD-OP2}	Operating Current 2	V_{DD}=15V; GATE Open, I_{REF}=10mA		16	20	mA
V_{TH-ON}	Start Threshold Voltage		15	16	17	V
V_{TH-OFF}	Minimum Operating Voltage		9	10	11	V
V_{TH-OLP}	I_{DD-OLP} Off Voltage		6.5	7.5	8.0	V
I_{TH-OLP}	Internal Sink Current	V_{TH-OLP} +0.1V	70	80	100	μA
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Turn Off PWM with Delay)		23.4	24.5	25.5	V
t_{OVP}	V_{DD} Over-Voltage Protection Debounce	V_{DD-OVP}=26V	80	100	120	μs
HV						
I_D	Maximum Input Current	V_{AC}=90V(V_{DC}=120V), V_{DD}=10μF	1.5	2.5	3.5	mA
I_{HV-CS}	Internal Current Source	HV=500V,V_{DD}=15V		10	50	μA
Oscillator and Green-Mode Operation						
V_{RI}	RI Voltage		1.176	1.200	1.224	V
f_{OSC}	Normal PWM Frequency	Center Frequency, R_I=24kΩ	62	65	68	kHz
		Jitter Range	±3.7	±4.2	±4.7	
$f_{OSC-G-MIN}$	Minimum Frequency in Green Mode	R_I=24kΩ	18	20	22	kHz
RI	RI Range		12	24	47	kΩ
RI_{OPEN}	RI Pin Open Protection	If RI > RI_{OPEN}, PWM Turned Off	1			MΩ
RI_{SHORT}	RI Pin Short Protection	If RI > RI_{SHORT}, PWM Turned Off			6	kΩ
V_{RMS} for AC Brownout Protection						
$V_{RMS-OFF}$	Off Threshold Voltage for AC Brownout Protection		0.75	0.80	0.85	V
V_{RMS-ON}	Start Threshold Voltage for AC Brownout Protection		$V_{RMS-UVP-1}$ +0.17	$V_{RMS-UVP-1}$ +0.19	$V_{RMS-UVP-1}$ +0.21	V
t_{RMS}	AC Brownout Protection Debounce Time	R_I=24kΩ	150	195	240	ms
VREF						
V_{REF}	Reference voltage	I_{REF}=1mA, C_{REF}=0.1μF	4.75	5.00	5.25	V
$\triangle V_{REF1}$	Load Regulation of Reference Voltage	C_{REF}=0.1μF, I_{REF}=1mA to 10mA			80	mV
$\triangle V_{REF2}$	Line Regulation of Reference Voltage	C_{REF}=0.1μF, V_{DD}=12V to 22V			25	mV
I_{REF_MAX}	Maximum Current		10		15	mA
I_{OS}	V_{REF} Short Current	V_{DD}=15V	15	20	25	mA

Electrical Characteristics

V_{DD}=18V; R_I=24kΩ;T_A=25°C, unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ON/OFF						
$R_{ON/OFF}$	Impedance ON/OFF Pin		50		100	kΩ
V_{ON}	High Threshold Level of Synchronizing Signal		2.4	3.0	3.6	V
V_{OFF}	Low Threshold Level of Synchronizing Signal		0.8	1.0	1.2	V
Over Temperature Protection (OTP)						
T_{Off}	Protection Junction Temperature(1)		130	140	+150	°C
$T_{Restart}$	Restart Junction Temperature(2)		100	110	+120	°C
Flyback PWM Stage						
FBFYB Feedback Input						
A_{V-FLY}	FB Input to Current Comparator Attenuation		1/3.75	1/3.20	1/2.75	V/V
Z_{FB}	Input Impedance		4	5	7	kΩ
V_{HGH}	Output High Voltage	FB Pin Open	5.0	5.2		V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.2	4.5	4.8	V
t_{OLP}	FB Open-Loop Protection Delay		53	56	59	ms
V_N	Green Mode Entry FB Voltage		2.4	2.5	2.6	V
S_G	Slope of Green-Mode Modulation		60	75	90	Hz/mV
V_G	Green Mode Ending FB Voltage		1.8	1.9	2.0	V
$V_{OZ-OFYB}$	V_{FBPWM} for Zero Duty Cycle(Forward Turn On)		1.2	1.3	1.4	V
IFYB Current Sense						
Z_{CS}	Input Impedance			12		kΩ
V_{LIMIT1}	Peak Current Limit Threshold Voltage 1	V_{RMS}=1V	0.75	0.80	0.85	V
V_{LIMIT2}	Peak Current Limit Threshold Voltage 2	V_{RMS}=1.5V		V_{LIMIT1} -0.1		V
t_{PD}	Propagation Delay to GATE Output	V_{DD}=15V, OFYB Drops to 9V	60		120	ns
t_{BNK}	Leading-Edge Blanking Time		200	270	350	ns
ΔV_{SLOPE}	Slope Compensation	Duty=DCY_{MAX}	0.34	0.37	0.41	V
V_{S-SCP}	Threshold Voltage for SENSE Short-Circuit Protection		0.1	0.15	0.2	V
t_{D-SSCP}	Delay Time for SENSE Short-Circuit Protection	V_{SENSE}<0.15V, R_I=24KΩ	100	180	240	µs
OFYB-GATE Driver						
$V_{OFYB-CLAMP}$	Flyback PWM Gate Output Clamping Voltage	V_{DD}=22V		16	18	V
$V_{OL-OFYB}$	Output Voltage Low	V_{DD}=15V; I_O=20mA			1.5	V
$V_{OH-OFYB}$	Output Voltage High	V_{DD}=12V; I_O=20mA	8			V
t_{R-OFYB}	Rising Time	V_{DD}=15V; Gate=1nF; Gate=2~9V	30	60	120	ns
t_{F-OFYB}	Falling Time	V_{DD}=15V; Gate=1nF; Gate=9~2V	30	50	90	ns

Electrical Characteristics

V_{DD}=18V; R_I=24kΩ;T_A=25°C, unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$DCY_{MAX-OFYB}$	Maximum Duty Cycle		60	65	70	%
Forward PWM Stage						
FBPWM-Feedback Input						
A_V	FB to Current Comparator Attenuation		1/3.2	1/2.7	1/2.2	V/V
Z_{FB}	Input Impedance		4	5	7	kΩ
V_{HGH}	Output High Voltage	FB Pin Open	5.0	5.2		V
$V_{OPEN-PWM}$	PWM Open-Loop Protection Voltage		4.2	4.5	4.8	V
$t_{OPEN-PWM-HICCUP}$	Interval of PWM Open-Loop Protection Reset	R_I=24kΩ	500	600	700	ms
$t_{OPEN-PWM}$	PWM Open-Loop Protection Delay Time	R_I=24kΩ	80	95	120	ms
$V_{OZ-OPWM}$	V_{FBPWM} for Zero Duty Cycle		1.2	1.3	1.4	V
IPWM-Current Sense						
t_{PD}	Propagation Delay to Output – V_{LIMIT} Loop	V_{DD}=15V, OPWM Drops to 9V	60		120	ns
V_{LIMIT1}	Peak Current Limit Threshold Voltage 1	V_{RMS}=1V	0.75	0.80	0.85	V
V_{LIMIT2}	Peak Current Limit Threshold Voltage 2	V_{RMS}=1.5V		V_{LIMIT1}-0.1		V
t_{BNK}	Leading-Edge Blanking Time		270	350	450	ns
ΔV_{SLOPE}	Slope Compensation $\Delta V_s=\Delta V_{SLOPE}$ x (t_{on}/t) ΔV_s: Compensation Voltage Added to Current Sense		0.40	0.45	0.55	V
OPWM-GATE Driver						
$V_{OPWM-CLAMP}$	Output Voltage Maximum (Clamp)	V_{DD}=22V		16	18	V
V_{OL}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_R	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	30	60	120	ns
t_F	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	30	50	110	ns
$DCY_{MAX-OPWM}$	FAN6791 Maximum Duty Cycle	R_I=24kΩ	47	48	49	%
	FAN6793 Maximum Duty Cycle		60	65	70	
Soft Start						
I_{SS}	Constant Current Output for Soft-Start	R_I=24kΩ	17	20	23	µA
R_D	Discharge Resistance			470	564	Ω

Notes:

1. When activated, the output is disabled and the latch is turned off.
2. This is the threshold temperature for enabling the output again and resetting the latch after over-temperature protection has been activated.

Typical Characteristics

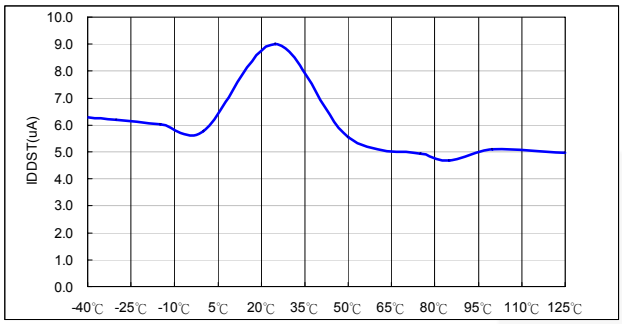

Figure 5. Startup Current I_{DD-ST} vs. Temperature

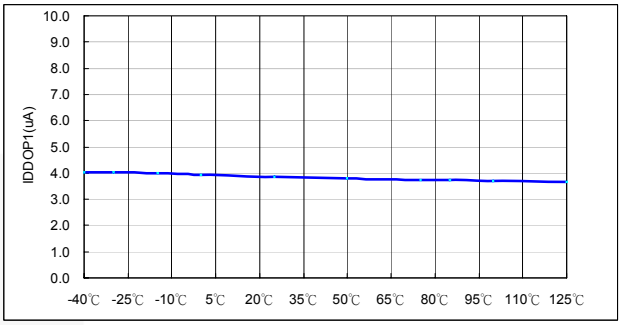

Figure 6. I_{DD-OP1} vs. Temperature

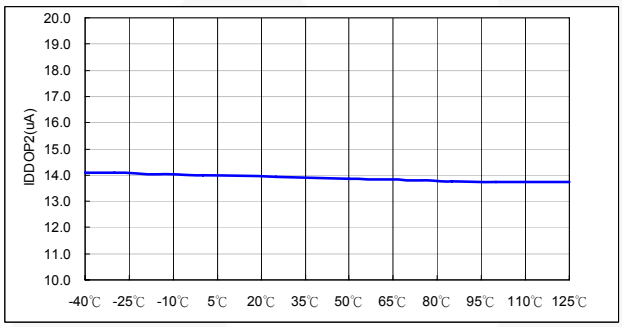

Figure 7. I_{DD-OP2} vs. Temperature

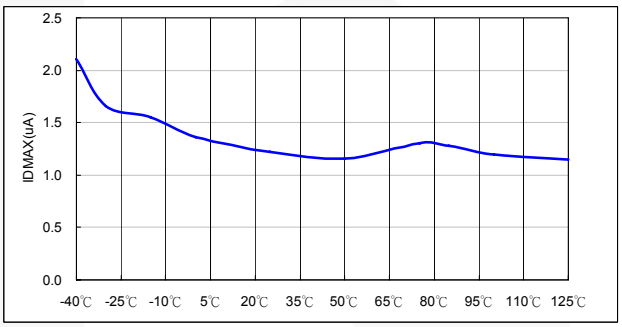

Figure 8. I_{D-MAX} vs. Temperature

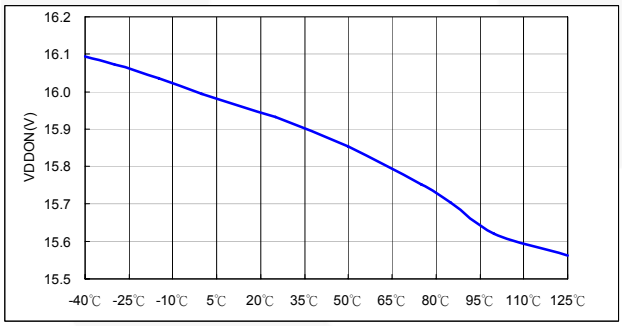

Figure 9. V_{DD-ON} vs. Temperature

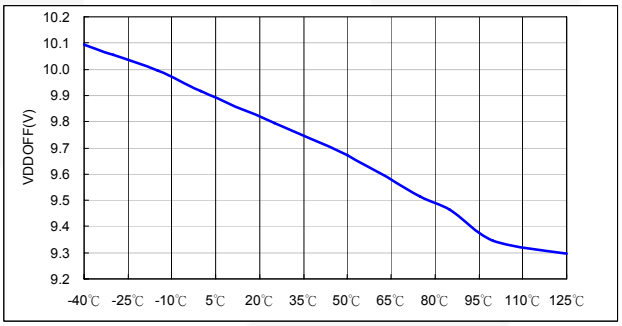

Figure 10. V_{DD-OFF} vs. Temperature

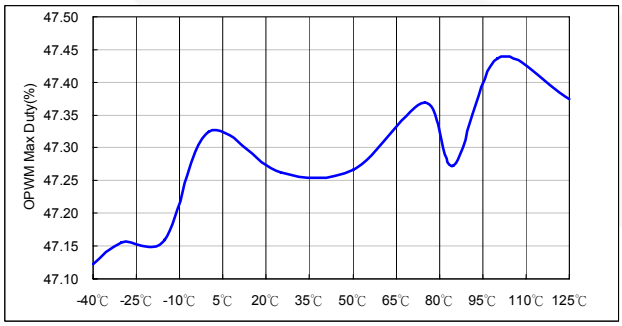

Figure 11. OPWM Maximum Duty Cycle vs. Temperature

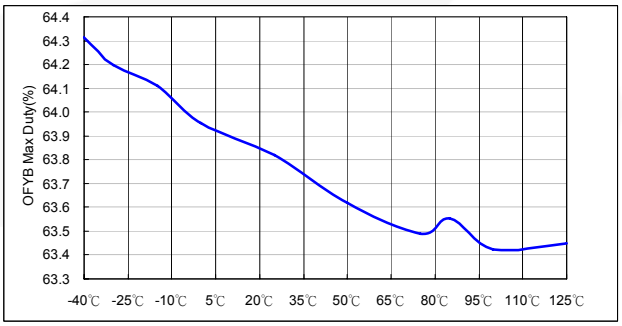

Figure 12. OFYB Maximum Duty Cycle vs. Temperature

Typical Characteristics

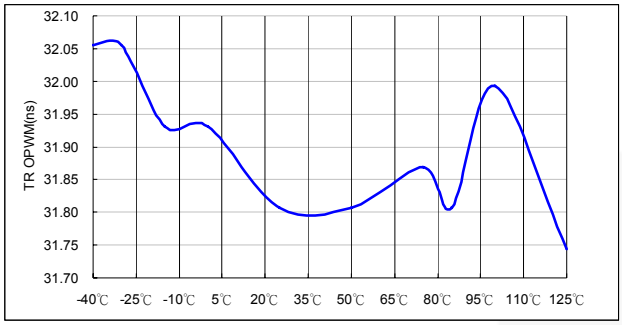

Figure 13. Rising Time $t_{R\text{-}OPWM}$ vs. Temperature

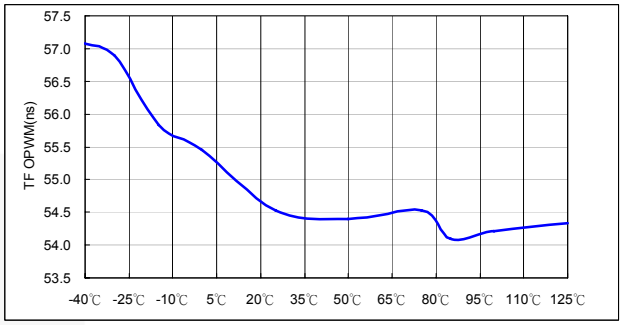

Figure 14. Falling Time $t_{F\text{-}OPWM}$ vs. Temperature

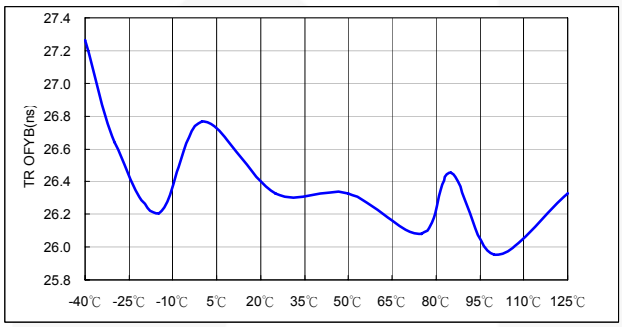

Figure 15. Rising Time $t_{R\text{-}OFYB}$ vs. Temperature

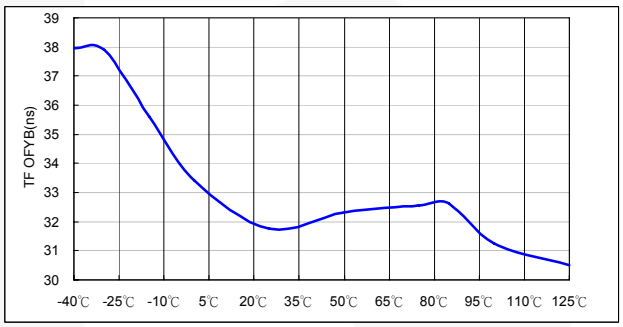

Figure 16. Falling Time $t_{F\text{-}OFYB}$ vs. Temperature

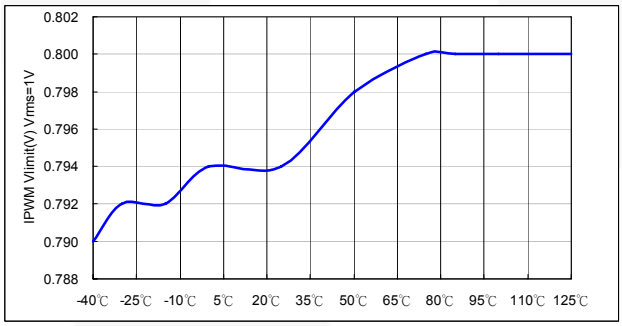

Figure 17. $I_{PWM\text{-}VLIMIT}$ (V_{RMS}=1V) vs. Temperature

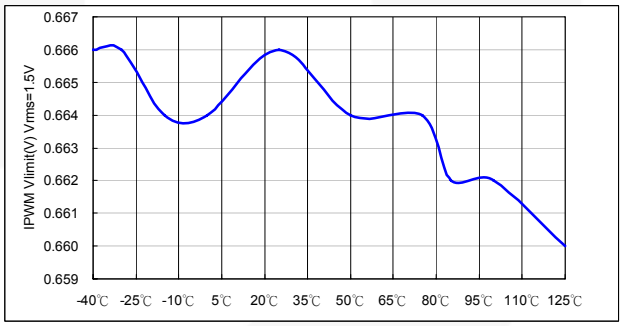

Figure 18. $I_{PWM\text{-}VLIMIT}$ (V_{RMS}=1.5V) vs. Temperature

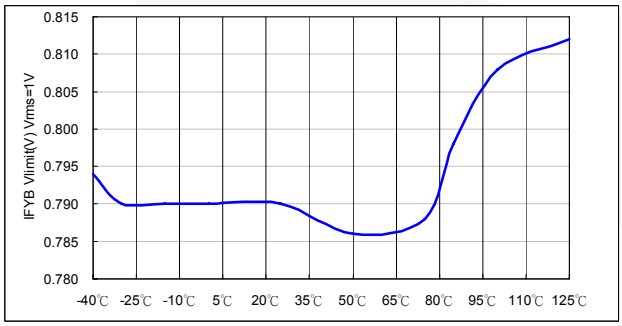

Figure 19. $I_{FYB\text{-}VLIMIT}$ (V_{RMS}=1V) vs. Temperature

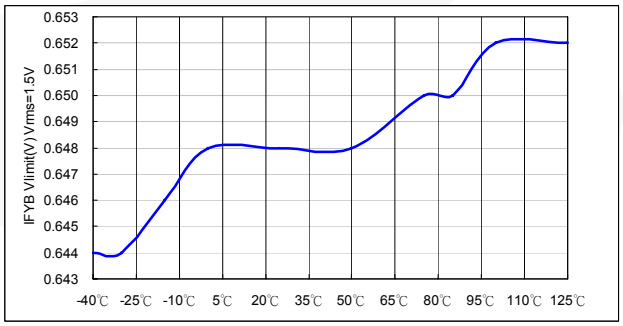

Figure 20. $I_{FYB\text{-}VLIMIT}$ (V_{RMS}=1.5V)vs. Temperature

Typical Characteristics

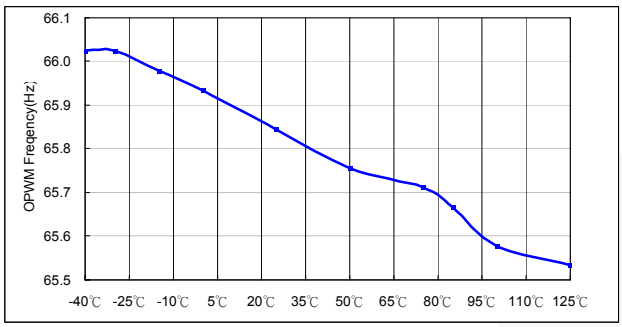

Figure 21. OPWM Frequency vs. Temperature

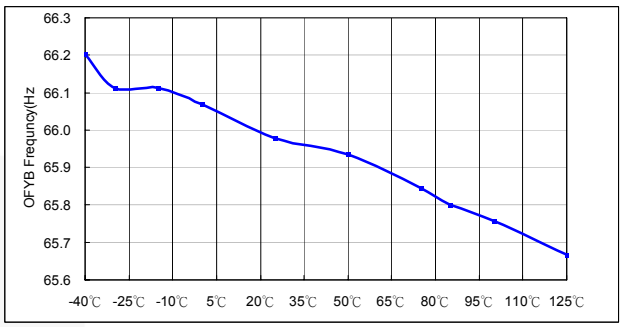

Figure 22. OFYB Frequency vs. Temperature

Functional Description

The highly integrated FAN6791/3 dual-PWM combination controller provides several features to enhance the performance of converters.

Proprietary interleave switching synchronizes the flyback and forward PWM stages. This reduces switching noise.

The proprietary frequency jittering function for the flyback and forward PWM stages helps reduce switching EMI emissions.

For the flyback and forward PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. In addition, FAN6791/3 provides complete protection functions, such as brownout protection and RI open/short.

Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through external resistor R_{HV}, recommended as 100kΩ. Typical startup current drawn from pin HV is 2mA and it charges the hold-up capacitor through the resistor R_{HV}. When the V_{DD} capacitor level reaches V_{DD-ON}, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6791/3 to maintain the V_{DD} before the auxiliary winding of the main transformer provides the operating current.

Oscillator Operation

A resistor connected from the RI pin to the GND pin generates a constant current source for the FAN6791/3 controller. This current is used to determine the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 24kΩ resistor results in a corresponding 65kHz PWM frequency. The switching frequency is programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$f_{PWM} = \frac{1560}{R_I(k\Omega)}(kHz) \quad (1)$$

The range of the PWM oscillation frequency is designed as 33kHz ~ 130kHz. FAN6791/3 integrates frequency hopping function internally. The frequency variation ranges from around 61kHz to 69kHz for a center frequency 65kHz. The frequency hopping function helps reduce EMI emission of a power supply with minimum line filters.

For power saving, flyback PWM stage has a green mode function. Frequency linearly decreases when V_{FB} is within V_G and V_N. Once V_{FB} is lower than V_G, switching frequency disables, and it enters burst mode.

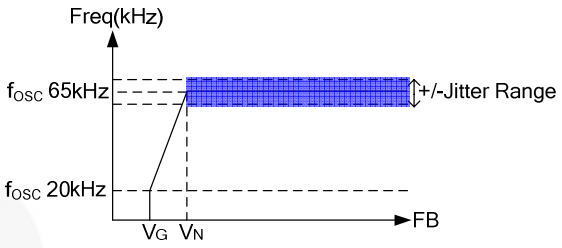

Figure 23. Oscillation Frequency in Green Mode

Line Voltage Detection (V_{RMS})

Figure 24 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The V_{RMS} voltage is used for high/low line compensation that keeps the constant power limit and provides brownout protection. For brownout protection, when the V_{RMS} voltage drops below 0.8V, OPWM turns off.

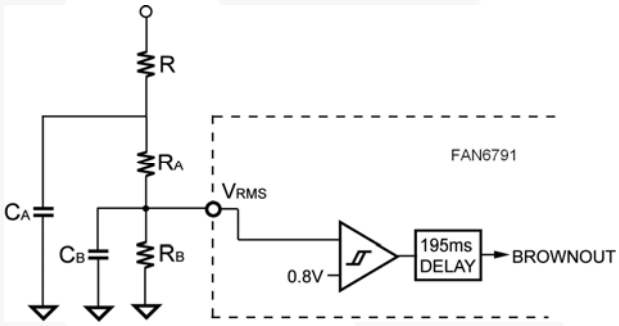

Figure 24. Line-Voltage Detection on VRMS Pin

Remote On/Off

Figure 25 shows the remote on / off function. When the supervisor FPO pin pulls down and enables the system by connecting an opto-coupler, V_{REF} applies to the ON/OFF pin to enable forward PWM stage.

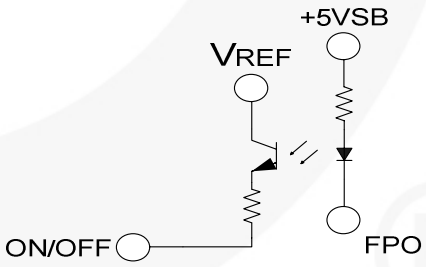

Figure 25. Remote On/Off

Interleave Switching

The FAN6791/3 uses interleaved switching to synchronize the stand-by PWM / forward PWM stages. This reduces switching noise and spreads the EMI emissions. Figure 26 shows that an off-time t_{OFF} is inserted in between the turn-off of the stand-by gate drives and the turn-on of the forward PWM.

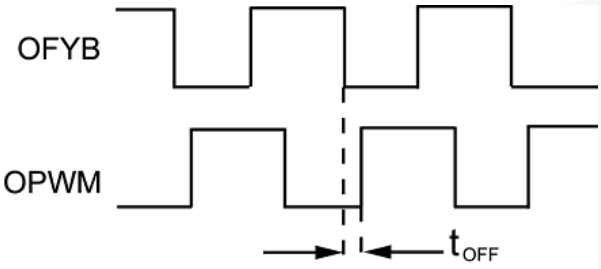

Figure 26. Interleaved Switching

Slope Compensation

The stand-by PWM and forward PWM stage are designed for flyback and forward power converters. Peak-current-mode control is used to optimize system performance. Slope compensation is added to stabilize the current loop. The FAN6791/3 inserts a synchronized, positively sloped ramp at each switching cycle. The positively sloped ramp is represented by the voltage signal $V_{s\text{-}comp}$ in Figure 27.

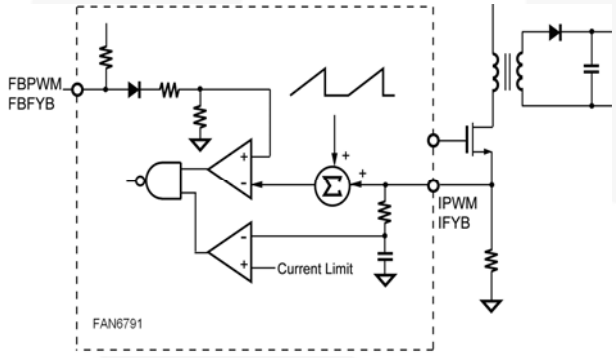

Figure 27. Slope Compensation

Gate Drivers

FAN6791/3 output stages are fast totem-pole gate drivers. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET.

Constant Power Control

To limit the output power of the converter constantly, a power-limit function is included. Sensing the converter input voltage through the VRMS pin, the power limit function generates a relative peak-current-limit threshold voltage for constant power control, as shown in Figure 28.

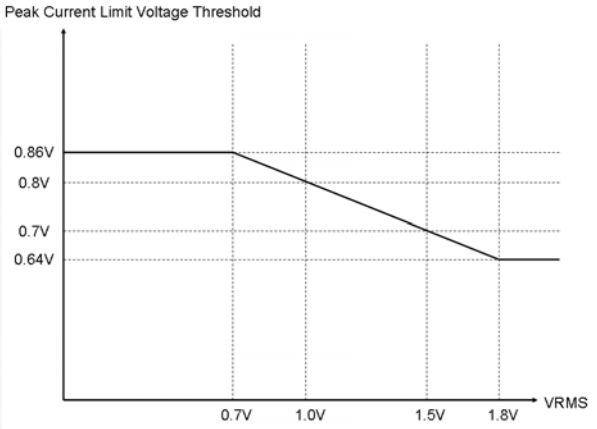

Figure 28. Constant Power Control

Protections

The FAN6791/3 provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

V_{DD} Over-Voltage Protection. The stand-by PWM and forward PWM stages will be disabled whenever the V_{DD} voltage exceeds the over-voltage threshold.

AC Under-Voltage Protection. The VRMS pin is used to detect the AC input voltage. When voltage is lower than the brownout threshold, voltage disables both forward and stand-by PWM.

RI Pin Open / Short Protection. The RI pin is used to set the switching frequency and internal current reference. The stand-by PWM and forward PWM stages are disabled whenever the RI pin is short or open.

Open-Loop Protection. The stand-by PWM and forward PWM stages of FAN6791/3 is disabled whenever the FBFYB / FBPWM pin is open.

Reference Circuit

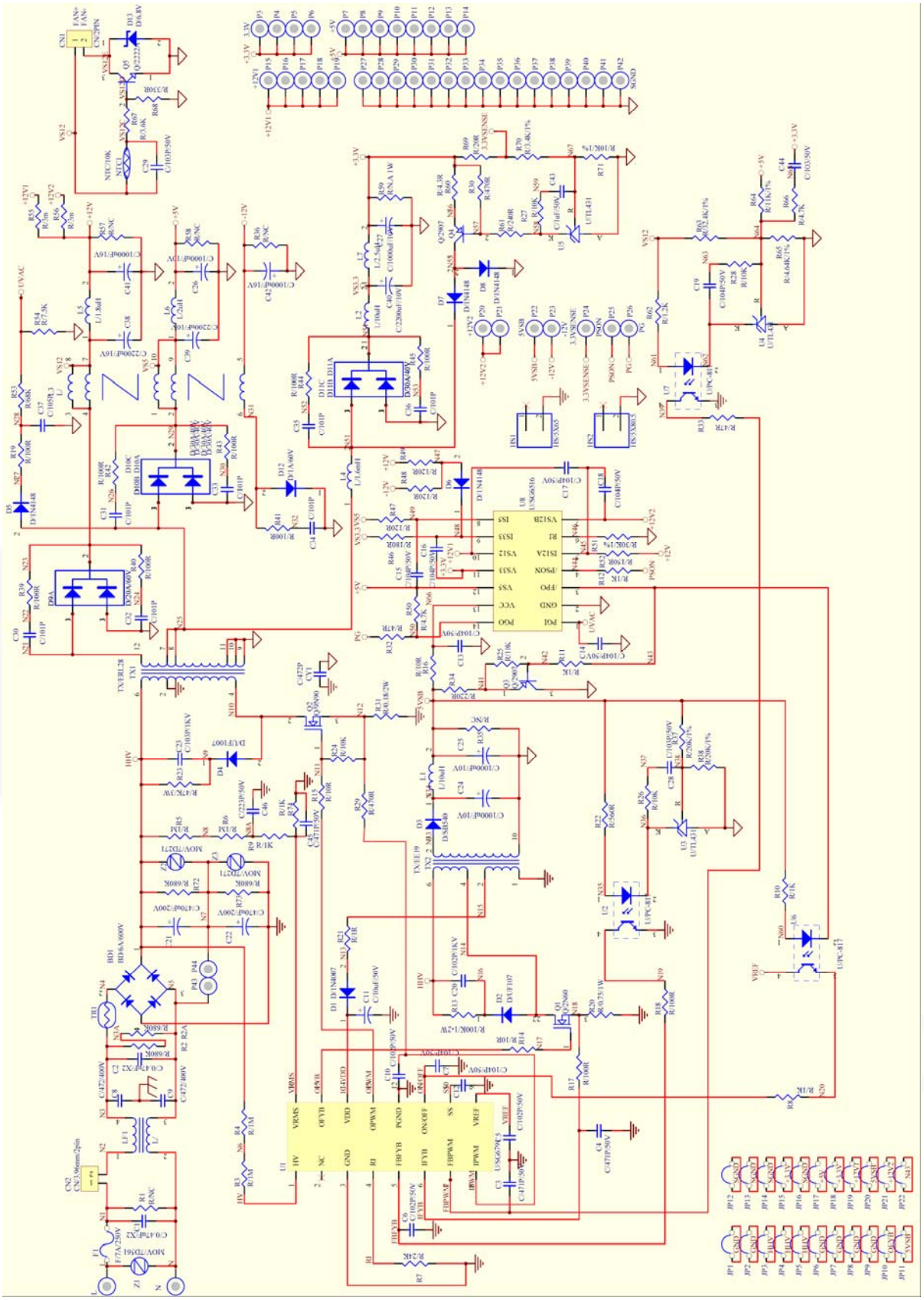

Figure 29. Reference Circuit

Build Of Materials List

Reference	Component	Reference	Component
C1	C/0.47μF/X2	R18	R/100 1/8W
C2	C/0.47μF/X2	R20	R/1/1W
C3	C/471P/50V	R21	R/1 1/8W
C4	C/471P/50V	R22	R/402 1/8W
C5	C/102P/50V	R23	R/47K 3W
C6	C/102P/50V	R24	R/10K 1/8W
C7	C/102P/50V	R26	R/2K 1/8W
C8	C/472/400V	R29	R/470 1/8W
C9	C/472/400V	R31	R/0.1/2W
C10	C/102P/50V	R35	R/N.A 1/4W
C11	C/10μF/50V	R37	R/20K 1% 1/8W
C12	C/104P/50V	R38	R/20K 1% 1/8W
C20	C/102P/1KV	Q1	2N/60
C21	C/470μF/200V	Q2	9N90
C22	C/470μF/200V	Z3	7D271
C23	C/103P/1KV	Z2	7D271
C24	C/1000μF/10V	Z1	7D561
C25	C/330μF/10V	D1	D/1N4007
C28	C/103P/50V	D2	D/UF107
R1	R/680K 1/4W NC	D3	D/SB540
R2	R/680K 1/4W	D4	D/UF1007
R3	R/51.1K 1/4W	BD1	D/6A/600V
R4	R/51.1K 1/4W	U1	SG6791/3
R5	R/2.4M 1/4W	U2	PC-817
R6	R/2.4M 1/4W	U3	TL431
R7	R/24K 1/8W	U6	PC-817
R8	R/1K 1/8W		
R9	R/19.1K 1/8W		
R10	R/1K 1/8W		
R13	R/100K 1/2W		
R14	R/10 1/8W		
R15	R/10 1/8W		
R17	R/100 1/8W		

Physical Dimension

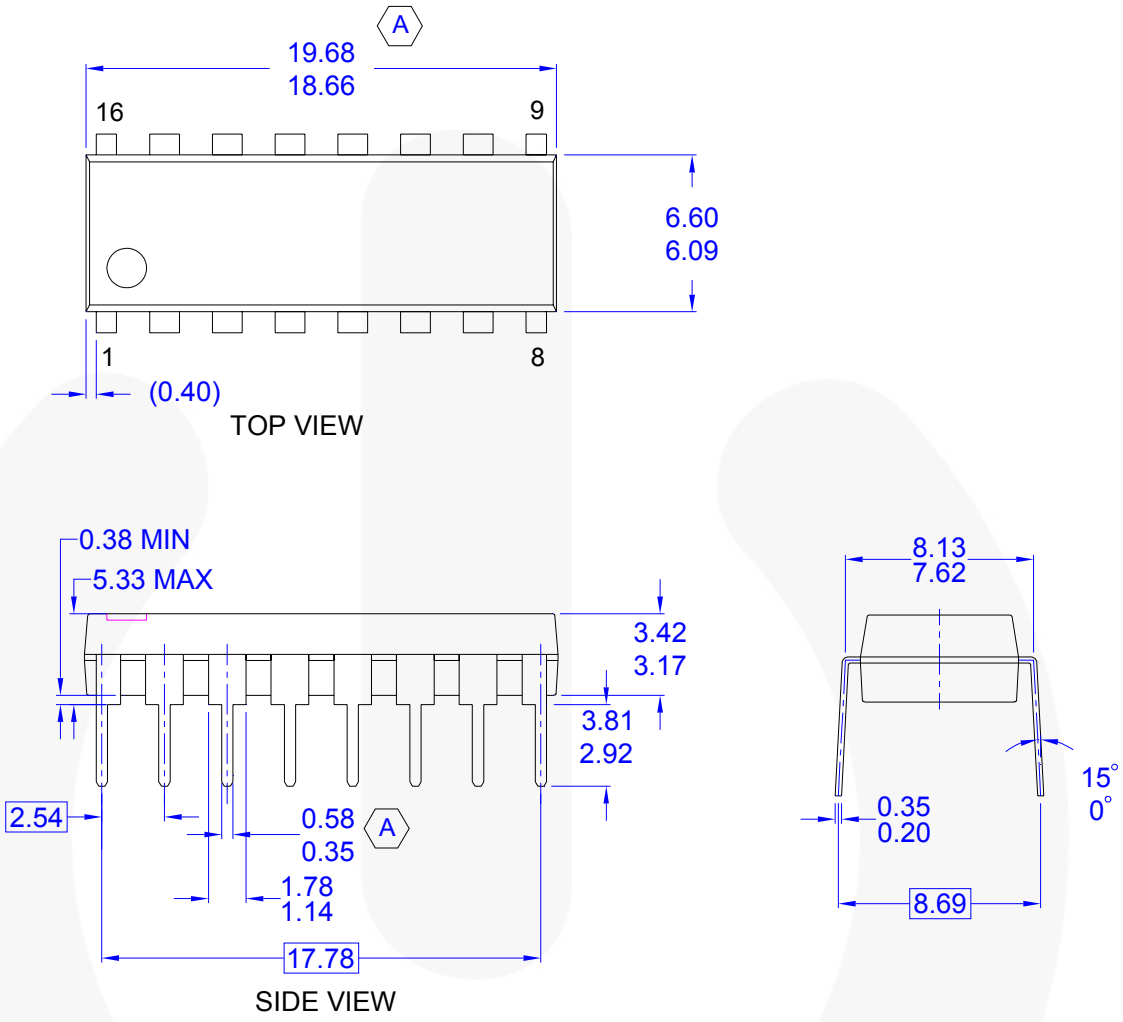

Figure 30. 16-Pin, Dual In-Line Package (DIP)

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Physical Dimensions (Continued)

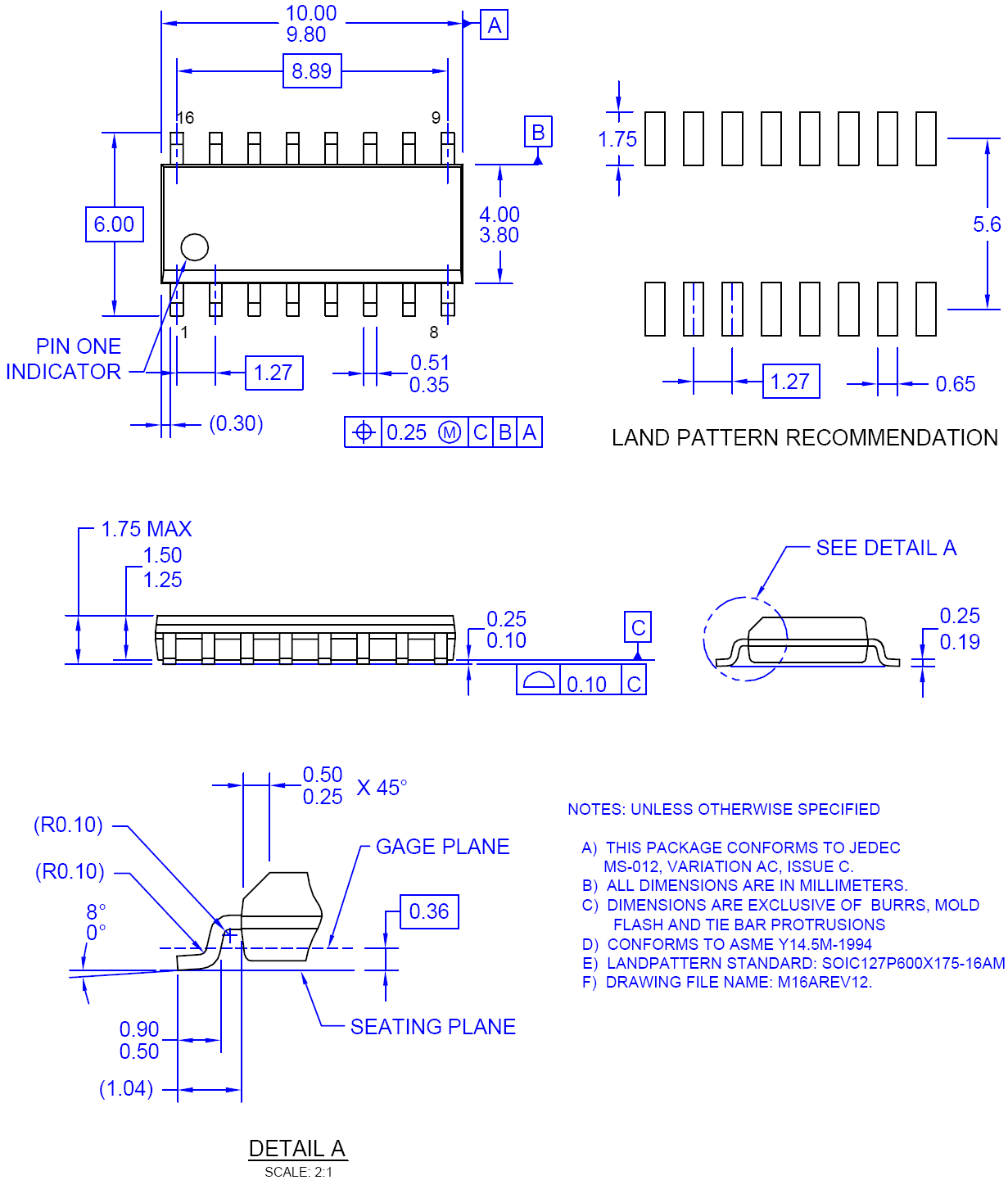

Figure 31. 16-Pin, Small Outline Integrated Circuit (SOIC)

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