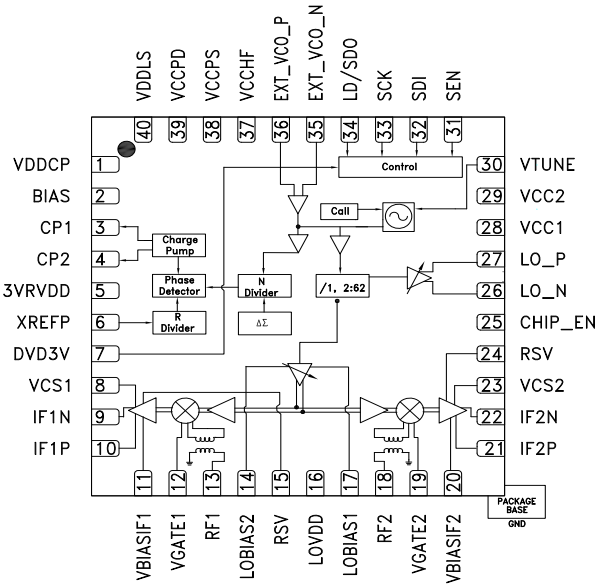
BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Typical Applications

The HMC1190LP6GE is Ideal for:

- Multiband/Multi-standard Cellular BTS Diversity Receivers
- GSM & 3G & LTE/WiMAX/4G
- MIMO Infrastructure Receivers
- Wideband Radio Receivers
- Multiband Basestations & Repeaters

Functional Diagram



Features

Broadband Operation with no external matching

High-side and Low-side LO injection Operation

High Input IP3 of +24 dBm

Power Conversion Gain of 8.9 dB

Input P1dB of 11 dBm

SSB Noise Figure of 9 dB

55 dBc Channel-to-Channel Isolation

Enable/Disable Mixer and PLLVCO independently

Single-ended RF input ports

Maximum Phase Detector Rate: 100 MHz

Low Phase Noise: -110 dBc/Hz in Band Typical

PLL FOM:

-230 dBc/Hz Integer Mode, -227 dBc/Hz Fractional Mode

< 180 fs Integrated RMS Jitter (1 kHz to 20 MHz)

LO Low Noise Floor: -165 dBc/Hz

Mixer Low Noise Floor: -161 dBc/Hz

Integrated VCO

External VCO Input, differential LO output

Exact Frequency Mode:
0 Hz Fractional Frequency Error

Programmable RF Output Phase

Output Phase Synchronous Frequency Changes

Output Phase Synchronization

LO Output Mute Function

Compact Solution, 6x6 mm Leadless QFN Package

General Description

The HMC1190LP6GE is a high linearity broadband dual channel downconverting mixer with integrated PLL and VCO optimized for multi-standard receiver applications that require a compact, low power design. Integrated wideband limiting LO amplifiers enable the HMC1190LP6GE to achieve an unprecedented RF bandwidth of 700 MHz to 3500 MHz for applications including Cellular/3G, LTE/WiMAX/4G. Unlike conventional narrow-band downconverters, the HMC1190LP6GE supports both high-side and low-side LO injection over all RF frequencies. The RF and LO input ports are internally matched to 50 Ohms.

The HMC1190LP6GE features an integrated LO and RF baluns, enable control of IF and LO amplifiers and bias control interface to high linearity passive mixer cores. Balanced passive mixer combined with high-linearity IF amplifier architecture provides excellent LO-to-RF, LO-to-IF, and RF-to-IF isolations. Low noise figure of 9 dB, and high IIP3 of +24 dBm allow the HMC1190LP6GE to be used in most demanding applications. External bias control pins enable optimization of already low power dissipation of 2.34 W (typical). Fast enable control interface reduces power consumption further in TDD applications.

External VCO input allows the HMC1190LP6GE to lock external VCOs, and enables cascaded LO architectures for MIMO applications. Two separate Charge Pump (CP) outputs enable separate loop filters optimized for both integrated and external VCOs, and seamless switching between integrated or external VCOs during operation. Programmable RF output phase features can further phase adjust and synchronize multiple HMC1190LP6GE's enabling scalable MIMO and beam-forming radio architectures.

Additional features include configurable LO output mute function, Exact Frequency Mode that enables the HMC1190LP6GE to generate fractional frequencies with 0 Hz frequency error, and the ability to synchronously change frequencies without changing phase of the output signal that increases efficiency of digital pre-distortion loops. The HMC1190LP6GE is housed in RoHS compliant compact 6x6 mm leadless QFN package.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Electrical Specifications, (Unless Otherwise Specified, the Following Test Conditions Were Used)

T_A = +25°C, IF Frequency = 150 MHz, LO Power is set to '3' [1], RF Input Power = -5 dBm, LOVDD=3VRVDD=DVDD3V=CHIPEN= 3V, VDDCP=VCS1=VCS2=VBIASIF1=VBIASIF2= LOBIAS1=LOBIAS2=VCC1=VCC2=VGATE1=VGATE2=5V, VGATE = 4.8V.

Parameter	Typical				Units
Mixer Core RF Input Frequency Range	700 - 3500				MHz
Mixer Core IF Output Frequency Range	50 - 350				MHz
	RF=900 MHz[2]	RF=1900 MHz[3]	RF=2200 MHz [3]	RF=2700 MHz [3]	
Conversion Gain	9.3 [5]	8.4 [5]	8.1 [5]	7.1 [5]	dB
IP3 (Input)	24.5	24	23.5	23.5	dBm
Noise Figure (SSB)	8.5	9.2	9.5	10	dB
1 dB Compression (Input)	10.7	11.4	11.2	12	dBm
LO leakage @ RF port	-67	-58	-59	-58	dBm
RF to IF Isolation	40	46	45	52	dB
Channel to Channel Isolation [4]	53	49	48	48	dBc
+2RF-2LO Response	68	67	70	72	dBc
+3RF-3LO Response	69	68	74	78	dBc

[1] LO Power Level can be adjusted using Reg 16h.

[2] High Side LO injection, VGATE1,2 = 5V

[3] Low Side LO injection, VGATE1,2 = 4.8V

[4] RF1 input power= -5 dBm, measurement taken from IF2 output. RF2 and IF1 ports are terminated with 50 Ohms.

[5] Balun losses at IF output ports are de-embedded.

DC Power Supply Specifications

Parameter		Min.	Typ.	Max.	Units.
5 V Supply Rails (VDDCP, VCS1, VCS2, VDDLS, VBIASIF1, VBIASIF2, LOBIAS1, LOBIAS2, VCC1, VCC2, VGATE1, VGATE2)		+4.8	+5	+5.2	V
			348 [1]		mA
3.3 V Supply Voltage (LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF)		+3.1	+3.3	+3.5	V
			198		mA
Mixer Core Supply Currents when IF1EN and IF2EN are Enabled	VDDIF (5 V)		160		mA
	VCS1 + VCS2 (5 V)		3.3	4.2	mA
	VBIASIF1 + VBIASIF2 (5 V)		24	28	mA
	VGATE1 + VGATE2 (5 V)		8	9.2	mA
	LOBIAS1 + LOBIAS2 (5 V)		4.6	5.6	mA
	LOVDD (3.3 V)		140	148	mA

[1] LO Frequency=2400 MHz, LO_MIX Power and LO_OUT Power set to '3', LO_MIX and LO_OUT is differential and LO_OUT is off. When LO_OUT enabled in differential mode the bias current increases by 34 mA (Typ.)

DC Power Supply Specifications (Continued)

Parameter		Min.	Typ.	Max.	Units.
PLL/VCO Core Supply Currents when CHIPEN is Enabled	Charge Pump (VDDCP, +5 V) +VCCLS		6		mA
	LO_OUT differential, LO_MIXER off [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 148 58		 mA mA
	LO_OUT single-ended, LO_MIXER off [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 131 58		 mA mA
	LO_OUT off, LO_MIXER differential [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 148 58		 mA mA
	LO_OUT off, LO_MIXER single-ended [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 131 58		 mA mA
	LO_OUT differential, LO_MIXER differential [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 182 58		 mA mA
	LO_OUT single-ended, LO_MIXER single-ended [1] 5 V Supplies (VDDLS, VCC1, VCC2, VDDCP) 3.3 V Supplies (3VRVDD, DVDD3V, VCCHF, VCCPS, VCCPD)		 150 58		 mA mA
	VCCPD, VCCPS, VCCHF, DVDD3V, 3VRVDD (+3.3V)		58	64	mA
Mixer Core Supply Currents when IF1EN and IF2EN are Disabled	VDDIF (5V)		0		mA
	VCS1 + VCS2 (5V)		4		mA
	VBIASIF1 + VBIASIF2 (5V)		3.5		mA
	VGATE1 + VGATE2 (5V)		4		mA
	LOBIAS1 + LOBIAS2 (5V)		5.5		mA
	LOVDD (3.3 V)		4		mA
PLL/VCO Core Supply Currents when CHIPEN is Disabled	VDDCP, VCC1, VCC2, VDDLS (5V) [1]		3		mA
	3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF (3.3V) [1]		1		mA

[1] LO Frequency=2400 MHz, LO_MIX and LO_OUT outputs set to maximum gain.

PLL & VCO Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Logic Inputs					
Logic High		1.2			V
Logic Low				0.6	V
Input Current				+/- 1	uA
Input Capacitance			2		pF
LO Output Characteristics					
LO Output Frequency		50		4100	MHz
VCO Frequency at PLL Input		2000		4100	MHz
VCO Fundamental Frequency		2000		4100	MHz
VCO Output Divider					
VCO Output Divider Range	1, 2, 4, ... 60, 62	1		62	
PLL RF Divider Characteristics					
19-Bit N Divider Range	Integer	16		524287	
	Fractional	20		524283	
Phase Detector (PD)					
PD Frequency	Fractional Mode	DC		100	MHz
	Integer Mode	DC		100	MHz
Harmonics					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-30/-22/-32		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,... 62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynami-cally max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled	1	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-\Bit R-Divider Range		1		16,383	
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-167		dBc/Hz

PLL & VCO Specifications *(Continued)*

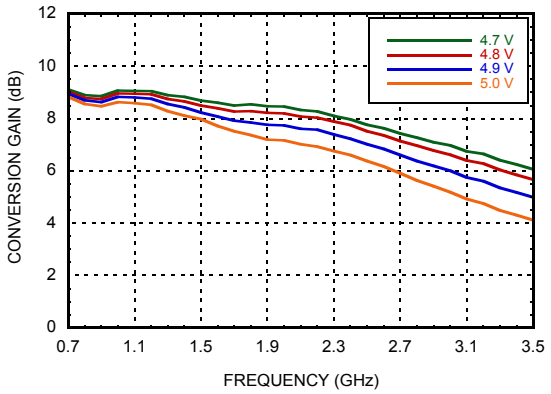
Parameter	Conditions	Min.	Typ.	Max.	Units
VCO Open Loop Phase Noise at fo @ 3 GHz/2 = 1.5 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 3862 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3643 MHz	Measured at 2.5 V		14.5		MHz/V
VCO Tuning Sensitivity at 3491 MHz	Measured at 2.5 V		16.2		MHz/V
VCO Tuning Sensitivity at 3044 MHz	Measured at 2.5 V		14.6		MHz/V
VCO Tuning Sensitivity at 2558 MHz	Measured at 2.5 V		15.4		
VCO Tuning Sensitivity at 2129 MHz	Measured at 2.5 V		14.8		
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

Enable/Disable Settling Time Specifications

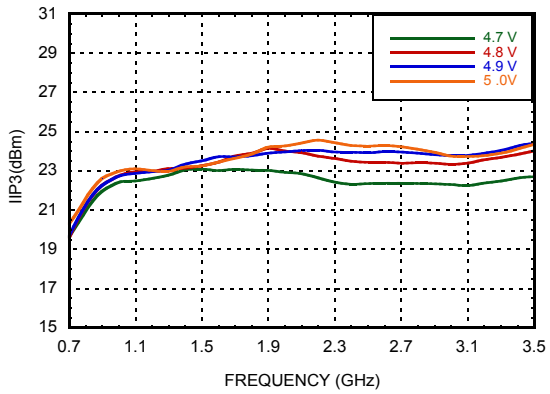
Parameter	Conditions	Min.	Typ.	Max.	Units
Enable Settling Time	Mixer Core Enabled		140		ns
Disable Settling Time	Mixer Core Disabled		110		ns

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

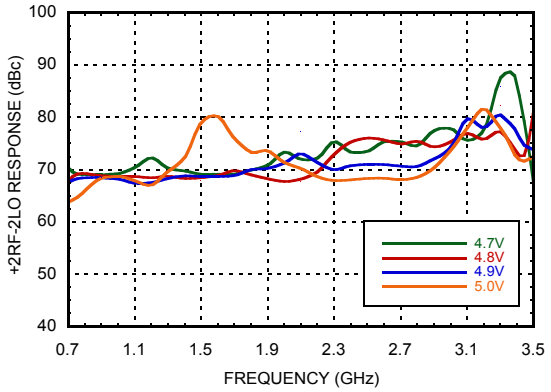
Conversion Gain vs. VGATE[1] [2]



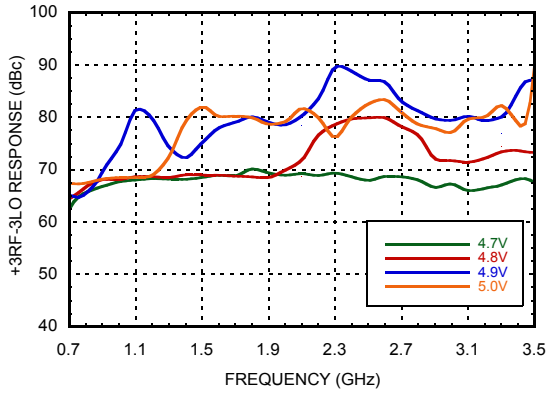
Input IP3 vs. VGATE[1]



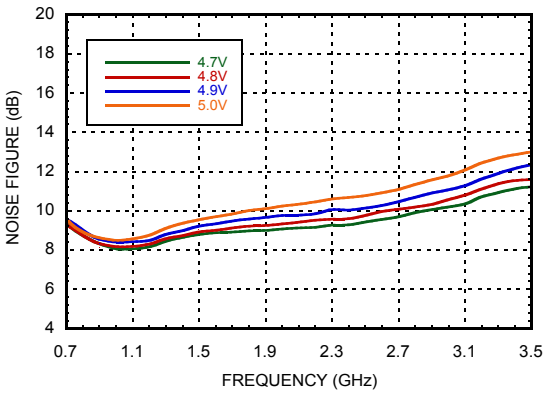
+2RF -2LO Response vs. VGATE[1]



+3RF -3LO Response vs. VGATE[1]

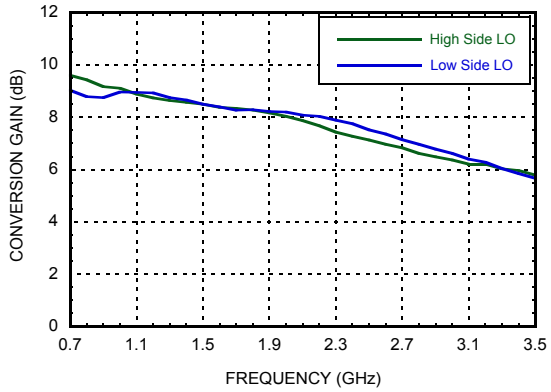


Noise Figure vs. VGATE[1]

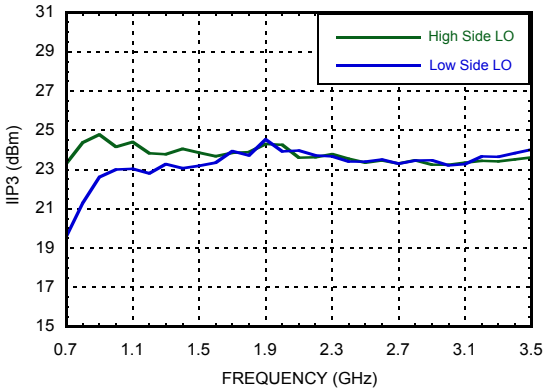


[1] VGATE is bias voltage for passive mixer cores (VGATE1 and VGATE2 pins). Refer to pin description table.
[2] Balun losses at IF output ports are de-embedded.

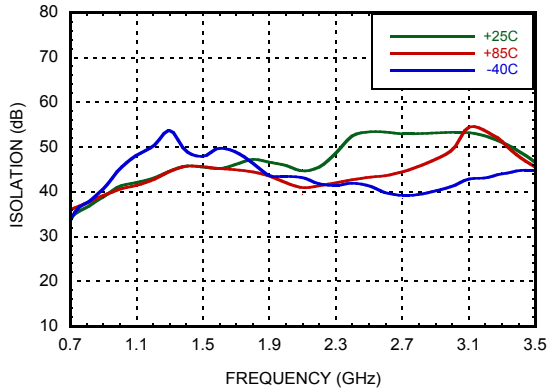
Conversion Gain vs. High Side LO & Low Side LO @ VGATE=4.8V [1]



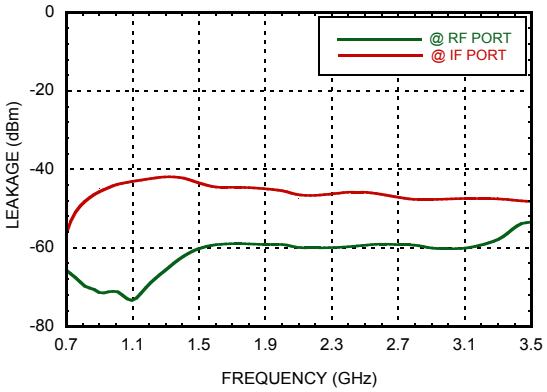
Input IP3 vs. High Side LO & Low Side LO @ VGATE=4.8V



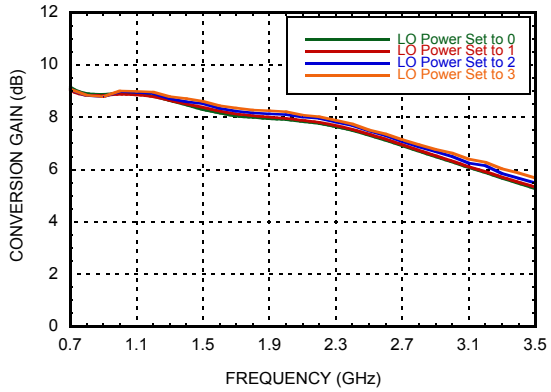
RF/IF Isolation vs. Temperature @ VGATE=4.8V



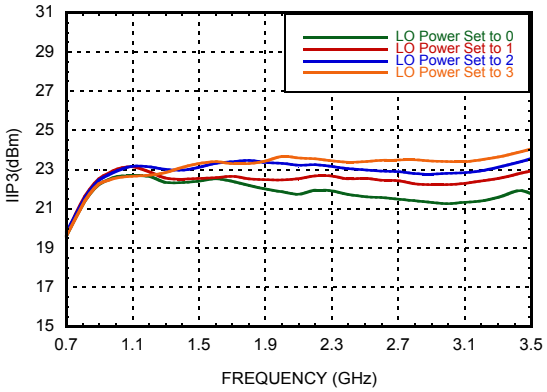
LO Leakage @ VGATE=4.8V



Conversion Gain vs. LO Drive @ VGATE=4.8V [1]



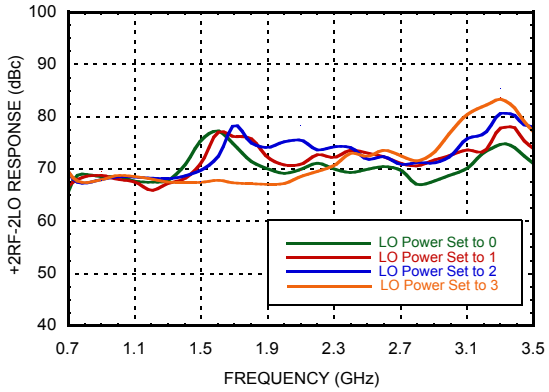
Input IP3 vs. LO Drive @ VGATE=4.8V



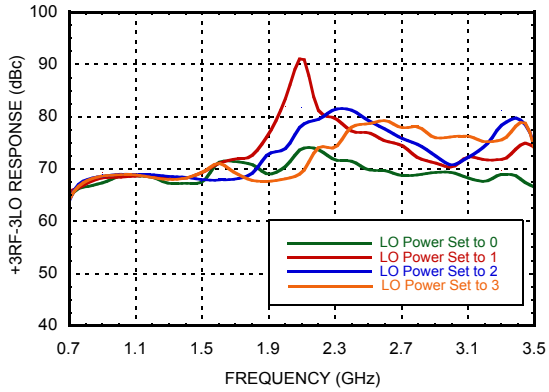
[1] Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

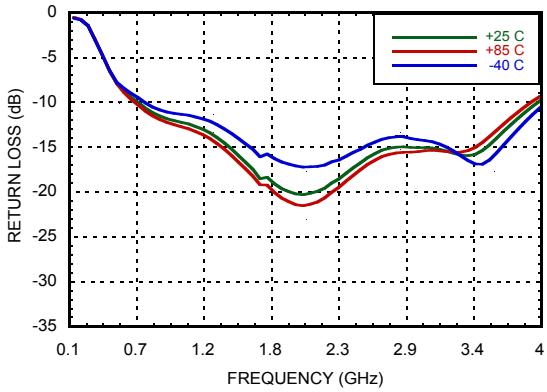
+2RF -2LO Response vs. LO Drive @ VGATE=4.8V



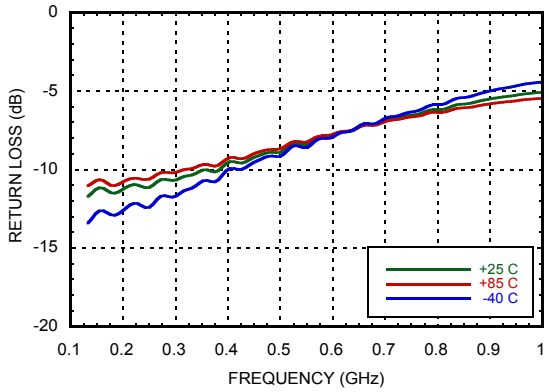
+3RF -3LO Response vs. LO Drive @ VGATE=4.8V



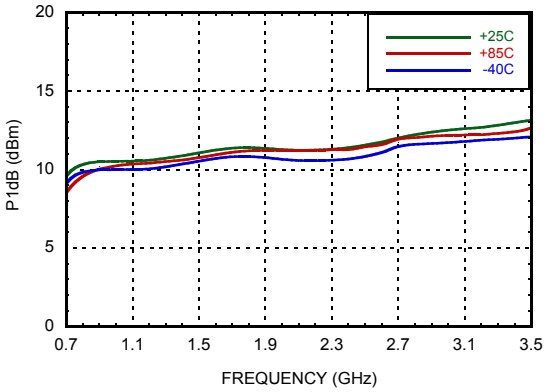
RF Input Return Loss @ VGATE=4.8V [1]



IF Output Return Loss @ VGATE=4.8V [1]



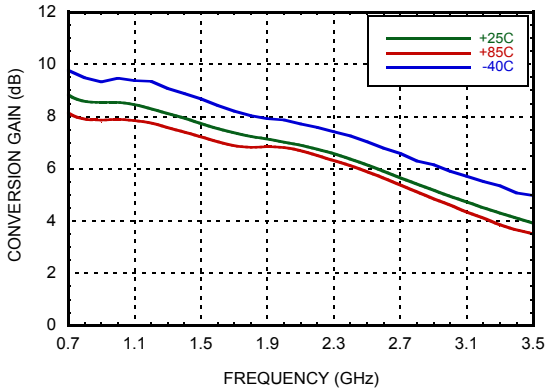
Input P1dB vs. Temperature @ VGATE=4.8V



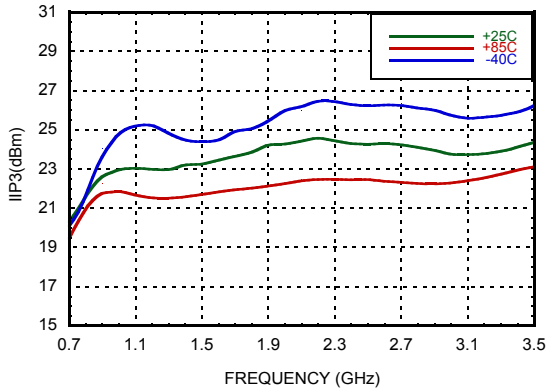
[1] LO input Frequency = 1700MHz, LO power = 0 dBm.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

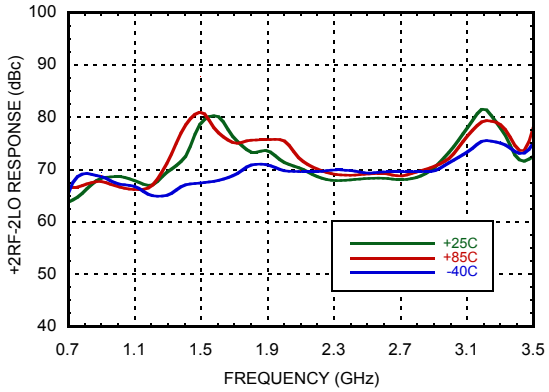
Conversion Gain vs. Temperature @ VGATE=5.0V [1]



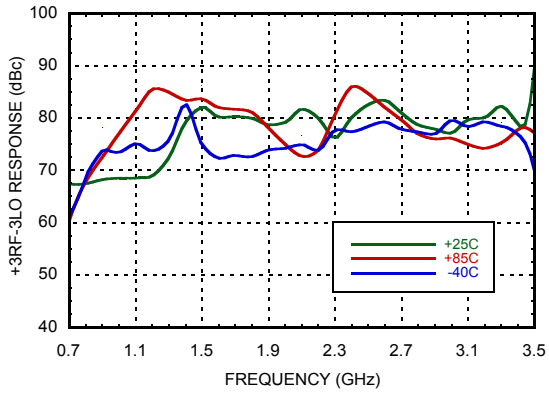
Input IP3 vs. Temperature @ VGATE=5.0V



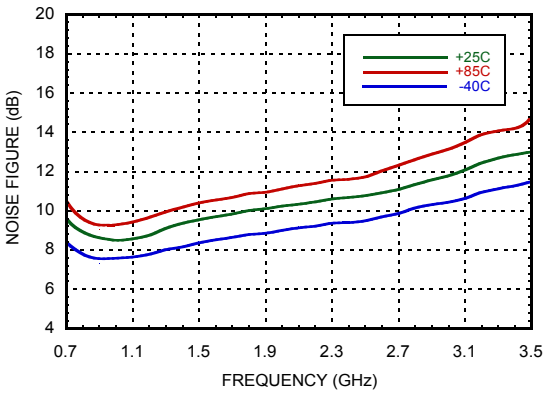
+2RF -2LO Response vs. Temperature @ VGATE=5.0V



+3RF -3LO Response vs. Temperature @ VGATE=5.0V

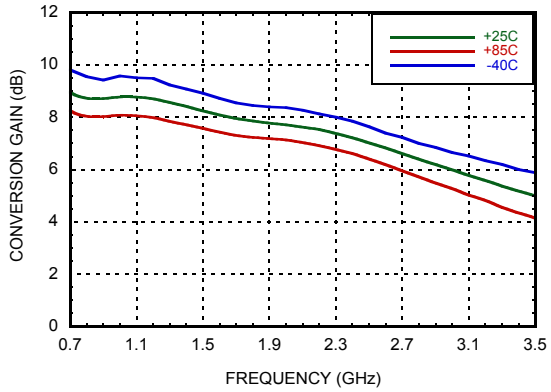


Noise Figure vs. Temperature @ VGATE=5.0V

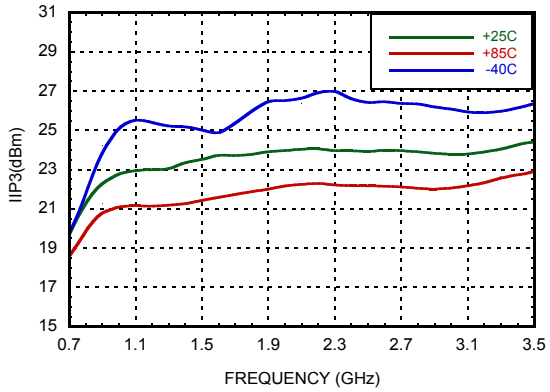


[1] Balun losses at IF output ports are de-embedded.

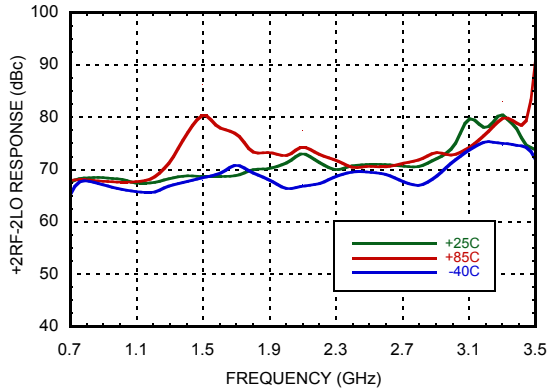
Conversion Gain vs. Temperature @ VGATE=4.9V [1]



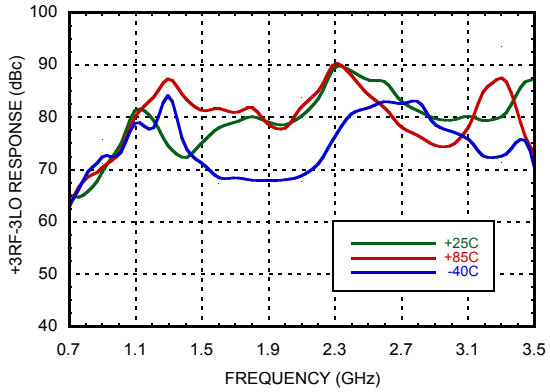
Input IP3 vs. Temperature @ VGATE=4.9V



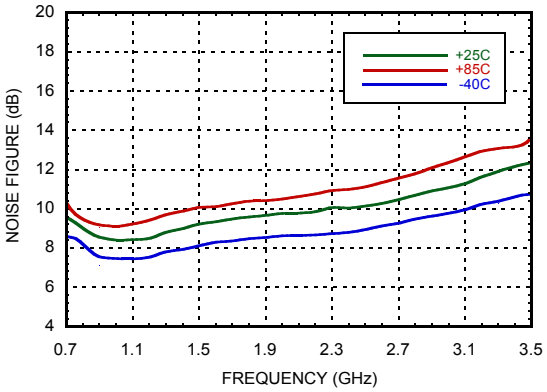
+2RF -2LO Response vs. Temperature @ VGATE=4.9V



+3RF -3LO Response vs. Temperature @ VGATE=4.9V



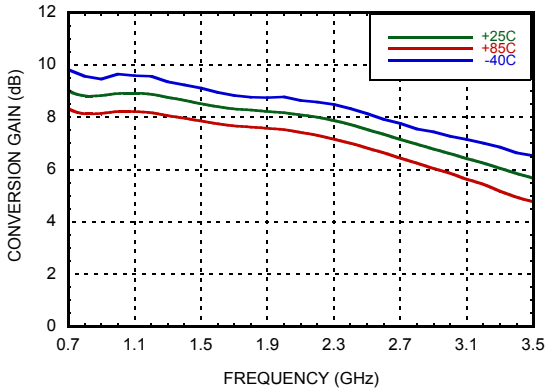
Noise Figure vs. Temperature @ VGATE=4.9V



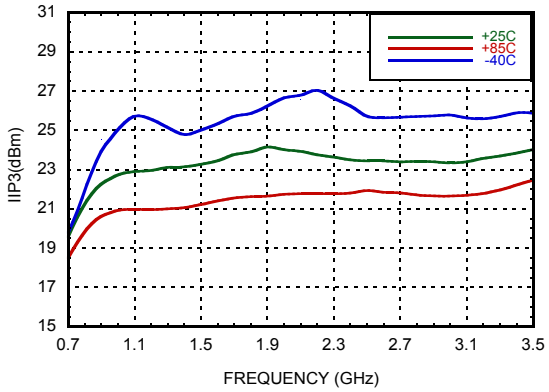
[1] Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

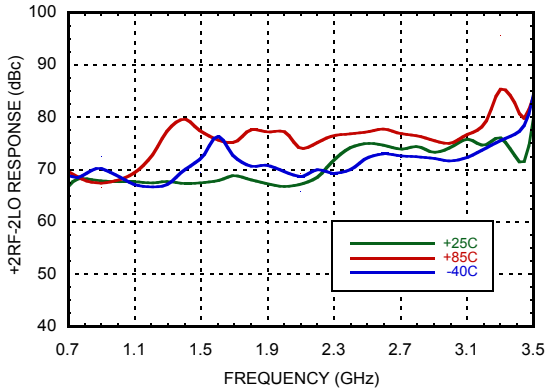
Conversion Gain vs. Temperature @ VGATE=4.8V [1]



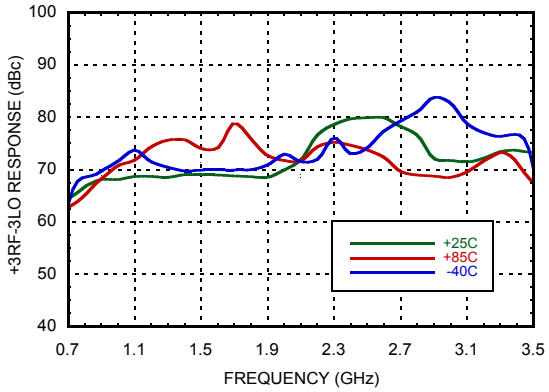
Input IP3 vs. Temperature @ VGATE=4.8V



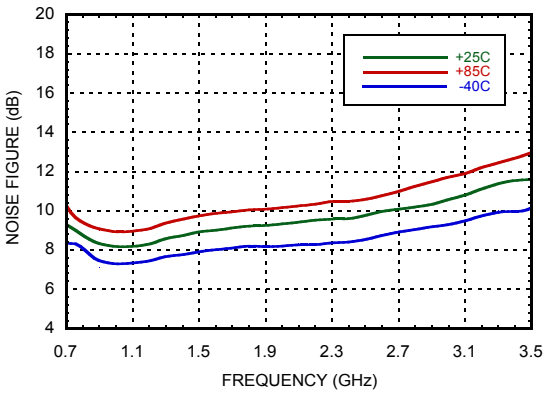
+2RF -2LO Response vs. Temperature @ VGATE=4.8V



+3RF -3LO Response vs. Temperature @ VGATE=4.8V



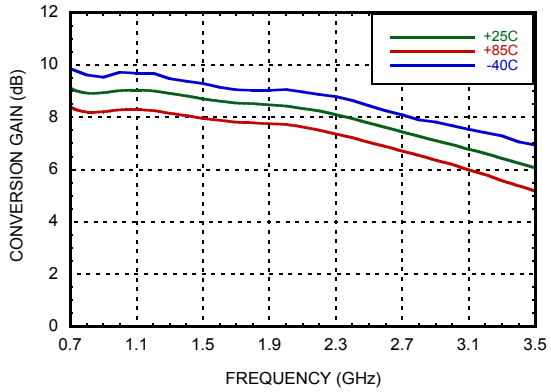
Noise Figure vs. Temperature @ VGATE=4.8V



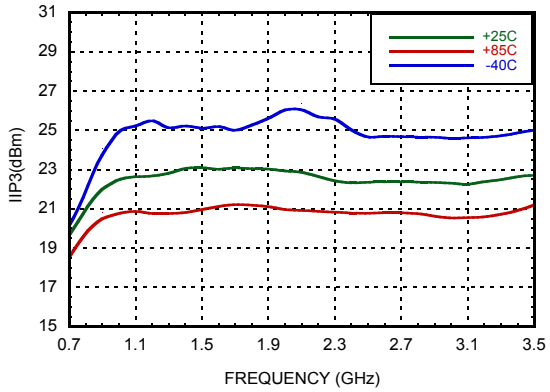
[1] Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

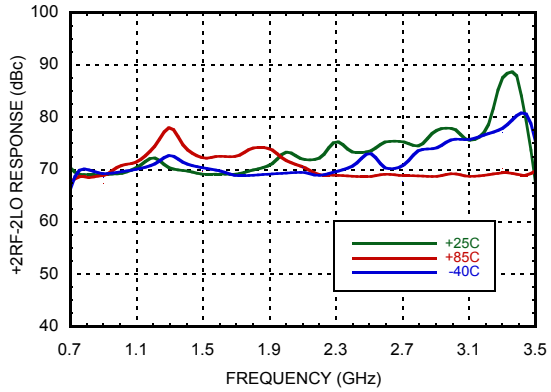
Conversion Gain vs. Temperature @ VGATE=4.7V [1]



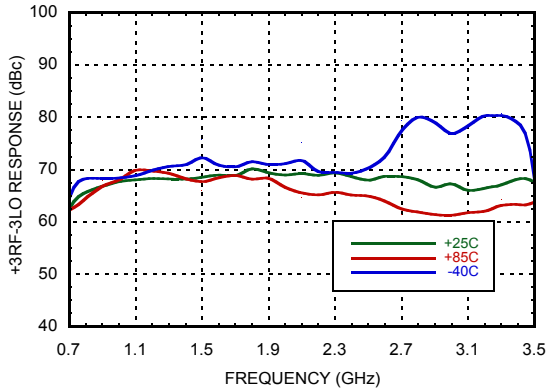
Input IP3 vs. Temperature @ VGATE=4.7V



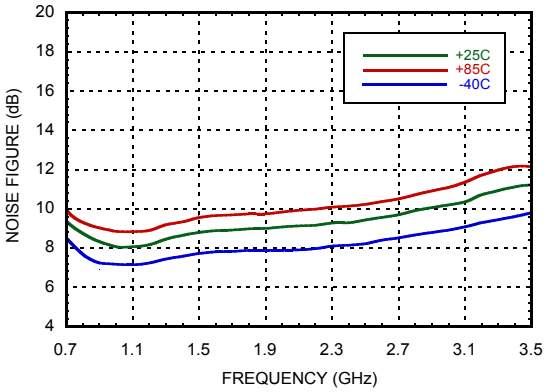
+2RF -2LO Response vs. Temperature @ VGATE=4.7V



+3RF -3LO Response vs. Temperature @ VGATE=4.7V

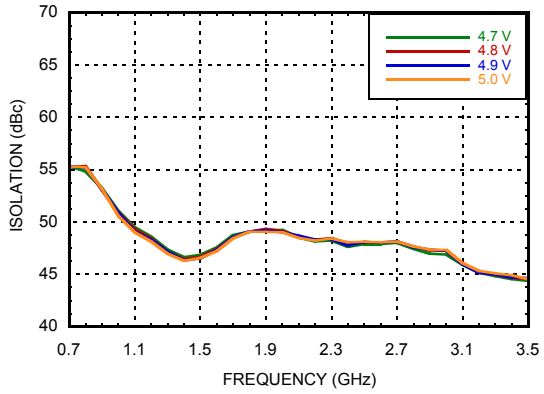


Noise Figure vs. Temperature @ VGATE=4.7V

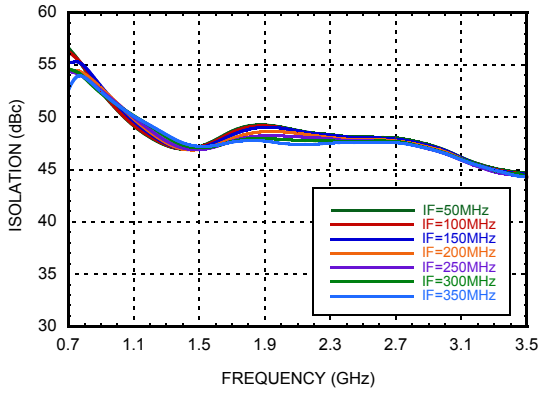


[1] Balun losses at IF output ports are de-embedded.

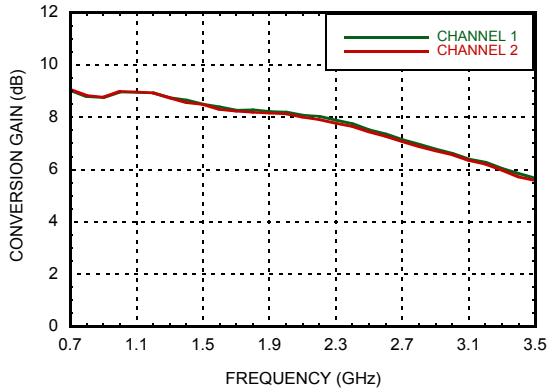
Channel to Channel Isolation vs. VGATE



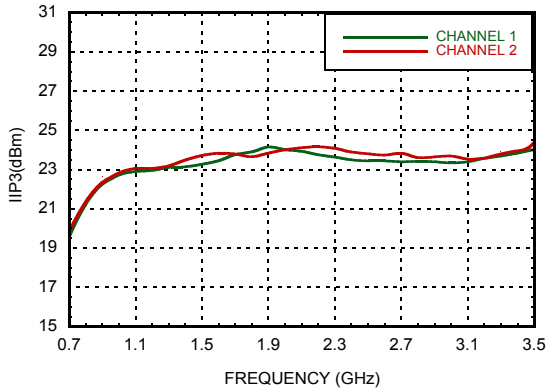
Channel to Channel Isolation vs. IF Frequency



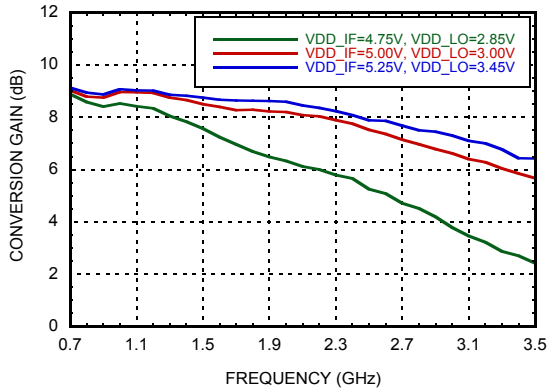
Conversion Gain, Channel Matching @ VGATE=4.8V [1]



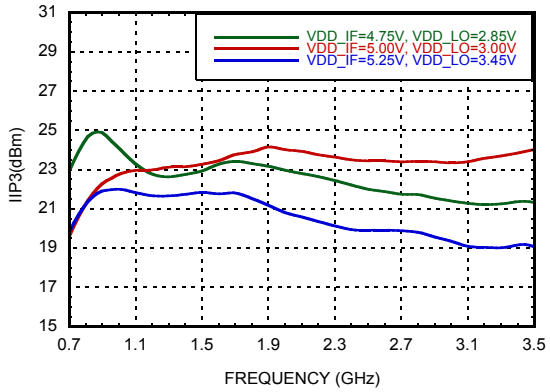
Input IP3, Channel Matching @ VGATE=4.8V



Conversion Gain vs. Vdd @ VGATE=4.8V [1]



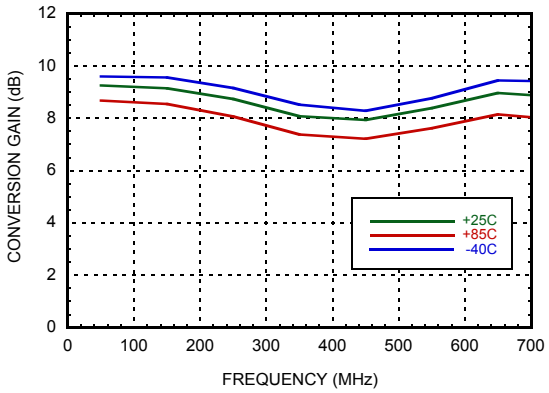
Input IP3 vs. Vdd @ VGATE=4.8V



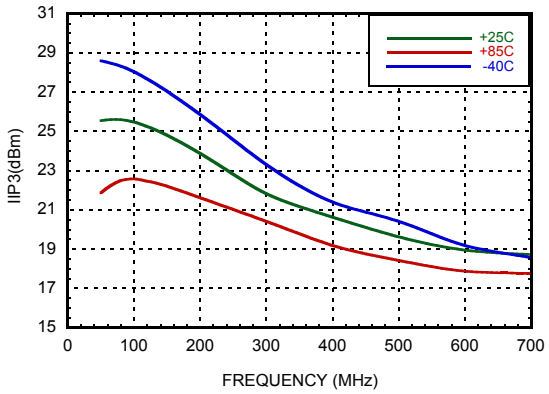
[1] Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

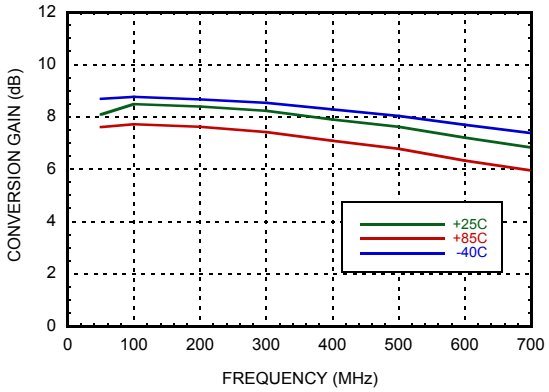
Conversion Gain vs. IF Frequency @ LO=850 MHz, VGATE=4.8V [1]



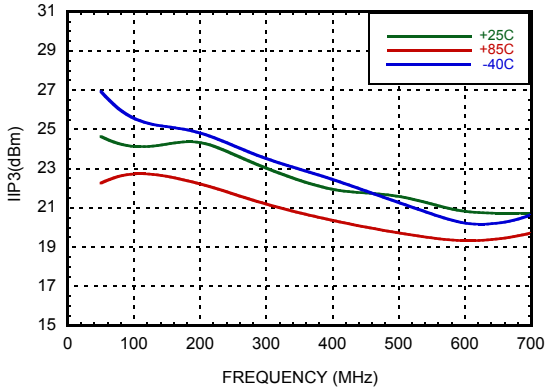
IIP3 vs. IF Frequency @ LO=850 MHz, VGATE=4.8V



Conversion Gain vs. IF Frequency @ LO=1800 MHz, VGATE=4.8V [1]



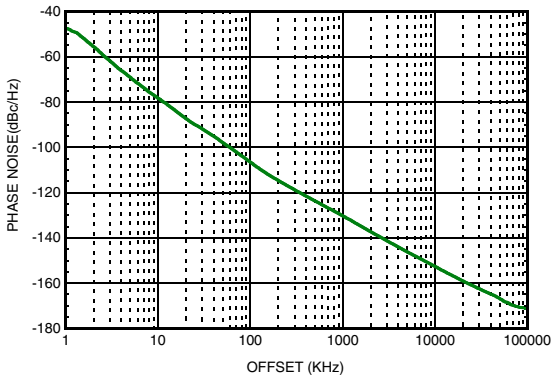
IIP3 vs. IF Frequency @ LO=1800 MHz, VGATE=4.8V



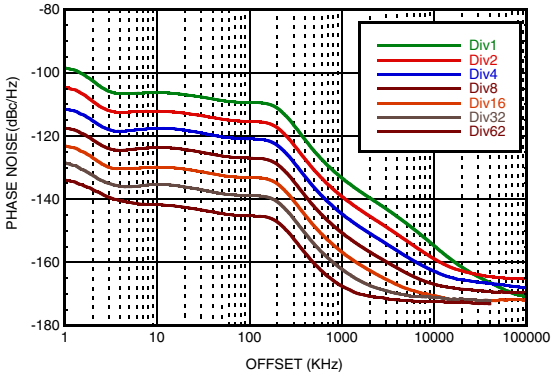
[1] Balun losses at IF output ports are de-embedded.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

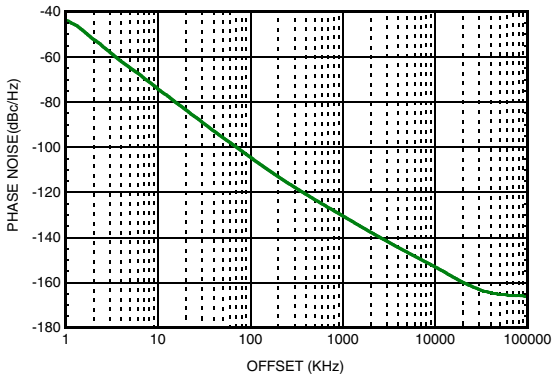
Auxiliary LO Output, Open Loop Phase Noise @ 3600 MHz



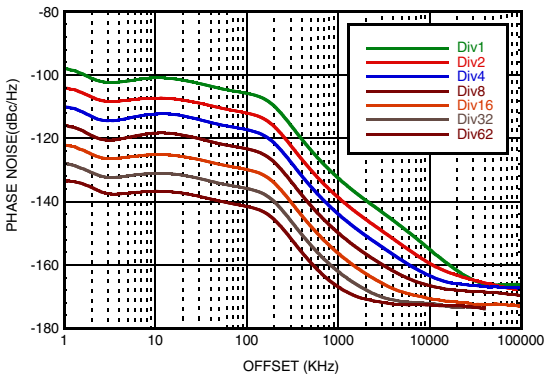
Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @3600 MHz with various divider ratios[1]



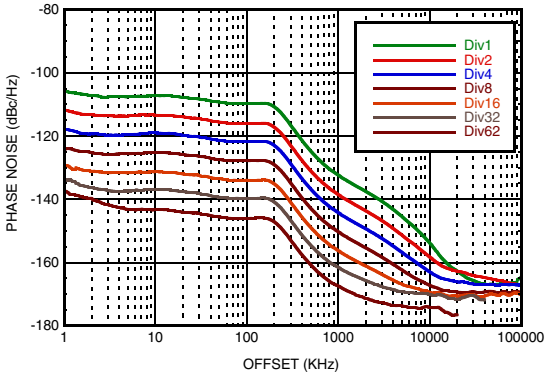
Auxiliary LO Output, Open Loop Phase Noise @ 4100 MHz



Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @4100 MHz with various divider ratios[1]

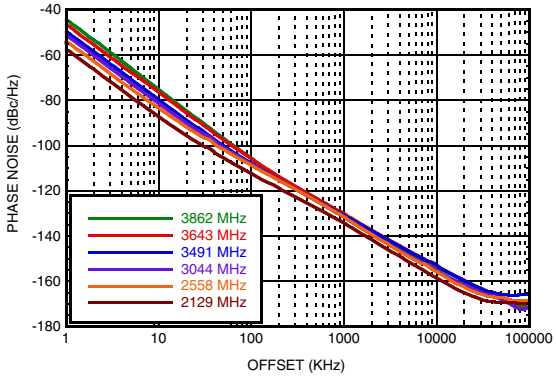


Auxiliary LO Output, Fractional Mode Closed Loop Phase Noise @ 3300 MHz with various divider ratios[2]

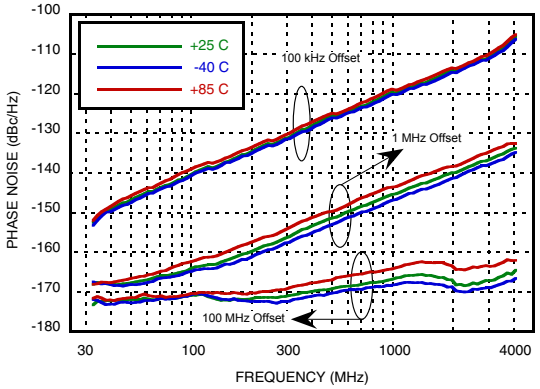


[1] Using 122.88 MHz clock input, 61.44 MHz PFD, 2.5 mA CP, 174 uA Leakage.
[2] Using 100 MHz clock input, 50MHz PFD, 2.5 mA CP, 174 uA Leakage.

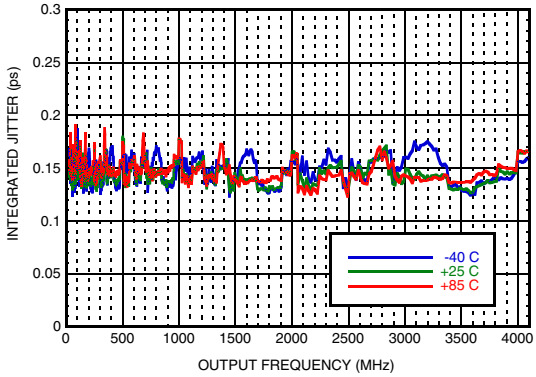
Auxiliary LO Output, Open Loop Phase Noise vs. Frequency



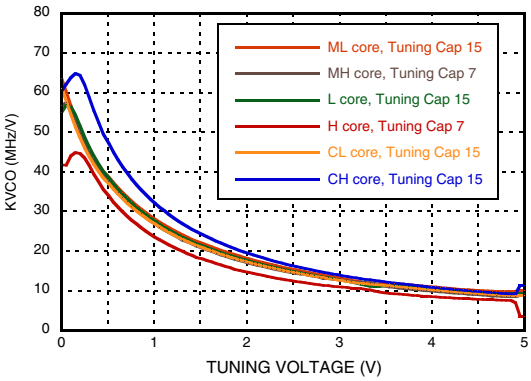
Auxiliary LO Output, Open Loop Phase Noise vs. Temperature



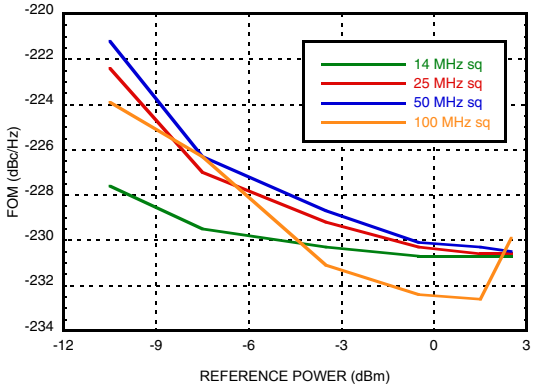
Integrated RMS Jitter [2]



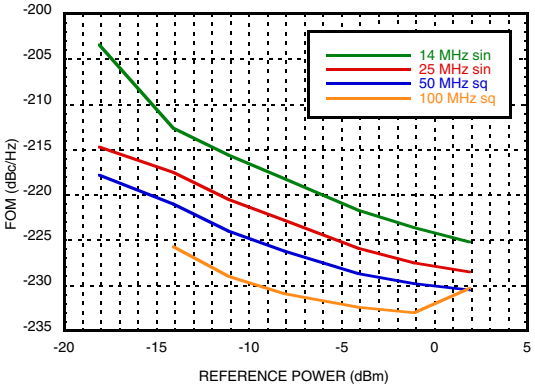
Typical VCO Sensitivity



Reference Input Sensitivity, Square Wave, 50 Ω [3]



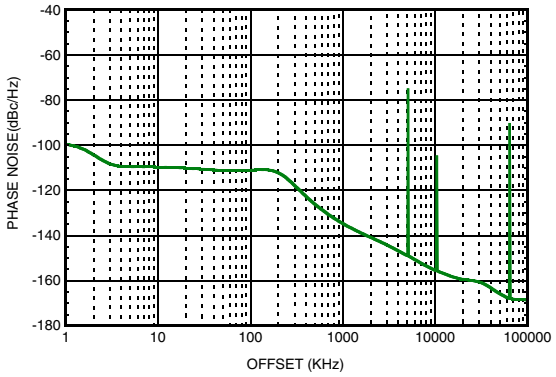
Reference Input Sensitivity, Sinusoid Wave, 50 Ω [3]



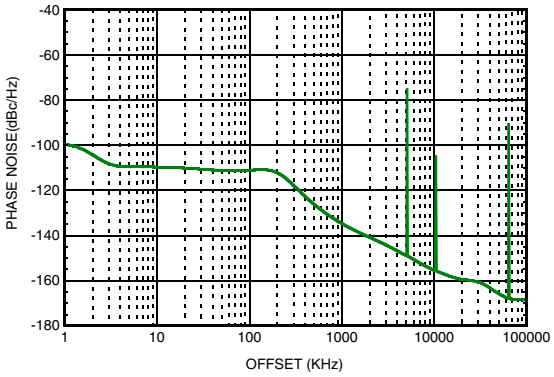
[1] Both LO and MIX Gain Set to '3', both LO and MIX Buffer Enabled, measured from Auxiliary LO Port.
[2] RMS Jitter data is measured in fractional mode using 50 MHz reference frequency, from 1 kHz to 100 MHz integration bandwidth.
[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. Full FOM performance up to maximum 3.3 Vpp input voltage.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

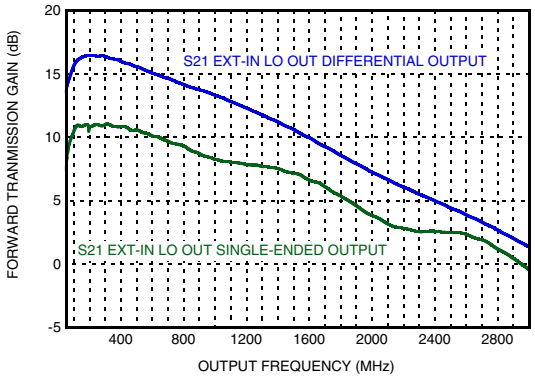
Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode ON [1]



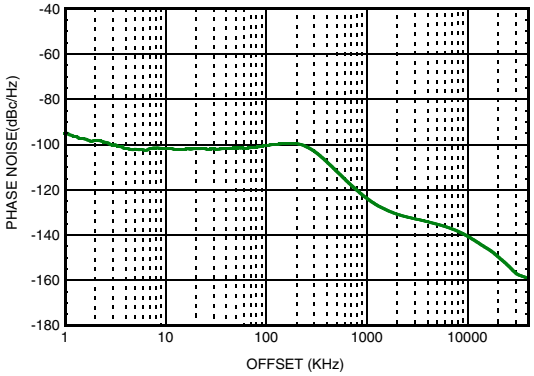
Fractional-N Spurious Performance @ 2646.96 MHz Exact Frequency Mode OFF [1]



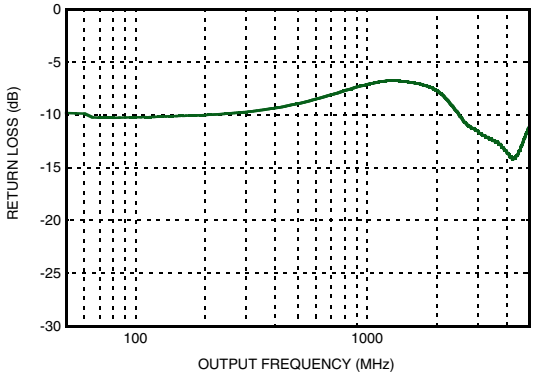
Forward Transmission Gain [2]



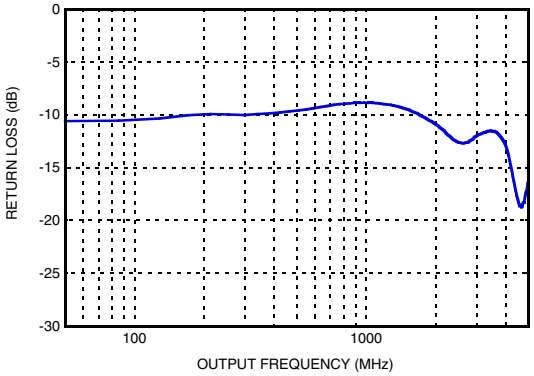
Closed Loop Phase Noise With External VCO HMC384LP4E @ 2200 MHz



Auxiliary LO Differential Output Return Loss

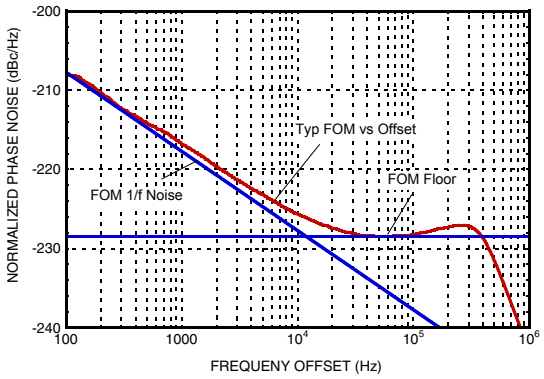


Auxiliary LO Single Ended Output Return Loss

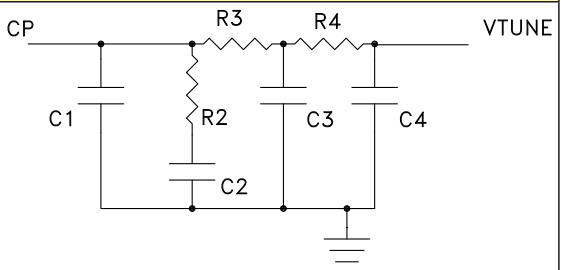


[1] 122.88 MHz clock input, PFD = 61.44 MHz, Channel Spacing = 240 KHz.
[2] S21 from Ext_VCO (pin 35, 36) in and LO (pin26, 27) out.

Figure of Merit for PLL/VCO



Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
156	180	6.8	47	47	2.2	1	1	

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
0.7	-65	-45	-67	-63
1.1	-80	-55	-64	-67
1.5	-59	-58	-65	-62
1.9	-59	-54	-72	-64
2.3	-60	-59	-73	-63
2.7	-59	-58	-82	-55
3.1	-60	-58	-77	-48
3.5	-53	-63	-73	-48

LO = Max. level
All values in dBm measured at RF port.

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-44	-52	-52	-55
1	-49	0	-44	-17	-52
2	-87	-45	-72	-50	-80
3	-88	-62	-88	-71	-87
4	-85	-85	-88	-88	-87

RF Freq. = 0.9 GHz @-5 dBm
LO Freq. = 0.8 GHz @ Max. level
All values in dBc below IF power level (1RF - 1LO).

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xxx	-44	-49	-64	-49
1	-54	0	-43	-28	-65
2	-83	-49	-76	-57	-84
3	-87	-72	-86	-88	-85
4	-83	-83	-85	-85	-87

RF Freq. = 1.9 GHz @-5 dBm
LO Freq. = 1.8 GHz @ Max. level
All values in dBc below IF power level (1RF - 1LO).

MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xxx	-44	-47	-65	-53
1	-58	0	-46	-40	-68
2	-80	-60	-75	-67	-85
3	-82	-82	-86	-83	-85
4	-84	-82	-85	-85	-87

RF Freq. = 2.5 GHz @-5 dBm
LO Freq. = 2.4 GHz @Max. level
All values in dBc below IF power level (1RF - 1LO).

Truth Table [1]

CHIPEN (V)	PLL/VCO
LOW	OFF
HIGH	ON

[1] IF and LO amplifiers can be disabled through SPI bus. See `Enabling/Disabling Mixer Features` application section.

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Absolute Maximum Ratings

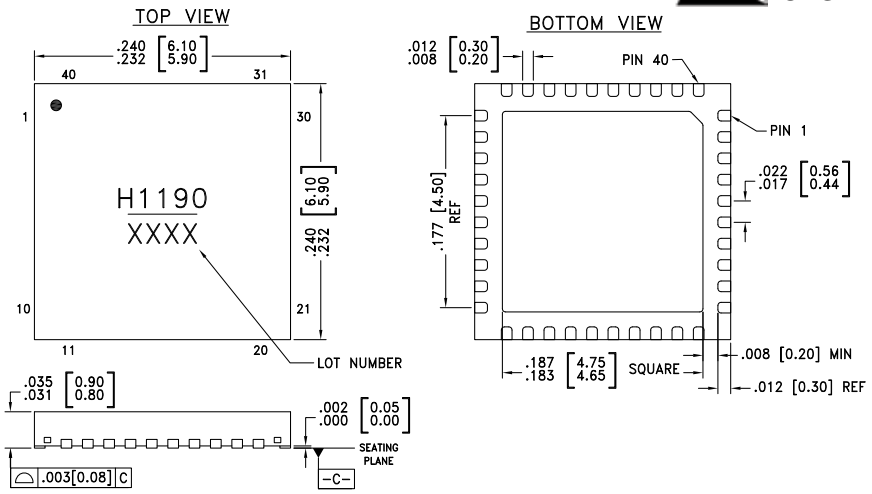
RF Input Power (VBIASIF1,2= +5V, LOVDD=3.0V)	+20 dBm
VBIASIF1,2, LOVDD	6V
VGATE1,2, VDDCP, VCS1, VCS2, LOVDD	-0.3V to +5.5V
3VRVDD, DVDD3V	-0.3V to +3.6V
Max. Channel Temperature	150°C
Thermal Resistance (channel to ground paddle)	3.3°C/W
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to +85°C
ESD Sensitivity (HBM)	Class 1B

Recommended Operating Conditions

VDDCP, VCS1, VCS2, VBIASIF1, VBIASIF2,LOBIAS1,LOBIAS2,VCC1,VCC2,VGATE1,VGATE2,VDDLS	5.0 V
LOVDD, 3VRVDD, DVDD3V, VCCPD, VCCPS, VCCHF	+3.3 V
Operating Temperature	-40 to +85°C

Outline Drawing

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking
HMC1190LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H1190 XXX

[1] Max peak reflow temperature of 260°C

[2] 4-Digit lot number XXXX

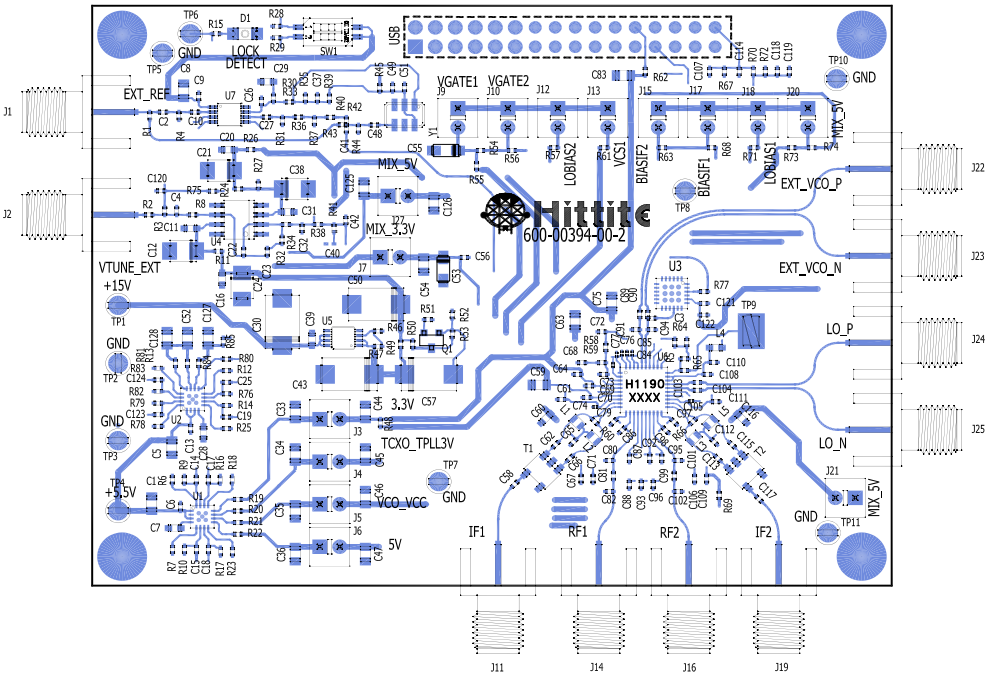
BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Pin Descriptions

Pin Number	Function	Description
1	VDDCP	Power Supply for charge pump analog section.
2	BIAS	External bypass decoupling for precision bias circuits.
3,4	CP1,CP2	Charge Pump Outputs.
5	3VRVDD	Reference supply, 3.3 V nominal.
6	XREFP	Reference Input. DC bias is generated internally. Normally AC coupled externally.
7	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry, 3.3 V nominal.
8,23	VCS1, VCS2	Bias control pins for IF amplifiers. Connect to 5V supply through 590 Ohms resistors. Refer to application section for proper values of resistors to adjust IF amplifier current.
9,10,21,22	IF1_N, IF1_P, IF2_P, IF1_N	Differential IF outputs. Connect to 5V supply through choke inductors. See application circuit.
11, 20	VBIASIF1, VBIASIF2	Supply voltage pin for IF amplifier's bias circuits. Connect to 5V supply through filtering.
12, 19	VGATE1, VGAET2	Bias pins for mixer cores. Set from 4.7V to 5.0V for operating frequency band.
13, 18	RF1, RF2	RF input pins of the mixer, internally matched to 50 Ohms. RF input pins require off chip DC blocking capacitors. See application circuit.
14, 17	LO_BIAS2, LO_BIAS1	Bias control pins for LO Amplifiers. Connect to 5V supply through 270 Ohms resistors. Refer to application section for proper values of resistors to adjust LO amplifier current.
15,24	RSV	Reserved for internal use.Should be left floating.
16	LOVDD	3V bias supply for LO Drive stages. Refer to application circuit for appropriate filtering and bias generation information.
25	CHIP_EN	Chip Enable. Connect to logic high for normal operation.
26	LON	Negative LO output used for single-ended, differential, or dual output mode.
27	LOP	Positive LO output used for differential or dual outputs only. While it can drive a separate load from LO_N, it cannot be used when LO_N is disabled.
28	VCC1	VCO Analog supply1, 5.0V nominal.
29	VCC2	VCO Analog Supply 2, 5.0V nominal.
30	VTUNE	VCO Varactor. Tuning Port Input.
31	SEN	PLL Serial Port Enable (CMOS) Logic Input.
32	SDI	PLL Serial Port Data (CMOS) Logic Input.
33	SCK	PLL Serial Port Clock (CMOS) Logic Input.
34	LD/SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO).
35	EXT_VC0_N	External VCO negative input
36	EXT_VCO_P	External VCO positive input.
37	VCCHF	Analog supply, 3.3 V nominal
38	VCCPS	Analog supply, Prescaler, 3.3 V nominal
39	VCCPD	Analog supply, Phase Detector, 3.3 V nominal
40	VDDLS	Analog supply, Charge Pump, 5.0 V nominal

BROADBAND HIGH IP3 DUAL CHANNEL DOWNCONVERTER w/ Fractional-N PLL & VCO, 0.7 - 3.5 GHz

Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC1190LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1190LP6GE Evaluation PCB	EVAL01-HMC1190LP6G
Evaluation Kit	HMC1190LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1190LP6G

REGISTER MAP

Table 1. Reg 00h ID Register (Read Only) DEFAULT C7701A h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	RO	Chip ID	24	C7701A	Chip ID Number

Table 2. Reg 00h Read Address Register (Write Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[4:0]	WO	Read Address	5	-	(WRITE ONLY) Specifies the address to be read in the next read cycle.
[5]	WO	Soft Reset	1	-	(WRITE ONLY) Soft Reset - (set to 0 during operation)
[23:6]	WO	Not Defined	18	-	Not defined, set to 0h.

Table 3. Reg 01h Chip Enable Register DEFAULT 3h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	Chip Enable Pin Select	1	1	1 = Chip enable via CHIP_EN pin, Reg 01h[0]=1 and CHIP_EN pin low places the PLL in Power Down Mode 0 = Chip enable via SPI - Reg 01h[0] = 0, CHIP_EN pin ignored (see Power Down Mode description for more details)
[1]	R/W	SPI Chip Enable	1	1	Controls Chip Enable (Power Down) if Reg 01h[0] =0 Reg 01h[0]=0 and Reg 01h[1]=1 - chip is enabled, CHIP_EN pin don't care Reg 01h[0]=0 and Reg 01h[1]=0 - chip disabled, CHIP_EN pin don't care (see Power Down Mode description for more information)
[2]	R/W	Keep Bias On	1	0	1: keeps internal bias generators on, ignores chip enable control 0: bias generators controlled automatically via chip enable control
[3]	R/W	Keep PFD Pn	1	0	1: keeps PFD circuit on, ignores chip enable control 0: PFD circuit controlled by chip enable control
[4]	R/W	Keep CP On	1	0	1: keeps Charge Pump on, ignores chip enable control 0: Charge Pump automatically controlled by chip enable control
[5]	R/W	Keep Reference Buffer ON	1	0	1: keeps reference buffer block on, ignores Chip enable control 0: reference buffer block automatically controlled by chip enable control
[6]	R/W	Keep VCO on	1	0	1: keeps VCO divider buffer on, ignores chip enable control 0: VCO divider buffer automatically controlled via chip enable control
[7]	R/W	Keep GPO Driver ON	1	0	1: keeps GPO output Driver ON, ignores Chip enable control 0: GPO output driver automatically controlled by chip enable control
[9:8]	R/W	reserved	2	0	reserved

Table 4. Reg 02h Reference Divider Register DEFAULT 1h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[13:0]	R/W	R Divider Setting	14	1	Reference Divider 'R' Value (EQ 8) min: 1d max: 16383d

Table 5. Reg 03h Frequency Register - Integer Part DEFAULT 9h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[18:0]	R/W	Integer Setting	19	25d 19h	Divider Integer part, used in all modes, see (EQ 10) Fractional Mode min 20d max 2^{19} -4 = 7FFFCh = 524,284d Integer Mode min 16d max 2^{19}-1 = 7FFFFh = 524,287d

Table 6. Reg 04h Frequency Register - Fractional Part DEFAULT 0h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	Fractional Setting	24	0	Divider Fractional part (24 bit unsigned) see Fractional Frequency Tuning Fractional Division Value = Reg4[23:0]/2^24 Used in Fractional Mode only min 0d max 2^24-1 = FFFFFFh = 16,777,215d

Table 7. Reg 05h Reserved

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	Reserved	24	0	Reserved

Table 8. Reg 06h Delta Sigma Modulator Register DEFAULT 30F0Ah

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[1:0]	R/W	Reserved	2	2d	Reserved, Program to 0h
[3:2]	R/W	DSM Order	2	2d	Select the Delta Sigma Modulator Type 0: 1st order 1: 2nd Order 2: 3rd Order - Recommended 3: Reserved
[4]	R/W	Synchronous SPI Mode	1	0	0: Normal SPI Load - all register load on rising edge of SEN 1: Synchronous SPI - registers Reg 03h, Reg 04h , Reg 1Ah wait to load synchronously on the next internal clock cycle. Normally (When this bit is 0) SPI writes into the internal state machines/counters happen asynchronously relative to the internal clocks. This can create freq/phase disturbances if writing register 3, 4 or 1A. When this bit is enabled, the internal SPI registers are loaded synchronously with the internal clock. This means that the data in the SPI shifter should be held constant for at least 2 PFD clock periods after SEN is asserted to allow this retiming to happen cleanly.
[5]	R/W	Exact Frequency Mode Enable	1	0	1: Exact Frequency Mode Enabled 0: Exact Frequency Mode Disabled
[6]	R/W	Reserved	1	0	Reserved
[7]	R/W	Fractional Bypass	1	0	0: Use Modulator, Required for Fractional Mode, 1: Bypass Modulator, Required for Integer Mode Note: When enabled fractional modulator output is ignored, but fractional modulator continues to be clocked if Reg 06h[11] =1. This feature can be used to test the isolation of the digital fractional modulator from the VCO output in integer mode.
[8]	R/W	Autoseed EN	1	1	1: loads the modulator seed (start phase) whenever the fractional register (Reg 04h) is written 0: when fractional register (Reg 04h) write changes frequency, modulator starts at previous value (phase)
[10:9]	R/W	Reserved	2	3d	Reserved
[11]	R/W	Delta Sigma Modulator Enable	1	1	0: Disable DSM, used for Integer Mode 1: Enable DSM Core, required for Fractional Mode
[22:12]	R/W	Reserved	11	30h	Reserved

Table 9. Reg 07h Lock Detect Configuration Register DEFAULT 200844 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	R/W	Lock Detect Window Count Max	3	4d	Lock Detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65535
[14:3]	R/W	Reserved	11	108h	Reserved
[15]	R/W	CSP Enable	1	0	Cycle Slip Prevention Enable 1: Enables Cycle Slip Prevention. Cycle Slip Prevention decreases the amount of time required for the PLL to converge (lock) to the new frequency during large frequency changes. 0: Cycle Slip Prevention Disabled. The PLL will still lock, but may take longer time to achieve lock.
[19:16]	R/W	Reserved	4	0	Reserved
[20]	R/W	Lock Detect Training	1	0	0 to 1 transition triggers the training. Lock Detect Training is only required after changing Phase Detector frequency. After changing PD frequency a toggle Reg 07h[20] from 0 to 1 retrains the Lock Detect.
[21]	R/W	Reserved	1	0	Reserved

Table 10. Reg 08h Analog Enable Register DEFAULT 1BFFF h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[20:0]	R/W	Reserved	21	114687d 1BFFFh	Reserved
[21]	R/W	Hi Frequency Reference	1	0	Program 1 for XTAL > 200 MHz (sets low gain mode for high frequency crystal buffer), 0 otherwise.
[22]	R/W	SDO Output Level	1	0	Output Logic Level on LD/SDO pin 0: 1.8 V Logic Levels 1: DVDD3V Logic Level
[23]	R/W	Reserved	1	0	Reserved

Table 11. Reg 09h Charge Pump Register Default 527264 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[6:0]	R/W	CP DN Gain	7	100d 64h	Charge Pump DN Gain Control 20uA/step Affects fractional phase noise and lock detect settings 0d = 0uA 1d = 20uA 2d = 40uA ... 127d = 2.54mA Default 2mA
[13:7]	R/W	CP UP Gain	7	100d 64h	Charge Pump UP Gain Control 20uA/step Affects fractional phase noise and lock detect settings 0d = 0uA 1d = 20uA 2d = 40uA ... 127d = 2.54mA Default 2mA
[20:14]	R/W	Offset Current	7	49h	Charge Pump Offset Control 5uA/step Affects fractional phase noise and spur sand lock detect settings 0d = 0uA 1d = 5uA 2d = 10uA ... 127d = 635uA Default 405uA
[21]	R/W	Offset Current UP	1	0	1 - Sets Direction of Reg 09h[20:14] Up, 0- UP Offset Off
[22]	R/W	Offset Current DN	1	1	1 - Sets Direction of Reg 09h[20:14] Down, 0- DN Offset Off
[23]	R/W	HiK charge pump Mode	1	0	Hi Kcp Charge Pump - Very Low Noise, Narrow Compliance range, requires external OpAmp in the loop filter.

Table 12. Reg 0Ah VCO AutoCal Configuration Register Default 2046 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[2:0]	R/W	Vtune Resolution	3	6d	1,2,4,8,...,32,64,128,256 Rdiv cycles for frequency measurement. Measurement should last > 4 µsec. Note: 1 does not work if R divider = 1.
[10:3]	R/W	Reserved	8	8d	Reserved
[11]	R/W	AutoTune Disable	1	0	1 - Disable AutoTune procedure
[12]	R/W	Reserved	1	0	Reserved
[14:13]	R/W	FSM Clock Select	2	1	Set the AutoCal FSM (50 MHz maximum) 0: Input Crystal Reference 1: Input Crystal Reference/4 2: Input Crystal Reference/16 3: Input Crystal Reference/32
[16:15]	R/W	Reserved	2	0	Reserved
[17]	R/W	Auto Relock - One Try	1	0	1: Attempts to relock if Lock Detect fails for any reason. Only tries once.

Table 13. Reg 0Bh PD/CP Register Default 78061 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[3:0]	R/W	Reserved	4	1	Reserved
[4]	R/W	PD Phase Select	1	0	Inverts the PD polarity (program to 0) 0- Use with a positive tuning slope VCO and Passive Loop Filter (default) 1- Use with a Negative Slope VCO or with an inverting Active Loop Filter with a Positive Slope VCO
[5]	R/W	PD Up Output Enable	1	1	Enables the PD UP output, see also Reg 0Bh Reg 7h[9]
[6]	R/W	PD Down Output Enable	1	1	Enables the PD DN output, see alsoReg 0Bh Reg 7h [10]
[8:7]	R/W	Reserved	2	0	Reserved, .
[9]	R/W	Force CP UP	1	0	Forces CP UP output on if CP is not forced down - Use for Test only
[10]	R/W	Force CP DN	1	0	Forces CP DN output on if CP is not forced up - Use for Test only
[11]	R/W	Force CP MId Rail	1	0	Force CP MId Rail - Use for Test only (if Force CP UP or Force CP DN are enabled they have precedence)
[23:12]	R/W	Reserved	12	78h	Reserved.

Table 14. Reg 0Ch Exact Frequency Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	Number of Channels per Fpd	24	0	Comparison Frequency divided by the correction rate. Must be an integer. Frequencies at exactly the correction rate will have zero frequency error (Exact Frequency Mode). Only works in modulator Mode B (3rd order modulator type (Reg 06h[3:2] = 2h)). Reg 0Ch must be 0 if using other DSM types ie. if Reg 06h[3:2] ≠ 2h. 0: Disabled 1: Invalid ≥ 2 valid max: 2^{24}-1 = FFFFFFh = 16,777,215d

Table 15. Reg 0Fh GPO Register

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[4:0]	R/W	GPO	5	1	Select signal to be output to SDO pin when enabled DEFAULT LOCK DETECT 0: Data from Reg0F[5] 1: Lock Detect Output 2. Lock Detect Trigger 3: Lock Detect Window Output 4: Ring Osc Test 5. Pullup Hard from CSP 6. PullDN hard from CSP 7. Reserved 8: Reference Buffer Output 9: Ref Divider Output 10: VCO divider Output 11. Modulator Clock from VCO divider 12. Auxiliary Clock 13. Aux SPI Clock 14. Aux SPI Enable 15. Aux SPI Data Out 16. PD DN 17. PD UP 18. SD3 Clock Delay 19. SD3 Core Clock 20. AutoStrobe Integer Write 21. Autostrobe Frac Write 22. Autostrobe Aux SPI 23. SPI Latch Enable 24. VCO Divider Sync Reset 25. Seed Load Strobe 26.-29 Not Used 30. SPI Output Buffer En 31. Soft RSTB
[5]	R/W	GPO Test Data	1	0	1 - GPO Test Data when GPO_Select = 0
[6]	R/W	Prevent Automux SDO	1	0	1- Outputs GPO data only 0- Automuxes between SDO and GPO data
[7]	R/W	LDO Driver Always On	1	0	Only for HMC SPI mode 1- LD_SDO Pin driver always on 0- LD_SDO Pin driver only on during SPI read cycle
[9:8]	R/W	Reserved	1	0	Reserved

Table 16. Reg 10h Tuning Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[7:0]	R	VCO Tune Curve	8	80h	VCO sub-band selection. 0- maximum frequency '1111 1111'b- minimum frequency
[8]	R	VCO Tuning Busy	1	0	Indicates if the VCO tuning is in process 1- Busy 0- Not Busy

Table 17. Reg 11h SAR Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[18:0]	R	SAR Error Magnitude Count	19	2^{19}- 1d 7FFFFh	SAR Error Magnitude Count
[19]	R	SAR Error Sign	1	0	SAR Error Sign 0: positive 1: negative

Table 18. Reg 12h GPO/LD Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R	GPO Out	1	0	GPO Output
[1]	R	Lock Detect Out	1	0	Lock Detect Output
[4:2]	R	Reserved	3	7h	Reserved

Table 19. Reg 13h BIST Register (Read Only)

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[16:0]	R	Reserved	16	4697d 1259h	Reserved

Table 20. Reg 14h Auxiliary SPI Register Default

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	Aux SPI Mode	1	0	1- Use the 3 outputs as an SPI port 0- Use the 3 outputs as a static GPO port
[3:1]	R/W	Aux GPO Values	3	0	Output values when Reg 07h[1] = 1
[4]	R/W	Aux GPO 3.3 V	1	0	0- 1.8 V output out of the Auxiliary GPO pins when Reg 10h[1] = 1 1- 3.3 V output out of the Auxiliary GPO pins when [1] = 1
[8:5]	R/W	Reserved	4	1	Reserved
[9]	R/W	Phase Sync	1	1	When set, CHIP_EN pin is used as a trigger for phase synchronization. Can be used to synchronize multiple HMC1190LP6GE, or to along with the Reg 20h value to phase step the output. (Exact Frequency Mode must be enabled)
[11:10]	R/W	Aux SPI GPO Output	2	0	Option to send GPO multiplexed data (ex Lock Detect) to one of the auxiliary outputs 0- None 1 - to [0] 2 - to [1] 3 - to [2]
[13:12]	R/W	Aux SPI Outputs	2	0	When disabled: 0 - Outputs Hi Z 2 - Outputs stay driven 3 - Outputs driven to high 4 - Outputs driven to low

Table 21. Reg 15h Manual VCO Config Register Default F48AD h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	Manual Calibration Mode	1	0	1- VCO subsystem manual calibration enabled 0- VCO subsystem manual calibration disabled
[5:1]	R/W	Capacitor Switch Setting	5	16d 10h	capacitor switch setting
[8:6]	R/W	Manual VCO Selection	3	2d	Manual VCO Selection
[9]	R/W	Manual VCO Tune Enable	1	0	1- Manual VCO tuning enabled 0- Manual VCO tuning disabled
[15:10]	R/W	Reserved	6	18d 12h	Reserved
[16]	R/W	Enable Auto-Scale CP current	1	1	1 - Automatically scale CP current based on VCO frequency and capacitor setting 0- Don't scale CP current
[19:17]	R/W	Reserved	3	7d	Reserved

Table 22. Reg 16h Gain Divider Register Register Default 6C1 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[5:0]	R/W	RF Divide Ratio	6	1d	0 - Mute, VCO and PLL buffer On, RF output stages Off 1 - Fo 2 - Fo/2 3 - invalid, defaults to 2 4 - Fo/2 5 - invalid, defaults to 4 6 - Fo/6 ... 60 - Fo/60 61 - invalid, defaults to 60 62 - Fo/62 > 62 - invalid, defaults to 62
[7:6]	R/W	LO Output Buffer Gain Control	2	3d	3 - Max Gain 2 - Max Gain - 3 dB 1 - Max Gain - 6 dB 0 - Max Gain - 9 dB
[9:8]	R/W	LO2 Output Buffer gain Control	2	2d	3 - Max Gain 2 - Max Gain - 3 dB 1 - Max Gain - 6 dB 0 - Max Gain - 9 dB
[10]	R/W	Divider Output Stage Gain Control	1	1	1 - Max Gain 0 - Max Gain - 3 dB

Table 23. Reg 17h Modes Register Register Default 1A8 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[0]	R/W	VCO SubSys Master Enable	1	1	Master enable for the entire VCO Subsystem 1 - Enable 0 - Disable Chip Enable is also required.
[1]	R/W	VCO Enable	1	1	1: Internal VCO Enable 0: Internal VCO Disable
[2]	R/W	External VCO Buffer Enable	1	0	External VCO Buffer to output stage enable. Only used when locking an external VCO.
[3]	R/W	PLL Buffer Enable	1	1	PLL Buffer Enable. Used when using an internal VCO.
[4]	R/W	LO Output Buffer Enable	1	0	Enables LO (LO_P & LO_N pins) output buffer.
[5]	R/W	LO2 Output Buffer Enable	1	1	Enables the second (LO2_N & LO2_P pins) output buffer
[6]	R/W	External Input Enable	1	0	Enables External VCO input
[7]	R/W	Pre Lock Mute Enable	1	1	Mute both output buffers until the PLL is locked
[8]	R/W	LO Output Single-Ended Enable	1	1	Enables Single-Ended output mode for LO output 1- Single-ended mode, LO_N pin is enabled, and LO_P pin is disabled 0- Differential mode, both LO_N and LO_P pins enabled Please note that single-ended output is only available on LO_N pin.
[9]	R/W	LO2 Output Single-Ended Enable	1	0	Enables Single-Ended output mode for LO2 output 1- Single-ended mode, LO2_N pin is enabled, and LO2_P pin is disabled 0- Differential mode, both LO2_N and LO2_P pins enabled Please note that single-ended output is only available on LO2_N pin.
[10]	R/W	Reserved	1	0	Reserved
[11]	R/W	Charge Pump Output Select	1	0	Connects CP to CP1 or CP2 output. 0: CP1 1: CP2

Table 24. Reg 18h Bias Register Register Default 54C1 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[18:0]	R/W	Reserved	19	54C1h	Reserved
[19]	R/W	External Input buffer BIAS bit0	1	0	External Input buffer BIAS bit0
[20]	R/W	External Input buffer BIAS bit1	1	0	External Input buffer BIAS bit1

Table 25. Reg 19h Cals Register Register Default 19 h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	Reserved	24	19h	

Table 26. Reg 1Ah Seed Register Register Default B29DOB h

BIT	TYPE	NAME	W	DEFLT	DESCRIPTION
[23:0]	R/W	Delta Sigma Modulator Seed	24	B29D0Bh	Used to program output phase relative to the reference signal. Phase = 2π(Reg 20h/2^{24}). To exactly program output phase operation in Exact Frequency Mode is required. When not using Exact Frequency Mode Reg 20h sets the start phase of output signal. If Reg 06h[8] = 1, Reg 20h sets the start phase of the signal after every frequency change.

Application Information

The HMC1190LP6GE is a broadband dual channel, high dynamic range, high gain, low noise, high-linearity down converting mixer with integrated Fractional-N Integer-N PLL and VCO, designed to cover RF frequencies from 700 MHz to 3.5 GHz. The HMC1190LP6GE`s low noise and high linearity performance makes it suitable for a wide range of transmission standards, including TDD, FDD, LTE, WiMAX, CDMA,GSM, MC-GSM, W-CDMA, UMTS, TD-SCDMA applications.

The HMC1190LP6GE offers an easy-to-use and complete frequency conversion solution for diversity and MIMO receiver applications in a highly compact 6x6 mm plastic QFN package. The HMC1190LP6GE greatly simplifies the design of diversity and MIMO receiver applications by increasing the integration level and reducing the number of required circuit elements thereby reducing cost, area, and power consumption.

Principle of Operation

HMC1190LP6GE's single-ended RF inputs are converted into differential through the on-chip integrated baluns. The single-ended RF inputs are internally broadband matched to 50 Ω and require only standard DC-blocking capacitors.

HMC1190LP6GE's RF inputs can be externally matched for narrow band application frequencies with a simple matching network including a series inductor, and a shunt capacitor to further improve the performance. Please refer to the application circuit for narrow band RF input matching for the detailed information.

The HMC1190LP6GE's IF amplifiers are designed for differential 200 Ω output load impedance. A few external components are required at these IF outputs for the broadband frequency response as recommended in the application circuit.

Refer to the IF output interface section for detailed information.

The HMC1190LP6GE requires 5V, 3.3V and 3V supply voltages and external bias voltages. Bias voltages generate reference currents for the IF and LO amplifiers. 3.3V supply voltage and the external bias voltages can be generated from 5V supply voltage to operate with a single supply. Please refer to the single supply operation section for more information.

The reference currents to the IF and LO amplifiers can be disabled through SPI interface. See `Enabling / Disabling Mixer Features` section for details.

Supply Number Reduction

The LOVDD, VCS1, VCS2, LOBIAS1, LOBIAS2, VGATE1 and VGATE2 pins of HMC1190LP6GE requires different supply voltages.

Except LOVDD, other pin voltages i.e. VGATE1, VGATE2, LOBIAS1, LOBIAS2, VCS1, VCS2 voltages are already generated from 5.5V supply voltage on evaluation board (see application circuit). These bias voltages can be optimized by external resistors (VCS1, VCS2, LOBIAS1, LOBIAS2, VGATE1, and VGATE2). The resistor values of VCS1, VCS2 on evaluation board are 590 Ohms. LOBIAS1 and LOBIAS2 series resistor values are 270 Ohms. Refer to the VCS Interface and LOBIAS Interface section for more information.

On the evaluation board, VGATE1, VGATE2 pin voltages are 5V; however VGATE1, VGATE2 pin voltages can be tuned between 4.7V and 5V for optimization of Input IP3 and conversion gain performances. After VGATE1,VGATE2 pin voltages are optimized, these pin voltages can be generated from 5V supply by changing the values of series resistors, R14 and R15. Refer to the VGATE interface section for more information.

The 3 V supply voltage for the LO amplifiers can be generated from 5 V or 3.3 V supply voltages by adding a series resistor (R_LOVDD) between LOVDD pin and supply voltage in the configuration shown in Figure 1.

- If using a 5 V supply R_LOVDD = 14 Ω, and minimum power rating of R_LOVDD is 0.3 W
- If using a 3.3 V supply, R_LOVDD = 2.15 Ω, and minimum power of R_LOVDD is 0.05 W

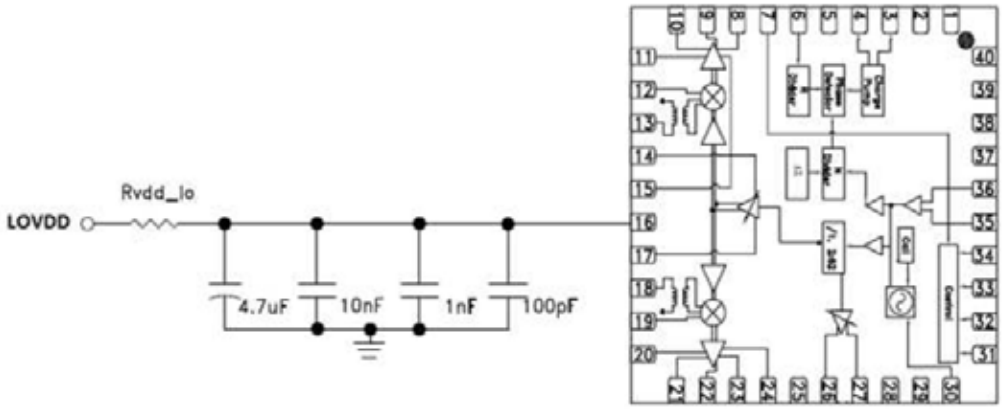
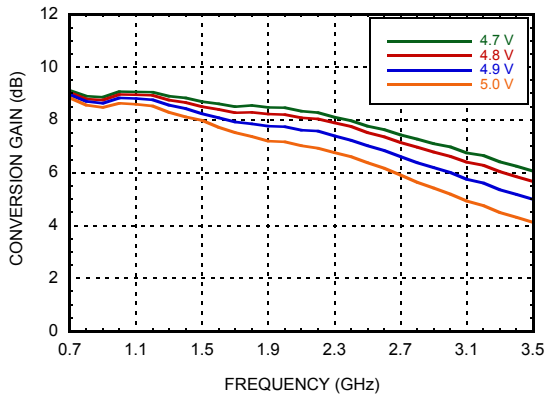


Figure 1. Interface to generate 3 V for LOVDD pin from 3.3V or 5V Supply.

VGATE Interface

The VGATE1, VGATE2 pins are bias pins for mixer cores. On evaluation board VGATE1, VGATE2 pin voltages are set to 5V. However voltage can be tuned between 4.7V and 5V for optimizing input IP3 and conversion gain performances for desired frequency band. Higher IIP3 values can be obtained by increasing the VGATE1, VGATE2 pin voltages but this will reduce HMC1190LP6GE`s conversion gain. Figure 4 shows the measured conversion gain and IIP3 for four values of VGATE1, VGATE2 pin voltages.

Conversion Gain vs. VGATE [1]



Input IP3 vs. VGATE

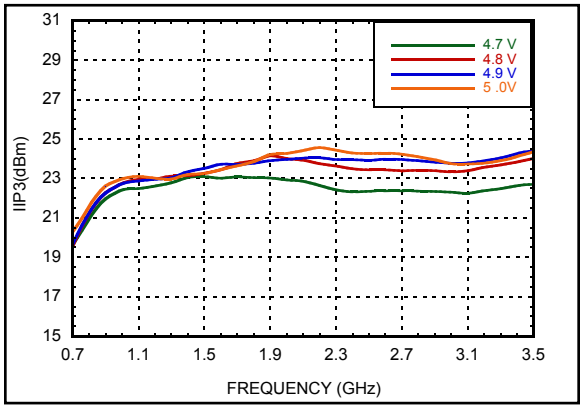


Figure 2. Conversion Gain & IIP3 vs. RF Frequency over VGATE Pin Voltage @25C, IF =150 MHz

After the VGATE voltage is tuned for optimized IIP3 and conversion gain performance, the VGATE pin voltage can be generated from 5V supply voltage by changing the value of series resistors, R54 and R56 from 0 Ohm to an appropriate value.

[1] Balun losses at IF output ports are de-embedded.

Table 1 shows the typical resistor values that need to be added in series with VGATE1, VGATE2 pins for different VGATE voltages.A fine tune for R54 and R56 resistors can be used if a better fit is required.

Table 1. Resistor values for Different VGATE Pin Voltages

VGATE1=VGATE2	R54=R56
4.7 V	174 Ohms
4.8 V	120 Ohms
4.9 V	56 Ohms
5.0 V	0 Ohm

VCS Interface and LOBIAS Interface

VCS1, VCS2 pins are bias pins for IF amplifiers on each channel and set the reference currents to these IF amplifiers. The VCS voltage is generated from the 5V supply by series resistors. Higher IIP3 values can be obtained by changing the values of these series resistors R61 and R73, which will change the total supply current of the IF amplifiers which can be seen on Table 2 a.

LOBIAS1, LOBIAS2 pins are bias pins for LO amplifiers and set the reference currents to these LO amplifiers. The LOBIAS voltage is generated from the 5V supply by series resistors R71 and R57. Changing LOBIAS2 voltage, changes current consumed by LOVDD pin, which can be seen at Table 2 b.

HMC1190LP6GE`s flexible design allows users to choose best configuration for their needs. For higher power consumption, better OIP3 values can be achieved.

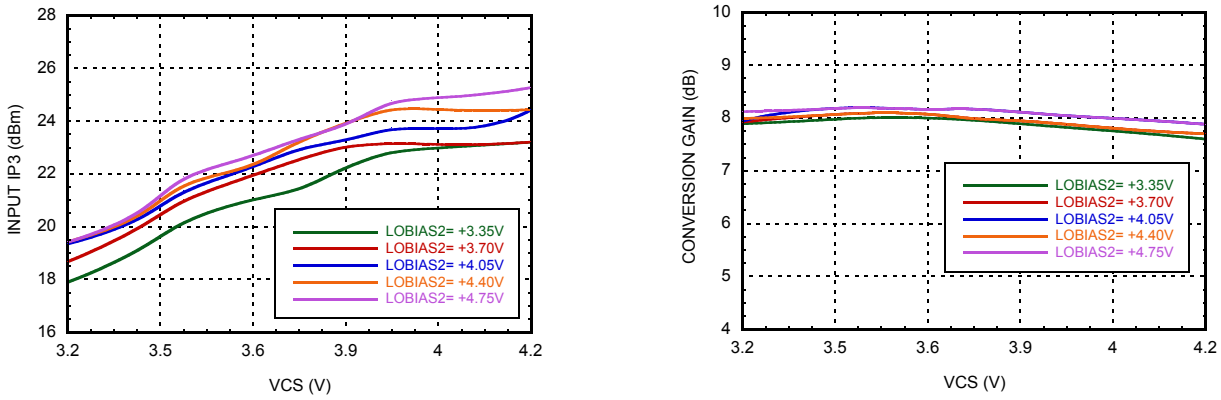


Figure 3. Conversion Gain, IIP3 vs. VCS1, VCS2 and LOBIAS2 voltages at 1900 MHz RF Input. [1]

Figure 3 shows the measured conversion gain and IIP3 vs. VCS and LOBIAS2 voltages at 1900MHz.Conversion gain and IIP3 vs. VCS and LOBIAS2 voltages at 1900MHz.

Table 2 a. VCS voltage vs IF Amplifier Currents

VCS Jumper, J13 (V)	VCS Pin (V)	IF Amp (mA)	R61=R73
5.0 V	4.25	181	440 Ohms
	4.0	159	590 Ohms
	3.75	135	740 Ohms
	3.5	110	880 Ohms
	3.25	86	1 KOhms

[1] Balun losses at IF output ports are de-embedded.

Table 2 b. LOBIAS2 voltage vs LO Amplifier Currents

LOBIAS Jumper, J12 (V)	LOBIAS2 Pin (V)	LO Amp (mA)	R71=R57
5.0 V	4.75	157	110 Ohms
	4.4	150	270 Ohms
	4.05	143	420 Ohms
	3.7	135	580 Ohms
	3.36	128	740 Ohms

External RF Matching

The HMC1190LP6GE`s RF inputs are internally broadband matched to 50Ω. RF inputs can be externally matched for a specific RF frequency band of interest to further improve Input IP3 (IIP3). Matching RF inputs to a specific RF frequency band can be easily accomplished by adding a series inductor and a shunt capacitor. See Table 3 for values of the external matching components for corresponding RF frequency bands. Application circuit with the external components on RF input pins can be seen at Figure 7.

VGATE1, VGATE2 pin voltages can be optimized for a specific RF frequency band by changing the resistor values in series with these pins. Table-1 shows the resistor values (R54, R56) for corresponding VGATE pin voltage.

Figure 4, Figure 5, and Figure 6 show the measured conversion gain, IIP3 and OIP3 for 900MHz, 1900MHz and 2500MHz RF frequency bands.

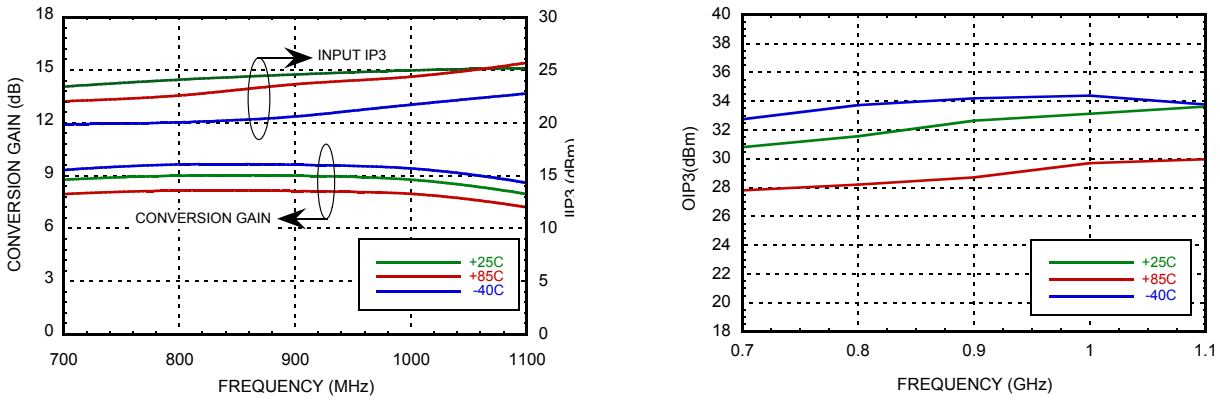


Figure 4. Conversion gain, IIP3 and OIP3 for 900MHz RF frequency band. [1]

[1] Balun losses at IF output ports are de-embedded.

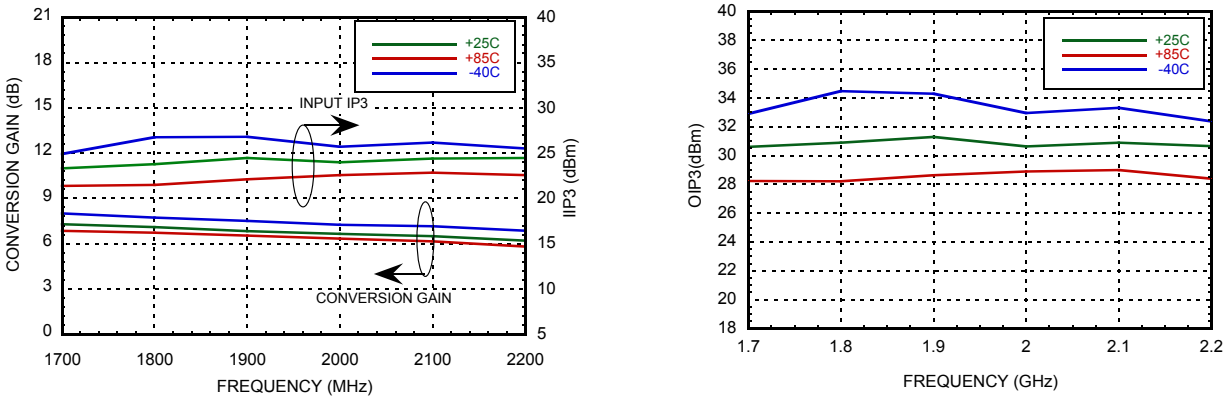


Figure 5. Conversion Gain, IIP3 and OIP3 for 1900MHz RF frequency band. [1]

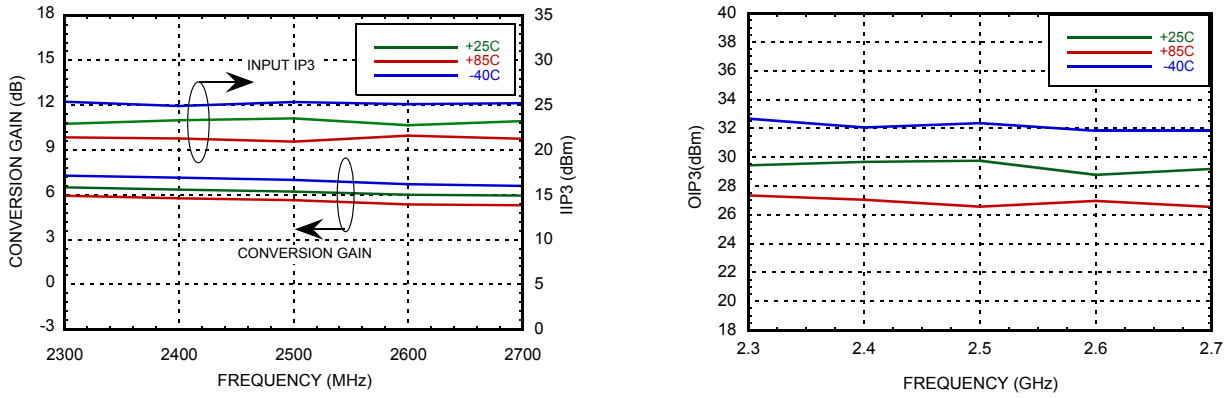


Figure 6. Conversion Gain, IIP3 and OIP3 for 2500MHz RF frequency bands. [1]

Table 3. Components for Selected Frequency Bands

Tune Frequency	C82	C81	C80	R55	Recommended VGATE1,2 Voltages
900 MHz	2.7 pF	8.2 nH	Open	0 Ohm	5.0V
1900 MHz	1 pF	2.7 nH	Open	120 Ohms	4.8V
2500MHz	Open	1 nH	1 pF	120 Ohms	4.8V

[1] Balun losses at IF output ports are de-embedded.

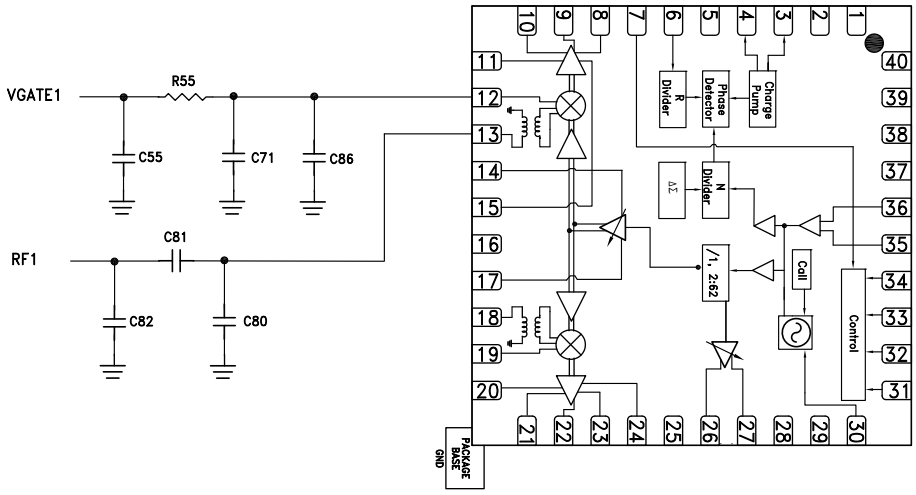


Figure 7. Application Circuit for Narrowband RF Input Matching

It is recommended to use high side LO injection for RF frequencies below 1.2 GHz for better IIP3. For instance, higher IIP3 can be obtained if LO input is driven with high side at RF=900 MHz. Please refer to Figure 8.

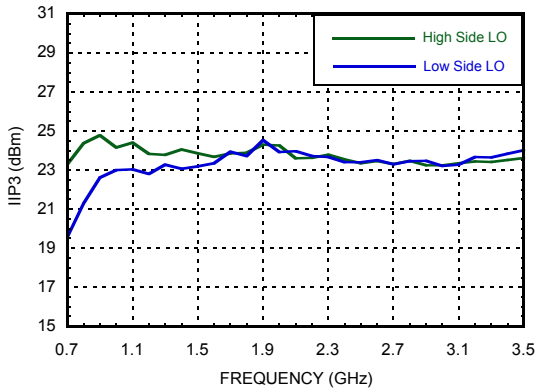


Figure 8. Input IP3 vs. High Side LO & Low Side LO @ VGATE=4.8V

Input IP3 Dependence on RF Input Power

The HMC1190LP6GE accepts a wide range of RF input power. Figure 9 shows the IIP3 vs. RF input power for 1900 MHz RF and 150 MHz IF.

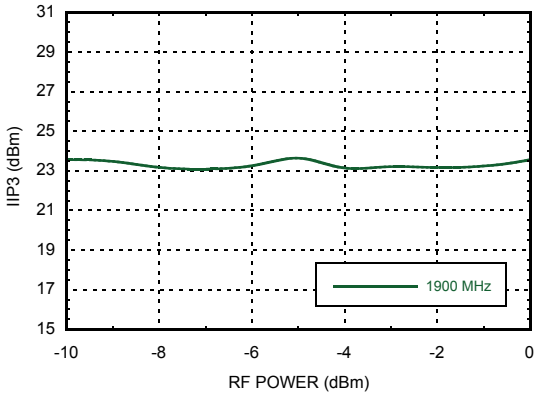


Figure 9. IIP3 vs. RF Input Power, RF= 1900 MHz, IF= 150 MHz, VGATE= 4.8V

Enabling / Disabling Mixer Features

HMC1190LP6GE has a dual channel down converter core but it can also be configured as a single channel one. When single channel option is desired, HMC1190LP6GE`s unused IF amplifier can be disabled through SPI interface.

HMC1190LP6GE can also be used as standalone PLL/VCO. In this case all IF and LO buffer amplifiers at mixer side can be disabled through SPI interface. Value of Reg14 should be changed in order to make necessary enable/disable changes. See Table 4 for details.

Table 4. Mixer Enable / Disable

REG14h value	Function
3F4	IF2 disabled, IF1 and LO_Mixer enabled
3F2	IF1 disabled, IF2 and LO_Mixer enabled
3F6	IF1, IF2 and LO_Mixer disabled
3F0	IF1, IF2 and LO_Mixer enabled

USING AN EXTERNAL VCO

In order to configure HMC1190LP6GE to use with an external VCO, Register 17 needs to be configured to disable the on chip VCO and VCO to PLL path. Enable External Buffer, second CP link and External I/O switch. To make these changes Reg 17 [0:11] should be configured as 3157d.

Figure 10 shows HMC1190LP6GE configured as PLL alone used with External VCO HMC384LP4E. Loop Filter components are used as below.

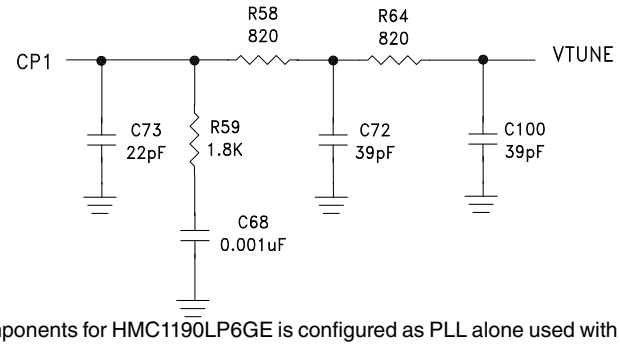


Figure 10. Loop filter components for HMC1190LP6GE is configured as PLL alone used with external VCO HMC384LP4E

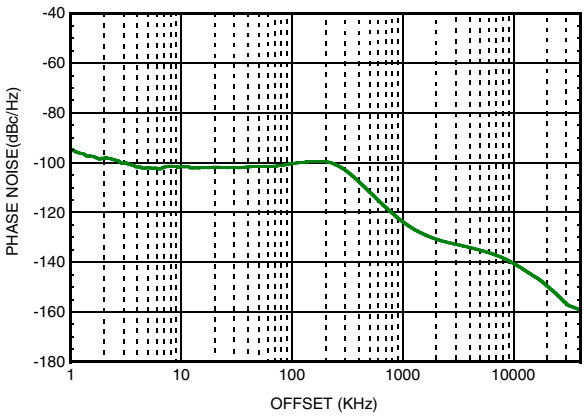


Figure 11. Closed Loop Phase Noise with External HMC384LP4E VCO @ 2200 MHz.

For detailed theory of operation of PLL/VCO, please refer to the "PLLs with Integrated VCOs - RF VCOs Operating Guide".

Serial Port Characteristics

Serial Port Open Mode

The Serial Port Open Mode features:

a. Compatibility with general serial port protocols that use shift and strobe approach to communication
b. Compatible with HMC PLL with Integrated VCO solutions, useful to address multiple chips of various types from a single serial port bus.

The Open Mode protocol has the following general features:

a. 3-bit chip address , can address up to 8 devices connected to the serial bus
b. Wide compatibility with multiple protocols from multiple vendors
c. Simultaneous Write/Read during the SPI cycle
d. 5-bit address space
e. 3 wire for Write Only capability, 4 wire for Read/Write capability

HMC RF PLLs with integrated VCOs support Open Mode.

Hittite's PLL and PLLs with integrated Microwave VCOs products do not support Open Mode.

Typical serial port operation can be run with SCLK at speeds up to 50 MHz

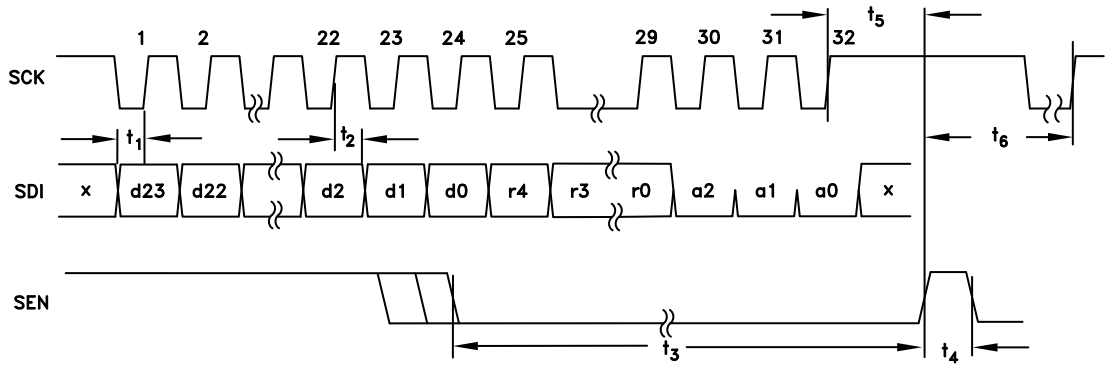


Figure 12. Open Mode - Serial Port Timing Diagram - WRITE

Open Mode - Serial Port WRITE Operation

AVDD = DVDD = 3V ±10%, AGND = DGND = 0V

Table 6. SPI Open Mode - WRITE Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK 32 Rising Edge to SEN Rising Edge	10			ns
	Max Serial port Clock Speed		50		MHz

Open Mode - Serial Port WRITE Operation cont'd

a. The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.

b. the slave (PLL with Integrated VCO) shifts in data on SDI on the first 24 rising edges of SCLK

c. Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK (25-29)

d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).

e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32).
Hittite reserves chip address a2:a0 = 000 for all RF PLL with Integrated VCOs.

f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).

g. Master asserts SEN after the 32nd rising edge of SCLK.

h. Slave registers the SDI data on the rising edge of SEN.

i. Master clears SEN to complete the WRITE cycle.

Open Mode - Serial Port READ Operation

A typical READ cycle is shown in Figure 13

In general, in Open Mode the LD_SDO line is always active during the WRITE cycle. During any Open Mode SPI cycle LD_SDO will contain the data from the current address written in Reg0h[7:3]. If Reg0h[7:3] is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress.

If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg0h[7:3], then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the Open Mode two cycle procedure to read from any random address is as follows:

a. The Master (host), on the first 24 falling edges of SCLK places 24-bit data, d23:d0, MSB first, on SDI as shown inFirst Cycle Figure 13. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on second cycle.
b. the slave (PLL with Integrated VCO) shifts in data on SDI on the first 24 rising edges of SCLK
c. Master places 5-bit register address , r4:r0, (the READ ADDRESS register), MSB first, on the next 5 falling edges of SCLK (25-29). r4:r0=00000.
d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32)..Chip address is always 000 for RF PLL with Integrated VCOs.
f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).
g. Master asserts SEN after the 32nd rising edge of SCLK.
h. Slave registers the SDI data on the rising edge of SEN.
i. Master clears SEN to complete the the address transfer of the two part READ cycle.
j. If one does not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.
k. Master places the same SDI data as the previous cycle on the next 32 falling edges of SCLK.
l. Slave (PLL with Integrated VCO) shifts the SDI data on the next 32 rising edges of SCLK. On these same edges the Slave places the desired read data (ie. data from the address specified in Reg0h[7:3] of the first cycle) on LD_SDO which automatically switches to SDO mode from LD mode, disabling the LD output.
m. Master asserts SEN after the 32nd rising edge of SCLK to complete the cycle and revert back to Lock Detect on LD_SDO.

Table 7. SPI Open Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK Rising Edge to SDO setup time			8.2ns+0.211ns/pF	ns

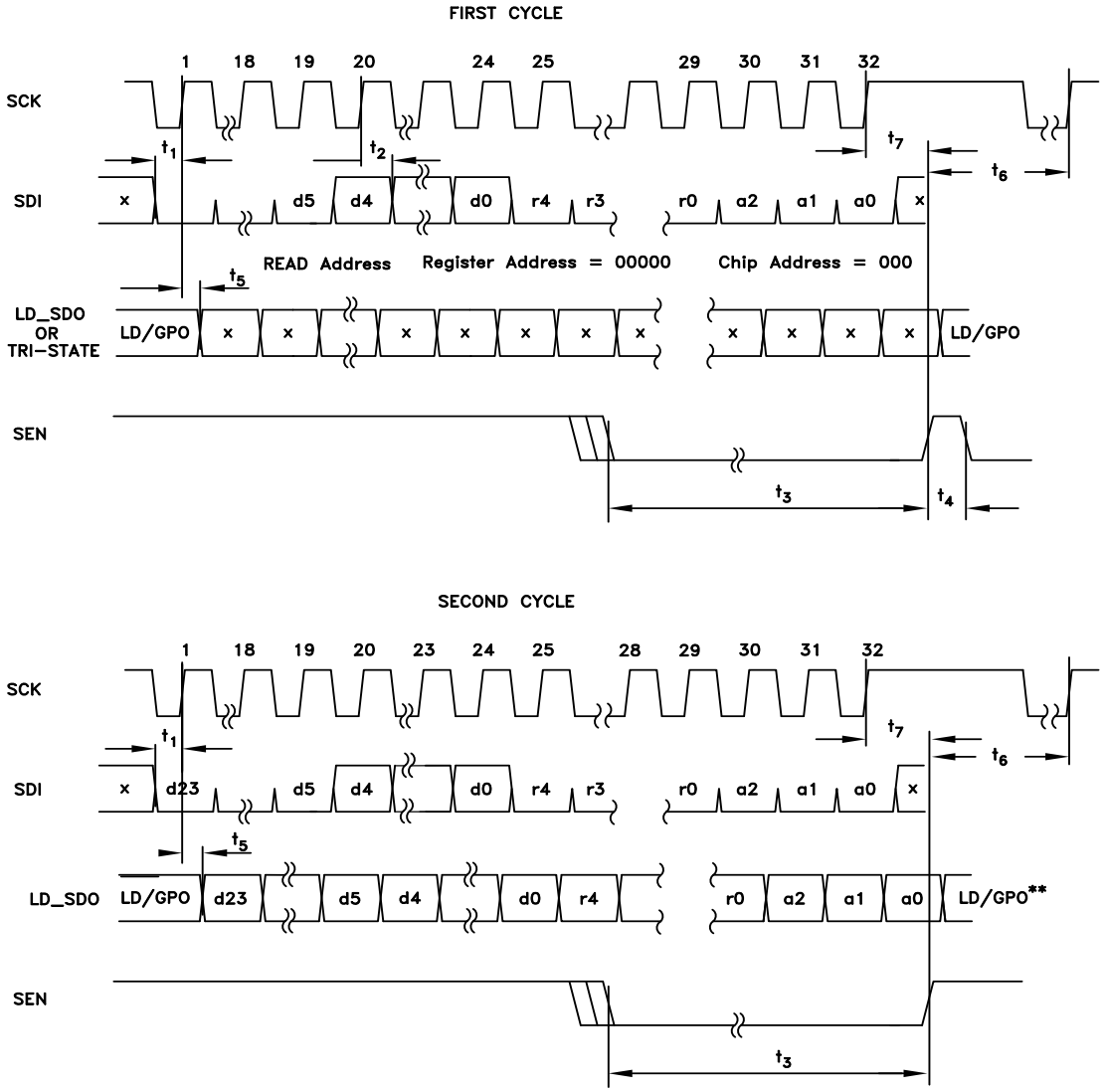


Figure 13. Open Mode - Serial Port Timing Diagram - READ 2 Cycle

Notes: