28 Gbps, 1:4 DEMUX WITH PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC855LC5 is ideal for:

- SONET OC-192
- Broadband Test & Measurement
- Serial Data Transmission up to 28 Gbps
- FPGA Interfacing

Features

Differential & Singe-Ended Operation

Half Rate Clock Input

Quarter Rate Reference Clock Output

Fast Rise and Fall Times: 22 ps

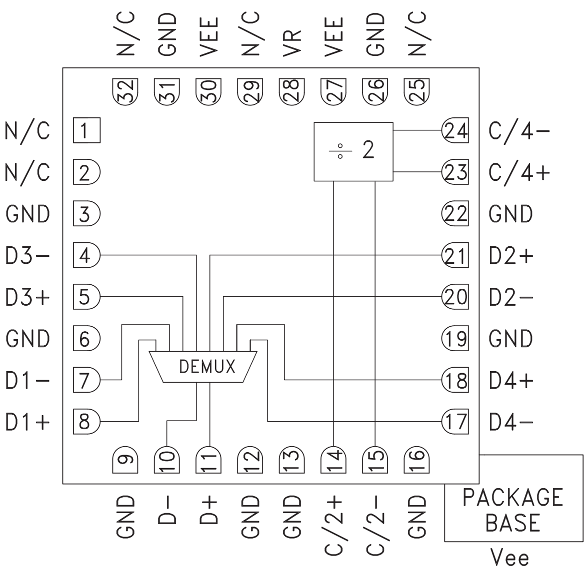
Low Power Consumption: 644 mW typ.

Programmable Differential
Output Voltage Swing: 450 - 1144 mV

Single Supply: -3.3V

32 Lead Ceramic 5x5 mm SMT Package: 25 mm^2

Functional Diagram



General Description

The HMC855LC5 is a 1:4 demultiplexer designed for data deserialization up to 28 Gbps. The device uses both rising and falling edges of the half-rate clock to sample the input data in sequence, D0-D3 and latches the data onto the differential outputs. A quarter-rate clock output generated on chip can be used to clock the data into other devices. The demux is DC coupled supporting broadband operation.

All clock and data inputs to the HMC855LC5 are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. The differential outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm ground terminated system, or drive devices with CML logic input. The HMC855LC5 also features an output level control pin, VR, which allows for loss compensation or signal level optimization. The HMC855LC5 operates from a single -3.3V supply and is available in RoHS compliant 5x5 mm SMT package.

Electrical Specifications, T_A = +25°C, Vee = -3.3V, VR = 0V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			195		mA
Maximum Data Rate			28		Gbps
Maximum Clock Rate, Half Rate			14		GHz
Input Voltage Range, CML		-1.5		0.5	V
Input Differential Voltage		100		2000	mV
Output Rise / Fall Time	Differential, 20% - 80%		22		ps
Input Return Loss	Frequency <28 GHz		10		dB

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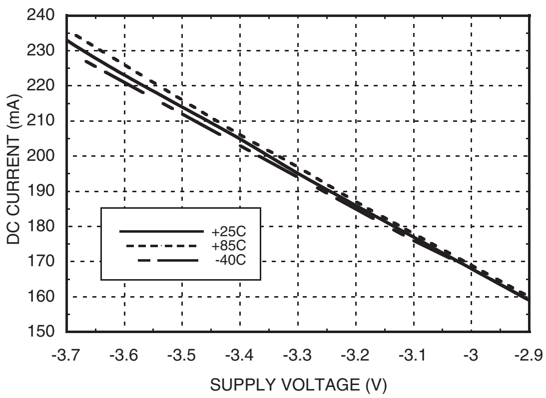
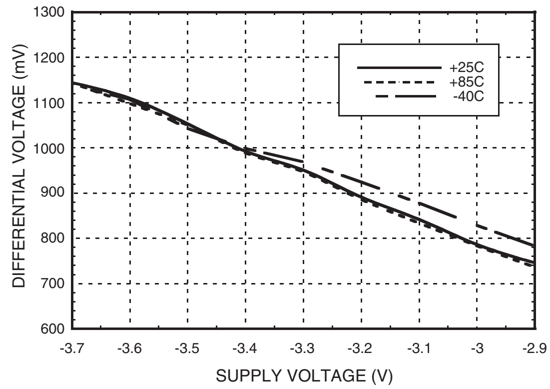
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Output Amplitude	Single-Ended, peak-to-peak		500		mVp-p
	Differential, peak-to-peak		1000		mVp-p
Output High Voltage			0		mV
Output Low Voltage			-500		mV
Output Return Loss	Frequency <22 GHz		10		dB
Propagation Delay Clock to Data, Tpdd			149		ps
Propagation Delay Clock to Output Clock, Tpdc			142		ps
Set Up Time, t_s			16		ps
Hold Time, t_h			3		ps

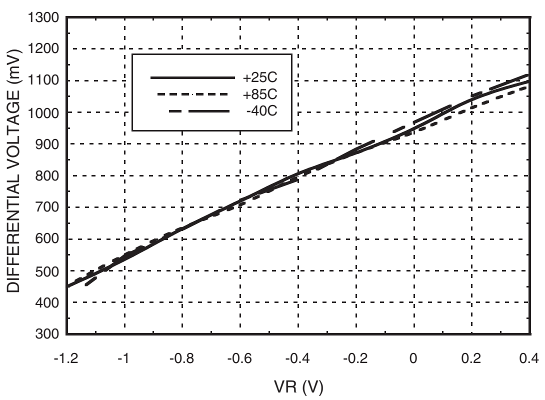
DC Current vs. Supply Voltage [1] [2]



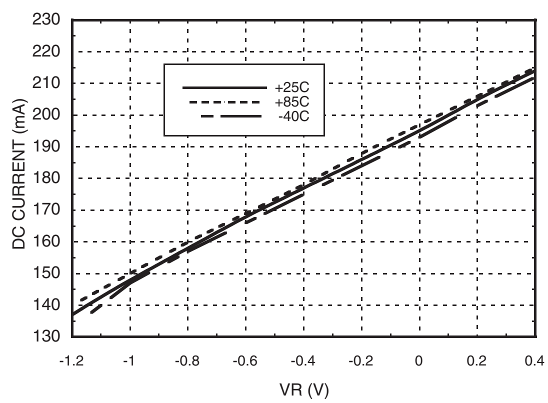
Output Differential vs. Supply Voltage [1] [2]



Output Differential vs. VR [2][3]



DC Current vs. VR [2][3]



[1] VR = 0.0V [2] Frequency = 28 Gbps [3] Vee = -3.3V

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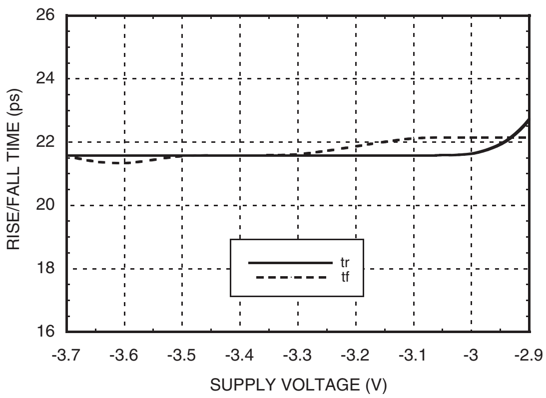
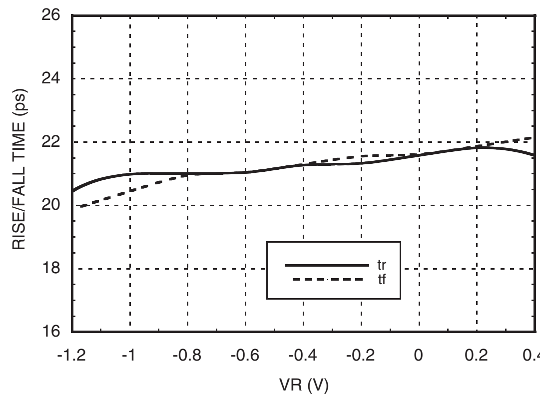
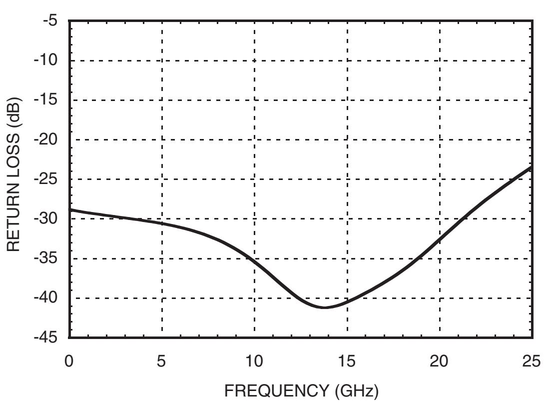
Rise / Fall Time vs. Supply Voltage [1][2]



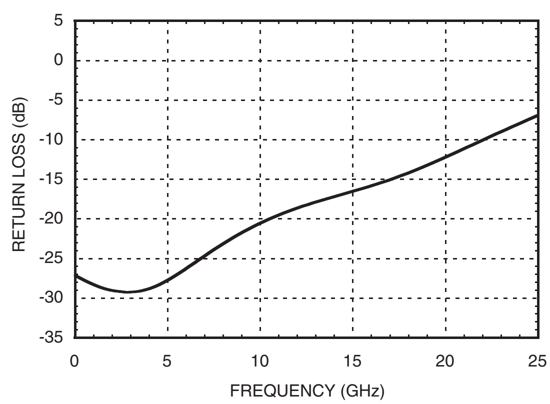
Rise / Fall Time vs. VR [2][4]



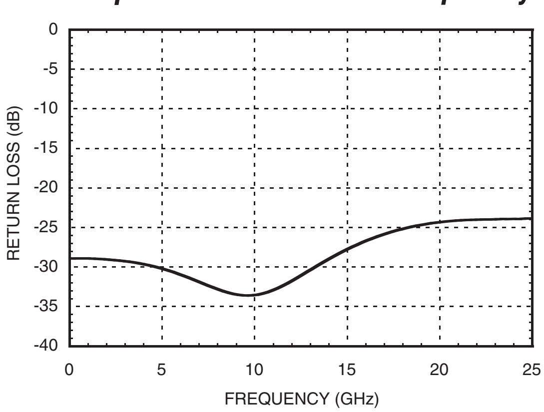
Data Input Return Loss vs. Frequency [1][3][4]



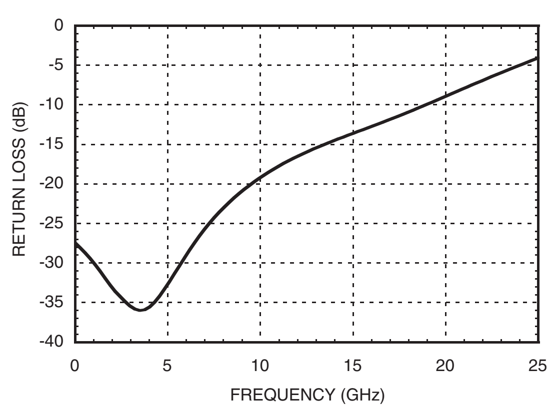
Data Output Return Loss vs. Frequency [1][3][4]



Clock Input Return Loss vs. Frequency [1][3][4]



Clock Output Return Loss vs. Frequency [1][3][4]



[1] VR = 0.0V [2] Frequency = 28 Gbps [3] Device measured on evaluation board with gating [4] Vee = -3.3V

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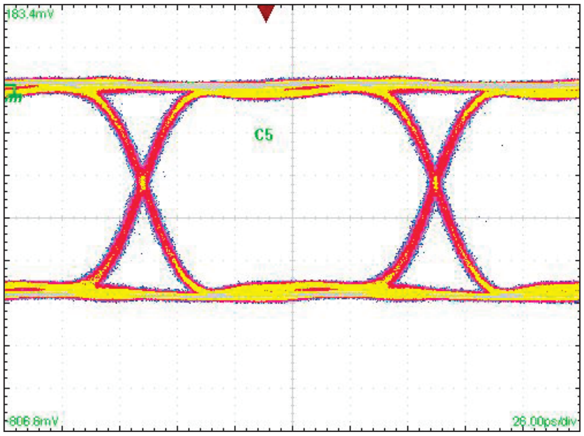
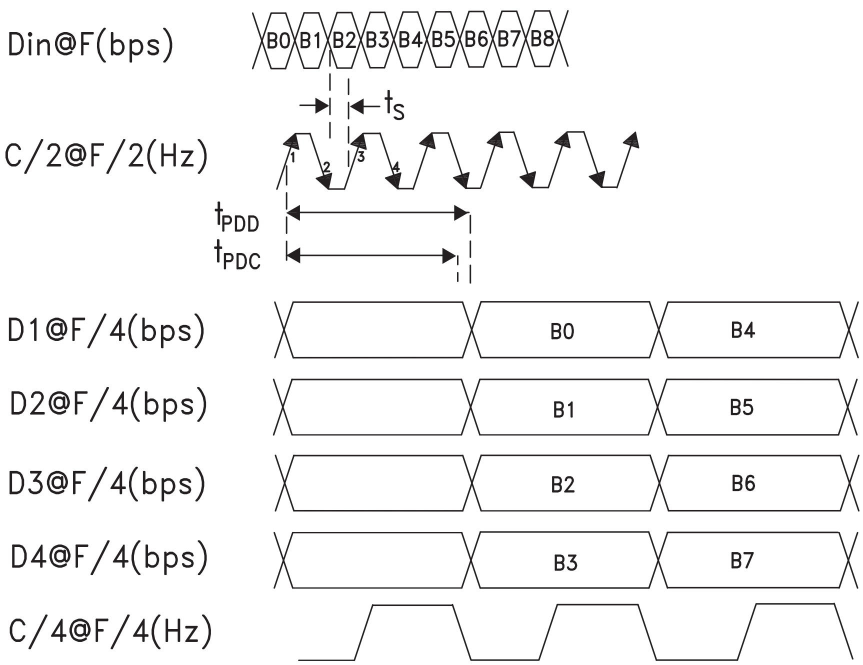
Eye Diagram @ 28 Gbps



Test Conditions:

Differential 400 mV data input and 300 mV clock input. Pattern generated with a 2^{15}-1 PN 28 Gbps PRBS pattern. Resulting in a 7 Gbps output measured using a Tektronix CSA 8000

Timing Diagram



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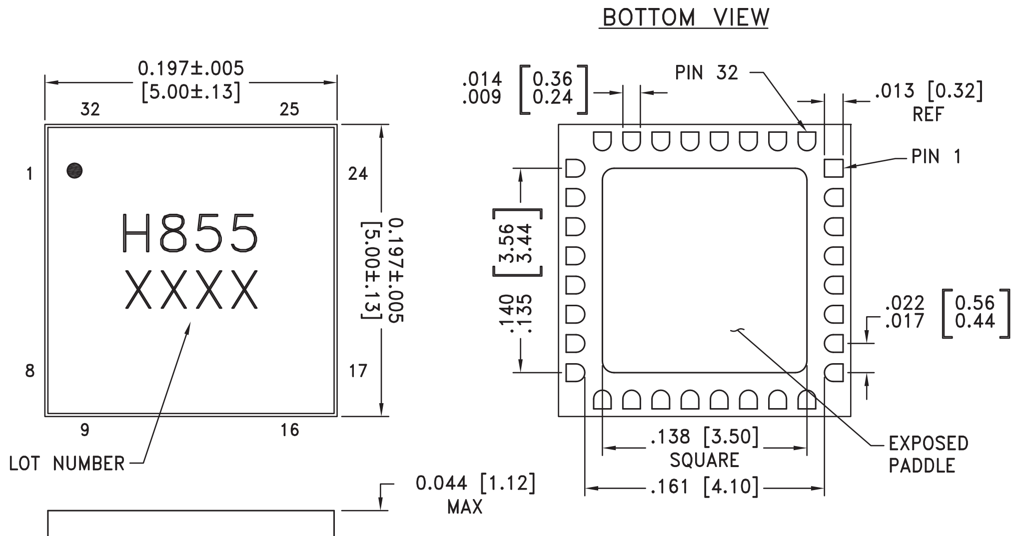
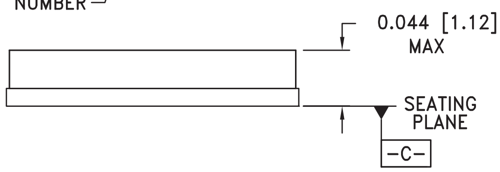
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75V to +0.5V
Input Signals	-2V to +0.5V
Output Signals	-1.5V to +0.5V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 33 mW/°C above 85 °C)	1.33 W
Thermal Resistance ($R_{th\ j-p}$) Worse case device to package paddle	30 °C/W
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing





NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

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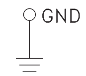
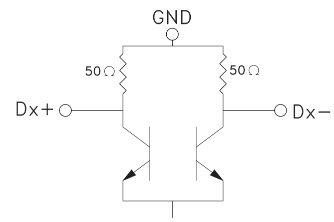
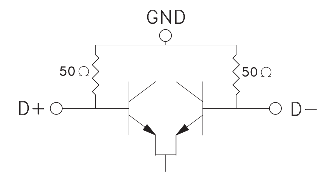
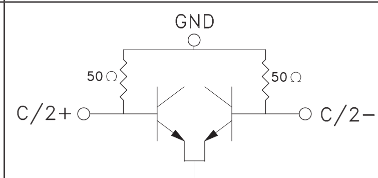
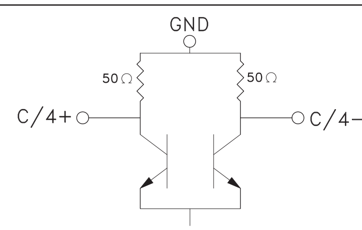
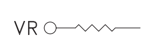
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 25, 29, 32	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
3, 6, 9, 12, 13, 16, 19, 22, 26, 31	GND	These pins must be connected to a high quality RF/DC ground.	
4, 5, 7, 8, 17, 18, 20, 21	D3-, D3+ D1-, D1+ D4-, D4+ D2-, D2+	Differential Data Outputs: Current Mode Logic(CML) referenced to positive supply	
10, 11	D-, D+	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply	
14, 15	C/2+, C/2-	Differential Half-Rate Clock Inputs: Current Mode Logic (CML) referenced to positive supply	
23, 24	C/4+, C/4-	Differential Quarter-Rate Clock Outputs: Current Mode Logic(CML) referenced to positive supply	
27, 30, Package Base	Vee	These pins and the exposed paddle must be connected to the negative voltage supply.	
28	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per “Output Differential vs. VR” plot.	

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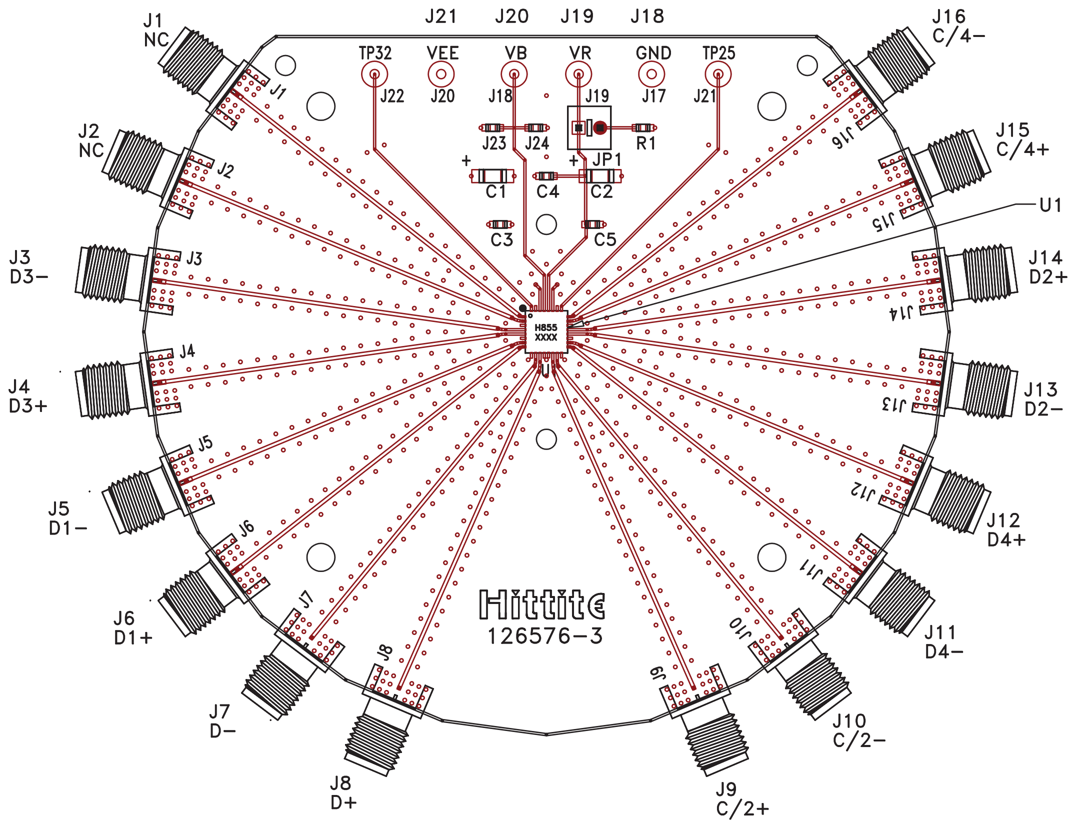
Evaluation PCB



List of Materials for Evaluation PCB 126578 [1]

Item	Description
J7 - J10	PCB Mount K RF Connectors
J3 - J6, J11 - J16	PCB Mount SMA RF Connectors
J18 -J21	DC Pin
JP1	2 Position Header with Shunt
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC855LC5 28 Gbps 1:4 Demux
PCB [2]	126576 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

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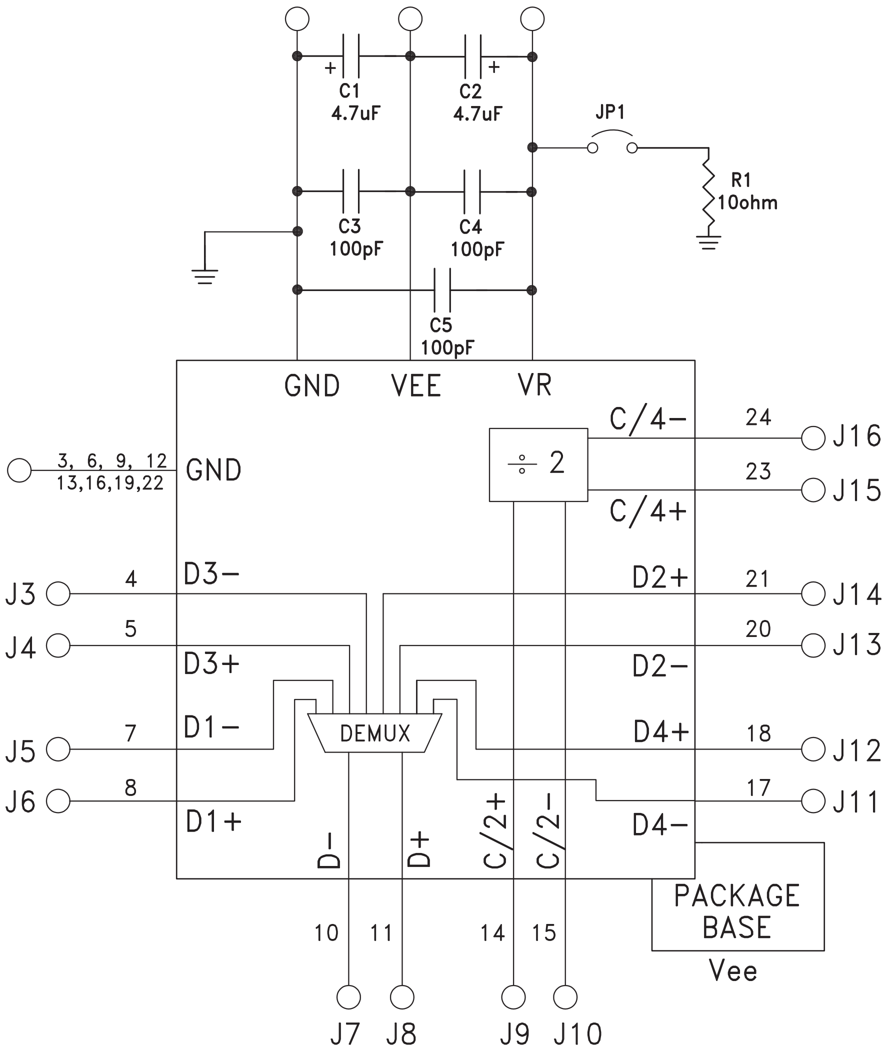
Application Circuit



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