

Rev. V6

Features

- High Linear Gain: 22 dB Typical
- High Saturated Output Power: +31.5 dBm Typical
- High Power Added Efficiency: 22% Typical
- 50 Ω Input/Output Broadband Matched
- Integrated Output Power Detector
- Lead-Free Ceramic Bolt Down Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The AM42-0002 is a three-stage MMIC linear power amplifier in a lead-free, ceramic bolt down style hermetic package. The AM42-0002 employs a fully matched chip with internally decoupled gate and drain bias networks and an output power detector. The AM42-0002 is designed to be operated from a constant voltage drain supply.

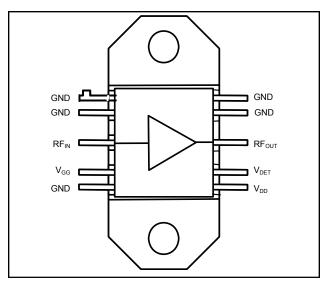
The AM42-0002 is designed for use as an output stage or a driver, in applications for VSAT systems. This design is fully monolithic and requires a minimum of external components.

The AM42-0002 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

Ordering Information

Part Number	Package
AM42-0002	Ceramic Bolt Down

Functional Schematic



Pin Configuration

Pin No.	Pin Name	Description	
1	GND	DC and RF Ground	
2	GND	DC and RF Ground	
3	RF _{IN}	RF Input	
4	V_{GG}	Gate Supply	
5	GND	DC and RF Ground	
6	V_{DD}	Voltage Drain Supply	
7	V_{DET}	Output Power Detector	
8	RF _{OUT}	RF Output	
9	GND	DC and RF Ground	
10	GND	DC and RF Ground	

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^{*} Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: $T_A = +25^{\circ}C$, $V_{DD} = +9$ V, $V_{GG} = -5.0$ V, $Z_0 = 50\Omega$

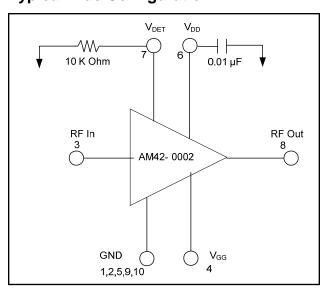
Parameter	Test Conditions	Units	Min.	Тур.	Max.
Linear Gain	P _{IN} ≤ 0 dBm	dB	19	22	_
Input VSWR	P _{IN} ≤ 0 dBm	Ratio	_	2.5:1	2.7:1
Output VSWR	P _{IN} ≤ 0 dBm	Ratio	_	2.7:1	_
Saturated Output Power	P _{IN} = +14 dBm	dBm	30.5	31.5	_
Output Power at P1dB	_	dBm	31	29.5	_
Output IP3	Two +24 dB, output tones @ 1 MHz spacing	dBm	_	39	_
Power Added Efficiency	P _{IN} = +14 dBm	%	_	22	_
Bias Current	P _{IN} = +14 dBm	mA	_	800	1400
Thermal Resistance	25°C Heat Sink	°C/W	_	9.5	_
Detector Output Voltage	R_L = 10 K Ω , P_{OUT} = +31dBm	V	_	+3.5	_

Absolute Maximum Ratings 1,2,3

Parameter	Absolute Maximum		
V _{DD}	12 Volts		
V_{GG}	-10 Volts		
Power Dissipation	13.2 W		
RF Input Power	+23 dBm		
Channel Temperature	150°C		
Storage Temperature	-65°C to +150°C		

- 1. Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM Technology does not recommend sustained operation near these survivability limits.
- 3. Case Temperature $(T_C) = +25^{\circ}C$.

Typical Bias Configuration^{4,5,6,7,8,9}



- Nominal bias is obtained by first connecting –5 volts to pin 4 (VGG), followed by connection +9 volts to pin 6 (VDD). Note sequence.
- RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
- 6. No DC bias voltage appears at the RF ports.
- The DC resistance at the input port is an open circuit and at the output port is a short circuit.
- 8. For optimum IP3 performance, the VDD bypass capacitors should be placed within 0.5 inches of pin 6.
- Resistor and capacitors surrounding the amplifier are suggestions and not included as part of the AM42-0002.

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PRELIMINARY: Data Sheets contain information regarding a product M/A-COM Technology

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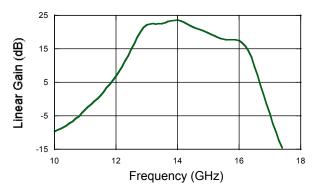
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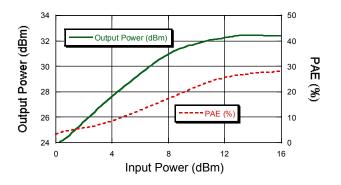
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Typical Performance Curves @ +25°C

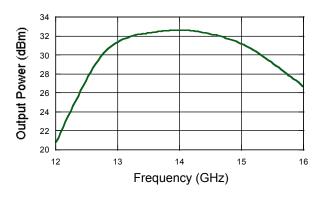
Linear Gain vs. Frequency



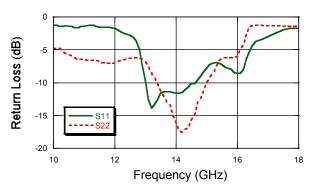
Output Power & PAE vs. Input Power @ 14.25 GHz



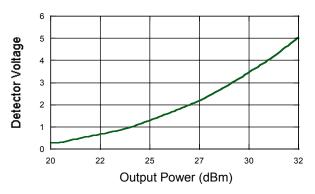
Output Power vs. Frequency @ $P_{IN} = +14 \text{ dBm}$



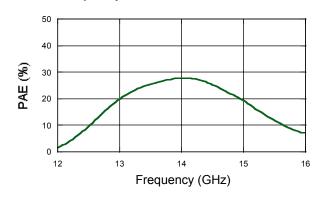
Input and Output Return Loss vs. Frequency



Detector Voltage vs. Output Power @ 14.25 GHz



PAE vs. Frequency @ $P_{IN} = +14 dBm$



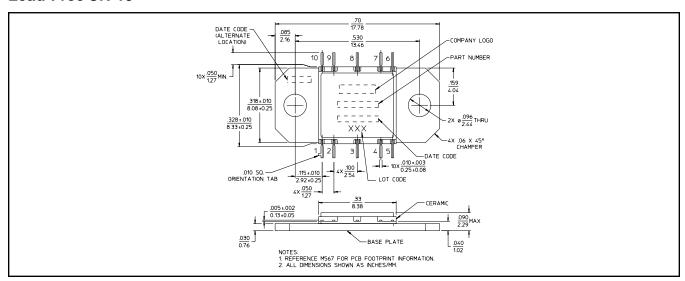
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Lead-Free CR-15[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level 1 requirements.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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