AM42-0007-DIE



GaAs MMIC Power Amplifier, 2.0 W 14.0 - 14.5 GHz

Rev. V6

Features

- High Linear Gain: 22 dB Typical.
- High Saturated Output Power: +33 dBm Typical
- High Power Added Efficiency: 22% Typical
- High P1dB: +32 dBm Typical
- 50 Ω Input / Output Broadband Matched
- Integrated Output Power Detector
- High Performance Ceramic Bolt Down Package

Description

The AM42-0007-DIE is a three stage MMIC linear power amplifier fabricated on a mature 0.5 micron MBE based GaAs process. The AM42-0007-DIE employs a fully matched chip with integral bias networks and output power detector.

This GaAs MMIC power amplifier is ideally suited for used as an output stage or driver in applications for VSAT applications.

Ordering Information

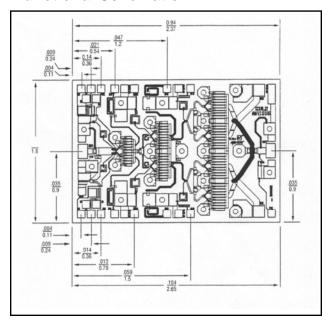
Part Number	Package		
AM42-0007-DIE	DIE		

Absolute Maximum Ratings ^{1,2}

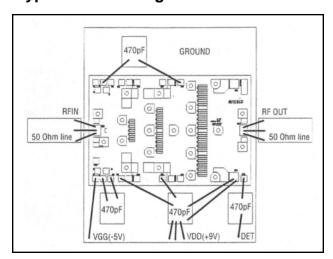
Parameter	Absolute Maximum			
V_{DD}	+12 Volts			
V_{GG}	-10 Volts			
Power Dissipation	17.9 W			
RF Input Power	+23 dBm			
ChannelTemperature	+150 °C			
Storage Temperature	-65 °C to +150 °C			

- 1. Exceeding any one or combination of these limits may cause permanent damage to this device.
- 2. Back of die temperature (T_B) = +25°C.

Functional Schematic



Typical Bias Configuration 3,4



- 3. Nominal bias is obtained by first connecting -5 volts to pin V_{GG} (resistor network used) followed by connecting +9 volts to pin V_{DD}. Note sequence.
- 4. It is recommended that the die be mounted with Au/Sn eutectic performs for good RF ground and thermal interface.

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Electrical Specifications 5 : $T_B = +25^{\circ}C$, $V_{DD} = +9$ V, $V_{GG} = -1.2V, \, Z_0 = 50 \; \Omega$

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Linear Gain	$P_{IN} < 0 \text{ dBm}$	dB	_	22	
Input VSWR	_	Ratio	_	2.5:1	
Output VSWR	_	Ratio	_	2.7:1	_
Saturated Output Power	P _{IN} < +14 dBm	dBm	_	+33	_
Output Power @ 1 dB Compression	-	dBm	31	+32	_
Output IP ₃	-	dBm	_	41	_
Power Added Efficiency (PAE)	P _{IN} < +14 dBm	%	_	22	_
Bias Current	I _{DSQ} (No RF) I _{GG} (No RF)	mA mA	_	850 0.1	_
Thermal Resistance	θ CB2 ⁶	°C/W	_	7	_
Detector Output Voltage (V _{DET})	Pin = +3 dBm, Ids = 750 mA Typ.	V	_	+3.5	_

^{5. 100%} on wafer tested (50 µs pulse width, 20% duty factor) without resistor network on gates.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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^{6.} Channel to die backside.

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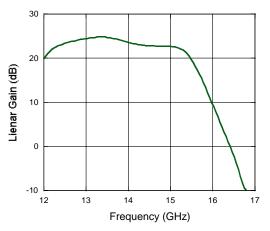


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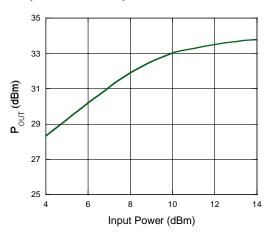
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Typical Performance @ 25°C

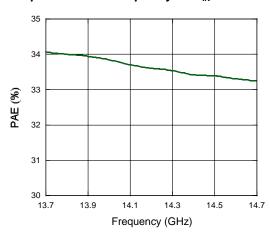
Linear Gain vs. Frequency



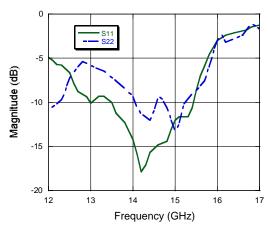
Output Power vs. Input Power @ 14 GHz



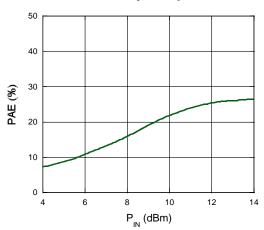
Output Power vs. Frequency @ $P_{IN} = +14 \text{ dBm}$



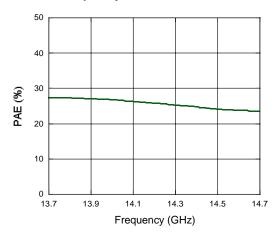
Input & Output Return Loss vs. Frequency



Power Added Efficiency vs. Input Power @ 14 GHz



PAE vs. Frequency @ $P_{IN} = +14 dBm$



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