AM42-0039

2 Watt C-Band VSAT Power Amplifier
5.9 - 7.1 GHz

Rev. V5

Features

- High Linear Gain: 33 dB Typical
- High Saturated Output Power: +33 dBm Typ.
- High Power Added Efficiency: 25% Typ.
- 50 Ω Input / Output Broadband Matched
- Integrated Output Power Detector
- Lead-Free Bolt Down Ceramic Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The AM42-0039 is a three stage MMIC power amplifier in a lead-free, bolt down ceramic package, allowing easy assembly. This device employs a fully matched chip with internally decoupled gate and drain bias networks. The device is designed to operate from a constant current drain supply or a constant voltage gate supply. By varying the bias conditions, the saturated output power performance of this device may be tailored for various applications.

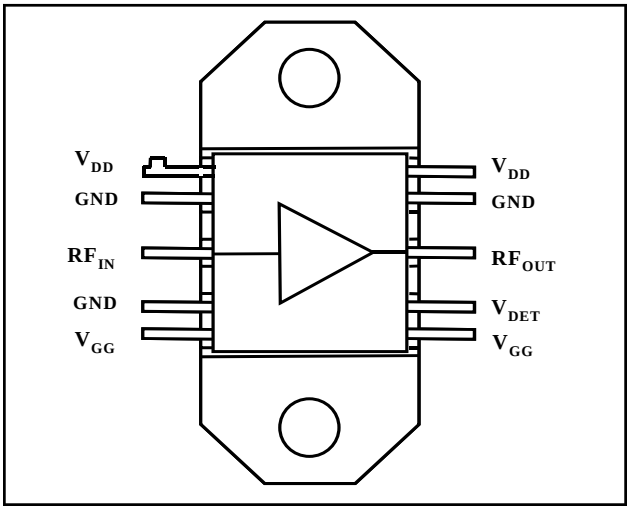
The AM42-0039 is ideally suited for use as an output stage or a driver amplifier in VSAT systems. The AM42-0039 includes internal supply line bypassing in the package, minimizing the number of external components required.

The AM42-0039 is fabricated using a mature 0.5 micron MBE based GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

Ordering Information

Part Number	Package
AM42-0039	CR-15 Ceramic Bolt Down Package

Functional Schematic



Pin Configuration

Pin No.	Pin Name	Description
1	V_{DD}	Drain Supply
2	GND	DC and RF Ground
3	RF_{IN}	RF Input
4	GND	DC and RF Ground
5	V_{GG}	Gate Supply
6	V_{GG}	Gate Supply
7	V_{DET}	Output Power Detector
8	RF_{OUT}	RF Output
9	GND	DC and RF Ground
10	V_{DD}	Drain Supply
Flange	GND	DC and RF Ground

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: T_A =+25°C, V_{DD} = +8 V, V_{GG} adjusted for I_{DD} = 900 mA, F = 5.9 - 7.1

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	P_{IN} = -10 dBm	dB	31	33	35
Input VSWR	P_{IN} = -10 dBm	Ratio	—	2.5:1	3.0:1
Output VSWR	P_{IN} = -10 dBm	Ratio	—	2.5:1	—
Output Power	P_{IN} = +3 dBm, Ids = 900 mA Typ.	dBm	31.7	33.0	—
Output Power vs. Frequency	P_{IN} = +3 dBm, Ids = 900 mA Typ. (5.9 to 6.4 GHz) P_{IN} = +3 dBm, Ids = 900 mA Typ. (6.4 to 7.1 GHz)	dB dB	— —	±0.3 ±0.3	±0.75 ±0.75
Output Power vs. Temperature	T_A = -40°C to +85°C, P_{IN} = +7 dBm	dB	—	±0.4	—
Drain Bias Current	P_{IN} = +3 dBm	mA	800	900	1000
Gate Bias Voltage	P_{IN} = +3 dBm, Ids = 900 mA Typ.	V	-2.0	-1.2	-0.4
Gate Bias Current	P_{IN} = +3 dBm, Ids = 900 mA Typ.	mA	—	10	20
Thermal Resistance (qJC)	25°C Heat Sink	°C/W	—	7.0	—
Second Harmonic	P_{IN} = +3 dBm, Ids = 900 mA Typ.	dBc	—	-35	—
Third Harmonic	P_{IN} = +3 dBm, Ids = 900 mA Typ.	dBc	—	-45	—
Detector Voltage	P_{IN} = +3 dBm, Ids = 900 mA Typ.	V	—	4.0	—

Absolute Maximum Ratings[1,2,3]

Parameter	Absolute Maximum
Input Power	+15 dBm
Operating Voltages	V_{DD} = +10 volts; V_{GG} = -3 volts; V_{DD} - V_{GG} = 12 volts
Ids	1200 mA
Channel Temperature	+150 °C
Operating Temperature	-40 °C to +80 °C
Storage Temperature	-65 °C to +150 °C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM does not recommend sustained operation near these survivability limits.
3. Adequate heat sinking and grounding required on flange base.

Operating the AM42-0039

The AM42-0039 is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply -2.0 Volts to V_{GG}.
2. Ramp V_{DD} to +8V.
3. Adjust V_{GG} to set quiescent drain current .
4. Apply RF.
5. Power down in reverse sequence. Turn gate voltage off last.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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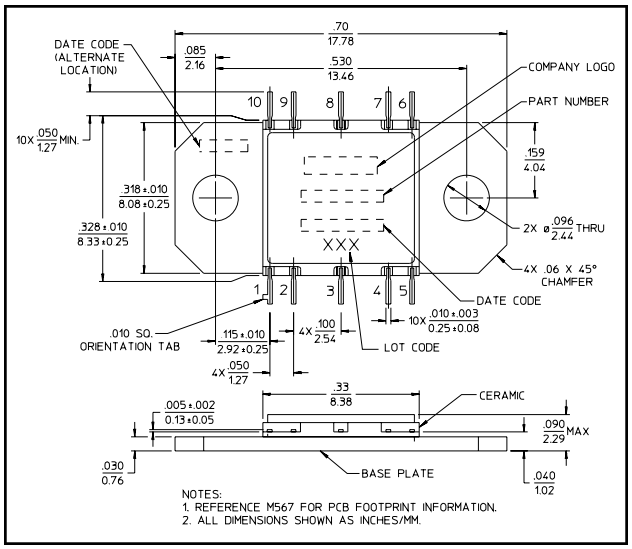
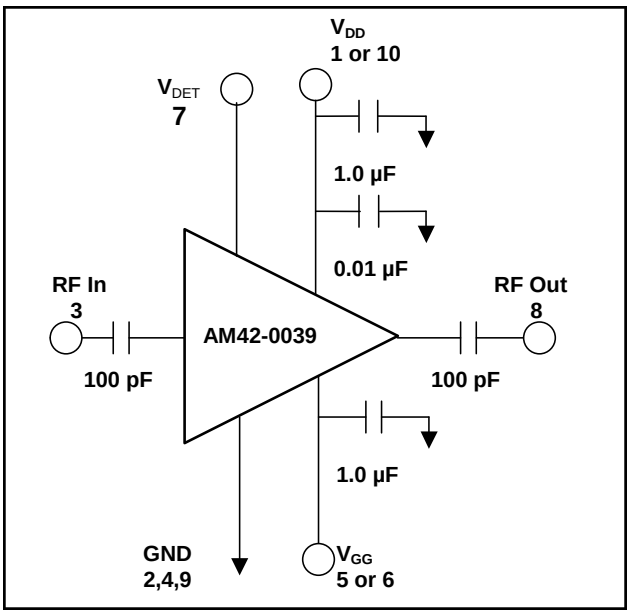
Lead-Free CR-15†



† Reference Application Note M538 for lead-free solder reflow recommendations.

Application Schematic [4,5,6]



4. Apply -2 volts to pin 5 or 6 (V_{GG}), prior to applying +8 volts to pins 1 or 10 (V_{DD}). Adjust V_{GG} for typical drain current.
5. External DC blocking capacitors required on the RF ports.
6. For optimum IP3 performance, V_{DD} bypass capacitors should be placed within 0.5 inches of the V_{DD} leads.

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