

Features

- N-Channel enhancement mode device
- DMOS structure
- Lower capacitances for broadband operation
- High saturated output power
- Lower noise figure than competitive devices

ABSOLUTE MAXIMUM RATINGS AT 25° C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	8*	A
Power Dissipation	P_D	206	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	0.85	°C/W

TYPICAL DEVICE IMPEDANCE

F (MHz)	Z_{IN} (Ω)	Z_{LOAD} (Ω)
30	4.5 - j14.5	13.5 + j4.5
100	3.0 - j10.5	13.5 + j6.0
175	2.0 - j7.5	12.0 + j4.5

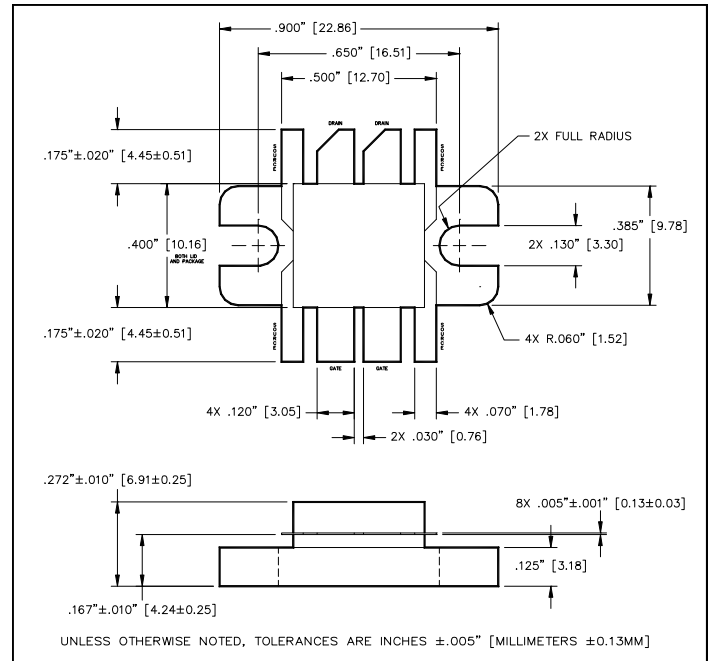
$V_{DD} = 28V, I_{DQ} = 400mA, P_{OUT} = 80W$

ELECTRICAL CHARACTERISTICS AT 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	65	-	V	$V_{GS} = 0.0V, I_{DS} = 10.0mA$
Drain-Source Leakage Current	I_{DSS}	-	2.0	mA	$V_{GS} = 28.0V, V_{DS} = 0.0V$
Gate-Source Leakage Current	I_{GSS}	-	2.0	μA	$V_{GS} = 20.0V, V_{DS} = 0.0V$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS} = 10.0V, I_{DS} = 200.0mA$
Forward Transconductance	G_M	1.0	-	S	$V_{DS} = 10.0V, I_{DS} = 2000.00mA, \Delta V_{GS} = 1.0V, 80\mu s$ Pulse
Input Capacitance	C_{ISS}	-	90	pF	$V_{DS} = 28.0V, F = 1.0MHz$
Output Capacitance	C_{OSS}	-	80	pF	$V_{DS} = 28.0V, F = 1.0MHz$
Reverse Capacitance	C_{RSS}	-	16	pF	$V_{DS} = 28.0V, F = 1.0MHz$
Power Gain	G_P	13	-	dB	$V_{DD} = 28.0V, I_{DQ} = 400mA, P_{OUT} = 80.0W, F = 175MHz$
Drain Efficiency	η_D	60	-	%	$V_{DD} = 28.0V, I_{DQ} = 400mA, P_{OUT} = 80.0W, F = 175MHz$
Load Mismatch Tolerance	VSWR-T	-	30:1	-	$V_{DD} = 28.0V, I_{DQ} = 400mA, P_{OUT} = 80.0W, F = 175MHz$

*Per side

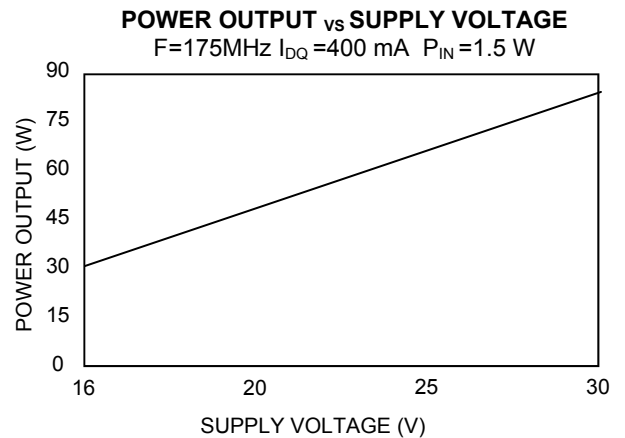
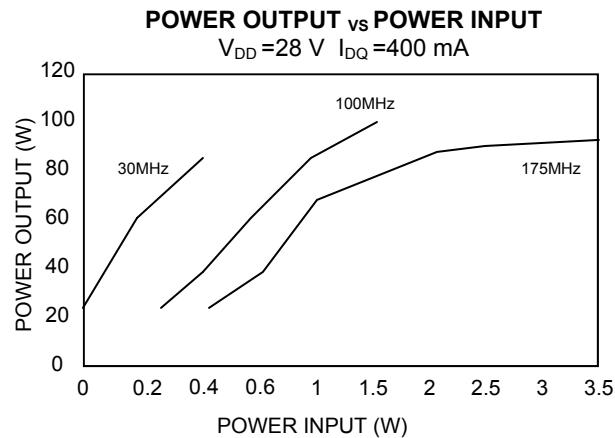
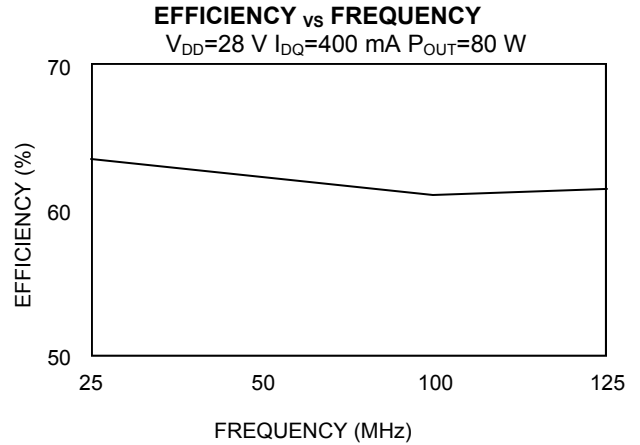
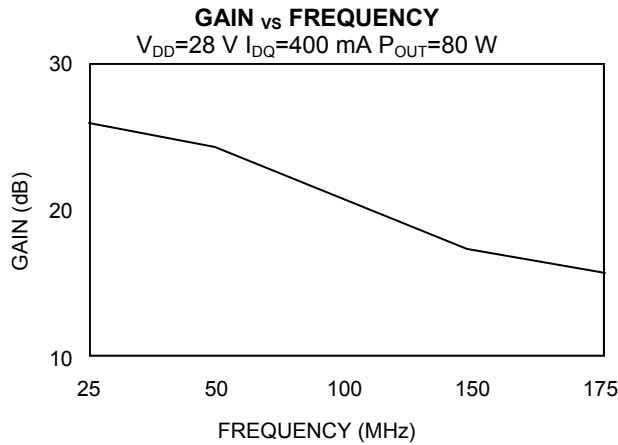
Package Outline



Z_{IN} is the series equivalent input impedance of the device from gate to source.

Z_{LOAD} is the optimum series equivalent load impedance as measured from drain to ground.

Typical Broadband Performance Curves



TEST FIXTURE ASSEMBLY

