

XP1005-BD



Power Amplifier
35.0-43.0 GHz

Rev. V2
MimiX Broadband

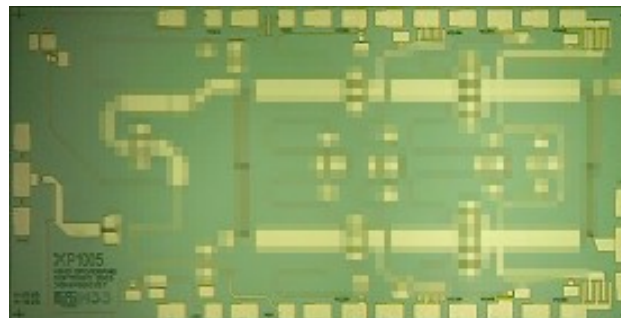
Features

- Excellent Saturated Output Stage
- Balanced Design Provides Good Output Match
- 26.0 dB Small Signal Gain
- +24.0 dBm Saturated Output Power
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's four stage 35.0-43.0 GHz GaAs MMIC power amplifier has a small signal gain of 26.0 dB with a +24.0 dBm saturated output power. The device also includes Lange couplers to achieve good output return loss. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	1050 mA
Gate Bias Voltage (Vg)	+0.3 V
Input Power (Pin)	+8.0 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to MTTF Table ¹
Channel Temperature (Tch)	MTTF Table ¹

1. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Ordering Information

Part Number	Package
XP1005-BD-000V	"V" - vacuum release gel paks
XP1005-BD-EV1	evaluation module

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Electrical Specifications: 35-43 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11) @ 37.0-40.0	dB	-	10.0	-
Output Return Loss (S22) @ 37.0-40.0	dB	-	15.0	-
Small Signal Gain (S21) @ 37.0-40.0	dB	23.0	26.0	-
Gain Flatness (ΔS_{21})	dB	-	+/-2.0	-
Reverse Isolation (S12) @ 37.0-40.0	dB	-	40.0	-
Saturated Output Power (Psat) @ 37.0-40.0	dBm	+23.0	+24.0	-
Drain Bias Voltage (Vd1,2,3,4)	VDC	-	+4.5	+5.5
Gate Bias Voltage (Vg1,2,3,4)	VDC	-1.0	-0.7	0.0
Supply Current (Id) (Vd=4.5 V, Vg=-0.7 V Typical)	mA	-	500	1000

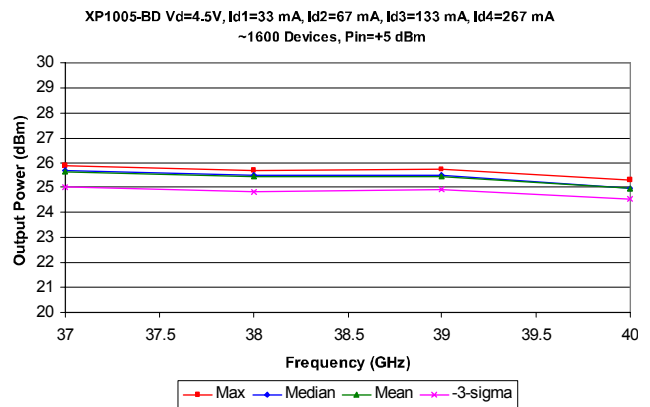
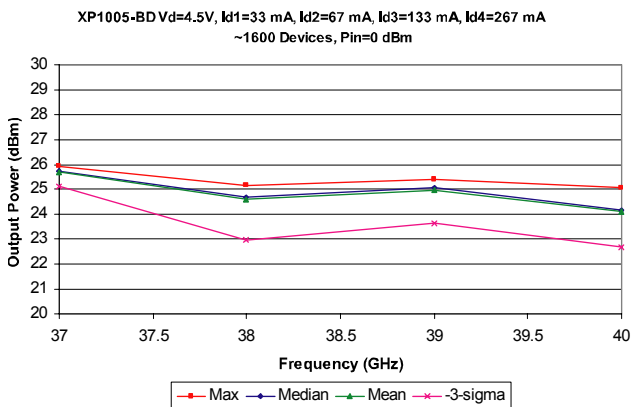
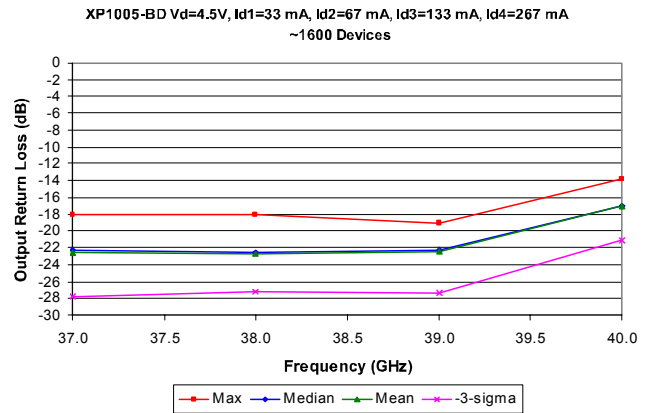
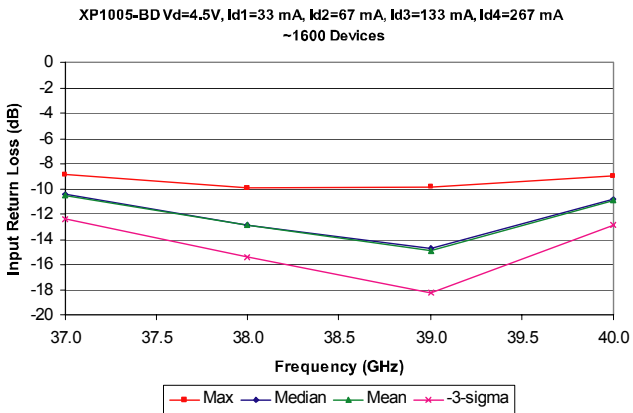
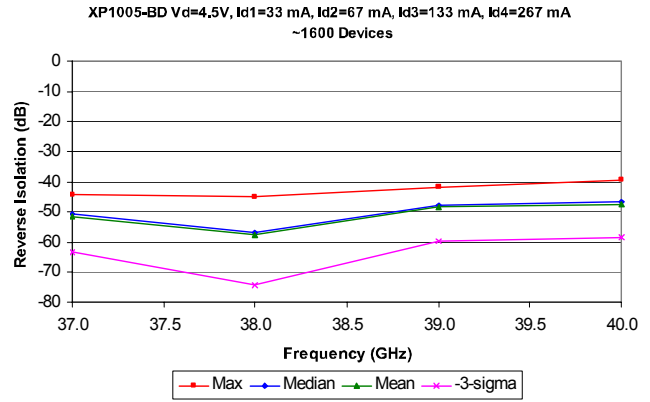
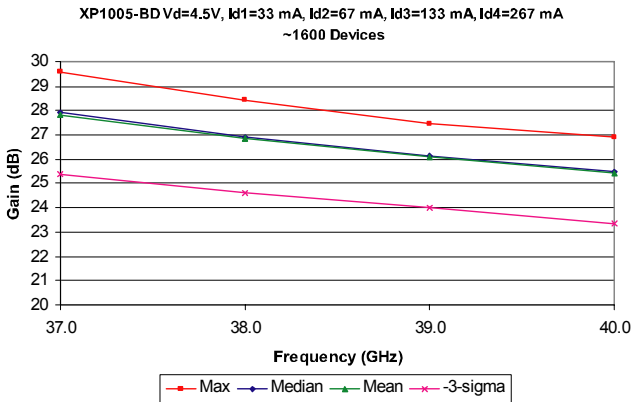
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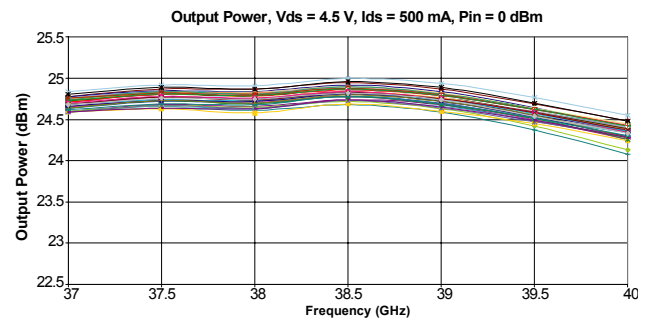
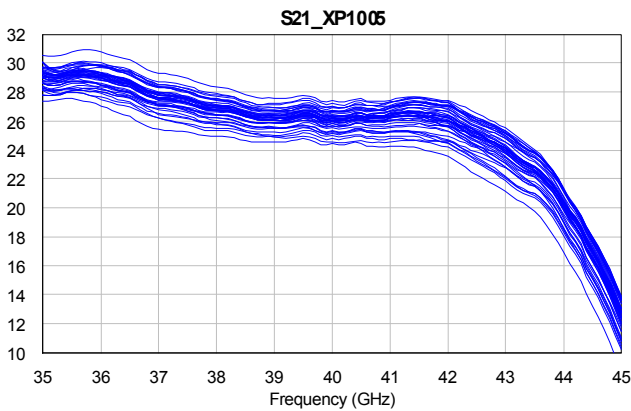
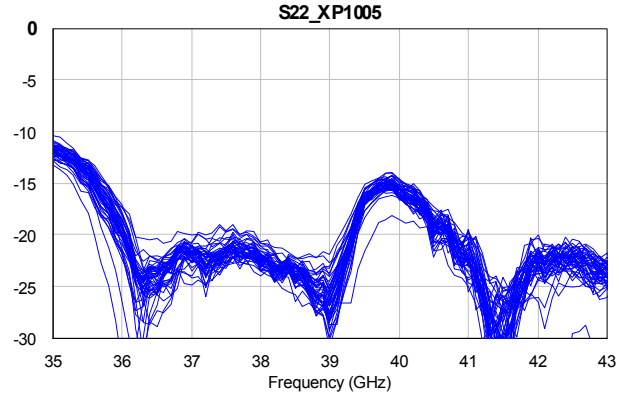
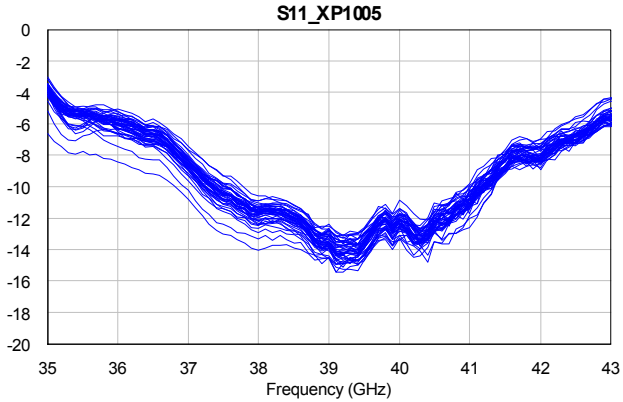
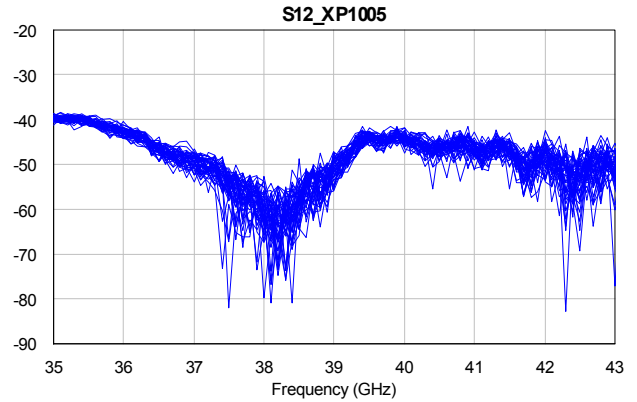
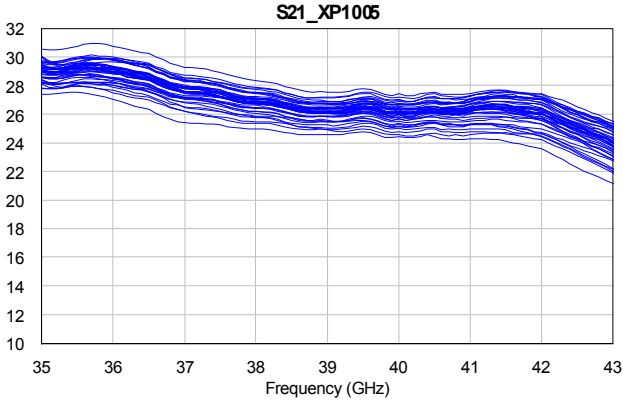
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Typical Performance Curves



Typical Performance Curves (cont.)



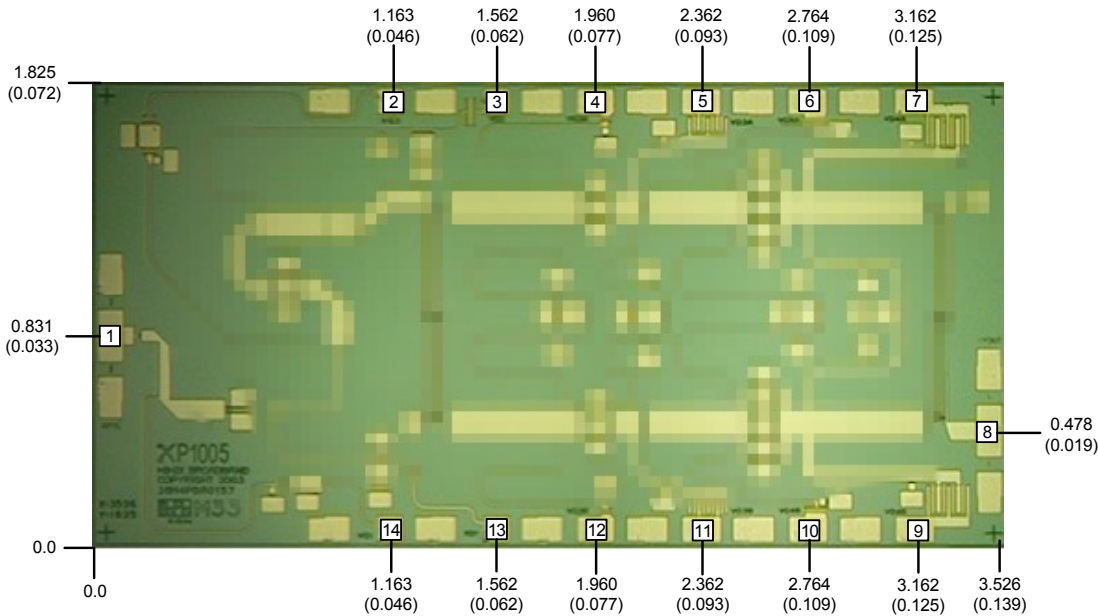
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Mechanical Drawing

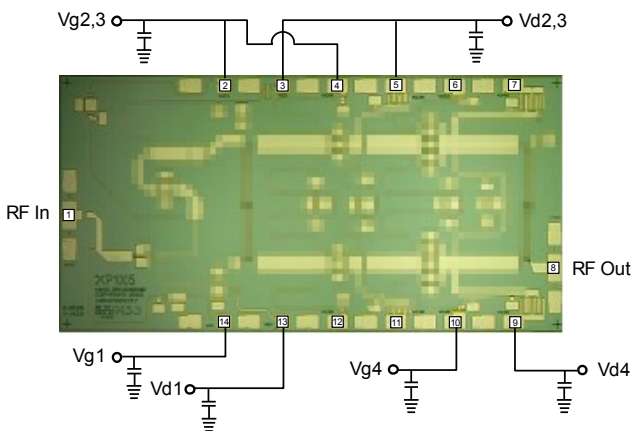


(Note: Engineering designator is 38H4PBA0157)

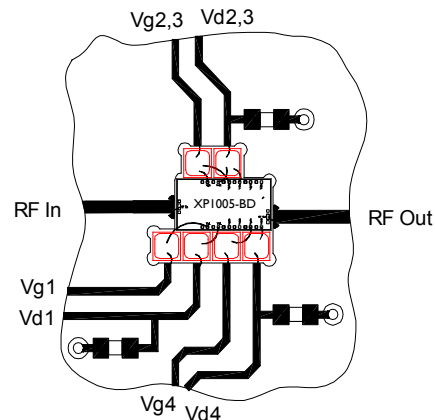
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
 Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
 All DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
 Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
 Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 3.987 mg.

- | | | | |
|---------------------|----------------------|---------------------|--------------------|
| Bond Pad #1 (RF In) | Bond Pad #5 (Vd3A) | Bond Pad #9 (Vd4B) | Bond Pad #13 (Vd1) |
| Bond Pad #2 (Vg2) | Bond Pad #6 (Vg4A) | Bond Pad #10 (Vg4B) | Bond Pad #14 (Vg1) |
| Bond Pad #3 (Vd2) | Bond Pad #7 (Vd4A) | Bond Pad #11 (Vd3B) | |
| Bond Pad #4 (Vg3A) | Bond Pad #8 (RF Out) | Bond Pad #12 (Vg3B) | |

Bias Arrangement



Bypass Capacitors - See App Note [2]



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MTTF Tables

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	133.8 deg Celsius	35.0° C/W	3.35E+08	2.99E+00
75 deg Celsius	159.1 deg Celsius	37.4° C/W	2.45E+07	4.08E+01
95 deg Celsius	184.0 deg Celsius	39.5° C/W	2.50E+06	4.01E+02

Bias Conditions: Vd1=Vd2=Vd3a(or Vd3b)=Vd4a(or Vd4b)=4.5V, Id1=35 mA, Id2=65 mA, Id3a/b=130 mA, Id4a/b=270 mA

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App Note [1] Biasing - It is recommended to separately bias each amplifier stage Vd1 through Vd4 at Vd (1,2,3,4)=4.5V with Id1=35mA, Id2=65mA, Id3=130mA and Id4=270mA. Separate biasing is recommended if the amplifier is to be used at high levels of saturation, where gate rectification will alter the effective gate control voltage. For non-critical applications it is possible to parallel all stages and adjust the common gate voltage for a total drain current Id(total)=500 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.7V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -

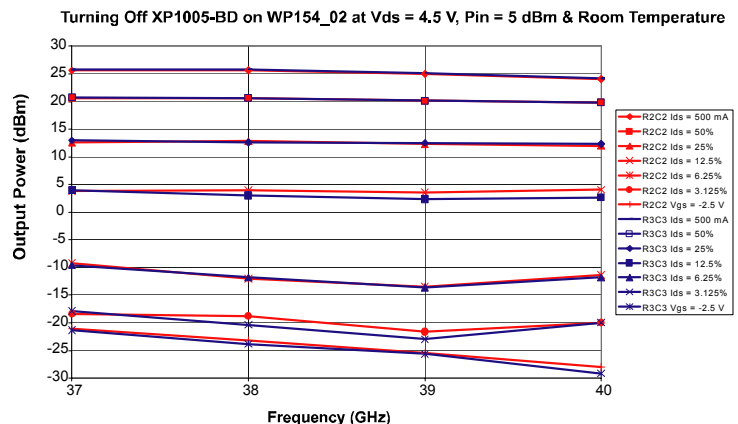
For Parallel Stage Bias (Recommended for general applications) -- The same as Individual Stage Bias but all the drain or gate pad DC bypass capacitors (~100-200 pF) can be combined. Additional DC bypass capacitance (~0.01 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads. The Vg3a/b, Vd3a/b, Vg4a/b and Vd4a/b pads have been tied together on chip and can be biased from either side. The unused Vg3a/b, Vd3a/b, Vg4a/b and Vd4a/b pads must be bypassed but can be left open.

For Individual Stage Bias (Recommended for saturated applications) -- Each DC pad (Vd1,2,3,4 and Vg1,2,3,4) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended. The Vg3a/b, Vd3a/b, Vg4a/b and Vd4a/b pads have been tied together on chip and can be biased from either side. The unused Vg3a/b, Vd3a/b, Vg4a/b and Vd4a/b pads must be bypassed but can be left open.

App Note [3] Output Power Adjust Using Gate Control - The XP1005 device has an interesting and very useful additional feature. The XP1005's output power can be adjusted by lowering the individual or combined gate voltages towards pinch off without sacrificing much in the way of Input 3rd Order Intercept Point. Improvements to the IIP3 and Noise Figure data shown here while attenuating the gain are also possible with individual gate control. Data here has been taken using combined gate control (all gates changed together) to lower the device's output power. The results are shown in the table below. Additionally, the accompanying curve shows the level and linearity of the typical attenuation achievable as the gate is adjusted at various levels until pinch-off.

Frequency: 40.0 GHz (worst case across 37.5-40.0 GHz) Pin: -19.0 dBm@scl Drain Voltage: 4.5 Volts
Id split: Vd1=35 mA, Vd2=65 mA, Vd3A=65.0 mA, Vd3B=65.0 mA, Vd4A=135 mA, Vd4B=135 mA

Gain (dB)	IM3 (dBc)	IIP3 (dBm)	NF (dB)
26.0	47.0	4.5	7.10
24.0	53.0	7.5	6.80
22.0	58.0	10.0	6.70
20.0	62.0	12.0	6.60
18.0	61.0	11.5	7.00
16.0	59.0	10.5	7.10
14.0	58.0	10.0	7.50
12.0	57.0	9.5	7.90
10.0	57.0	9.5	8.80
8.0	57.0	9.5	9.40

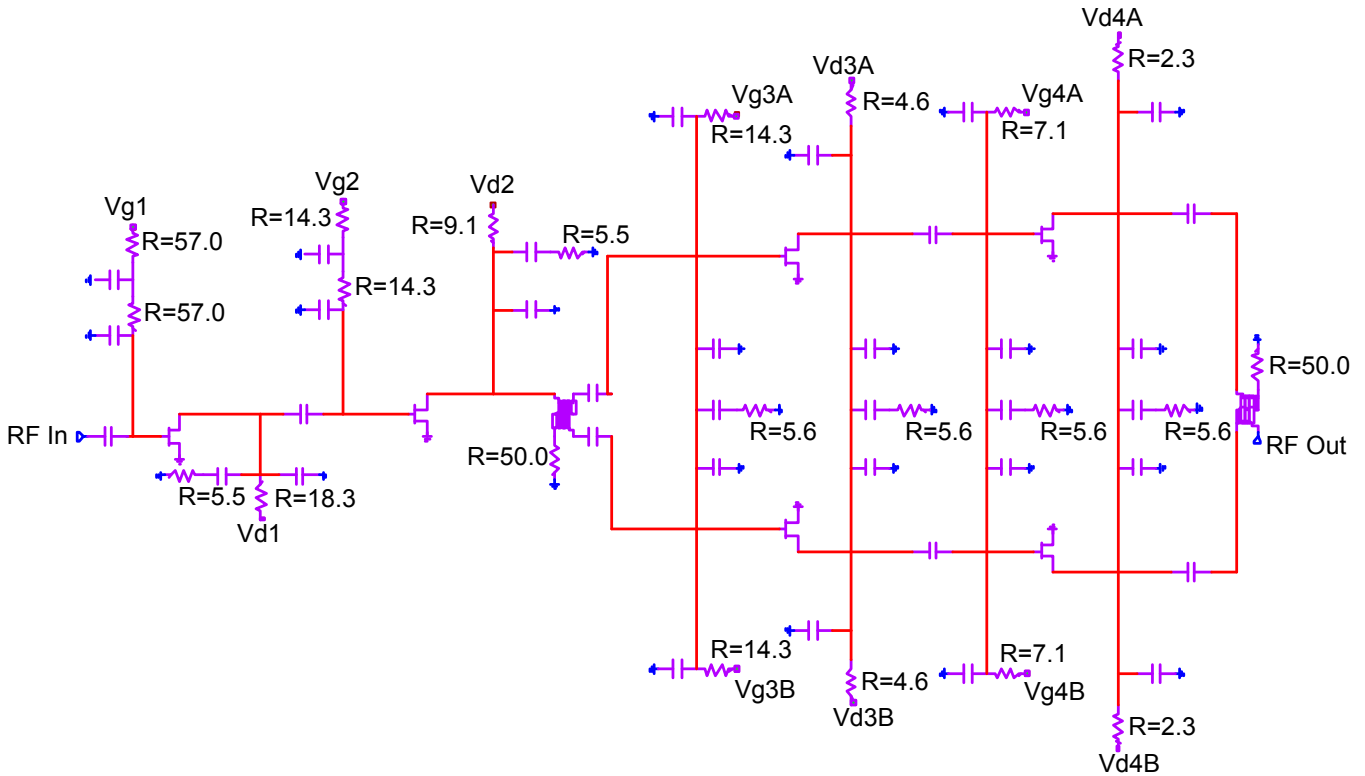


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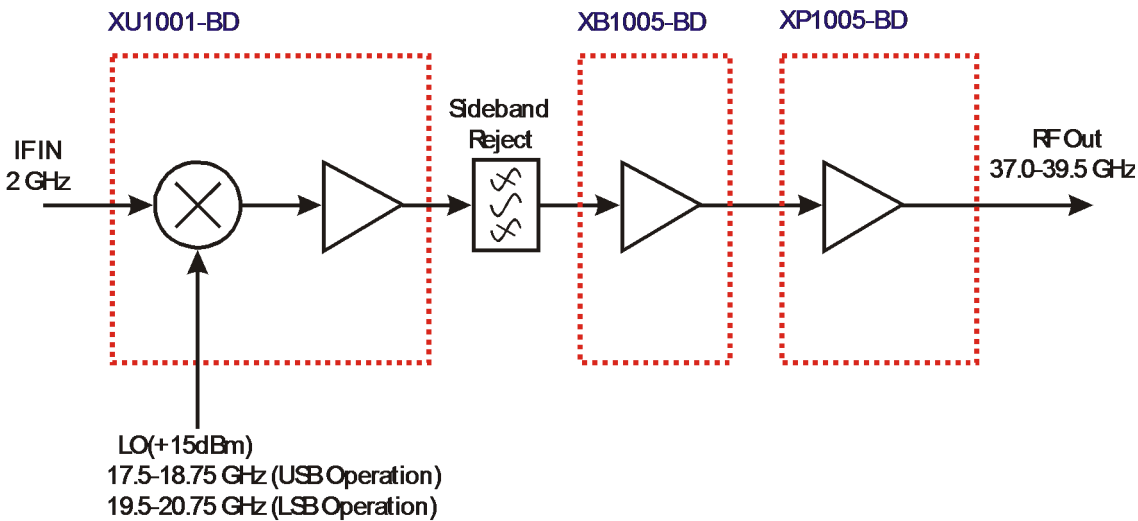
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Device Schematic



Typical Application



M/A-COM Tech MMIC-based 36.0-40.0 GHz Transmitter Block Diagram
(Changing LO and IF frequencies as required allows design to operate as high as 40 GHz)

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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.