XP1031-QK

Power Amplifier 37.0-40.0 GHz

Rev. V1

Mimix Broadband

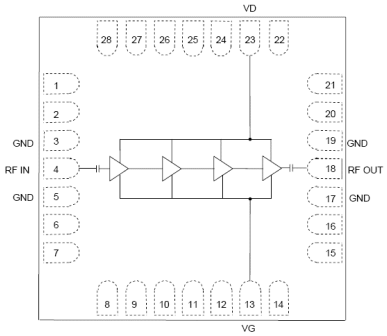
Features

- Linear Power Amplifier
- Output Power Adjust
- 25.0 dB Small Signal Gain
- +25.0 dBm P1dB Compression Point
- +35.5 dBm OIP3
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's four stage 37.0-40.0 GHz SMD GaAs MMIC power amplifier has a small signal gain of 25.0 dB with a +35.5 dBm Output Third Order Intercept. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The device comes in a RoHS compliant 7x7mm QFN Surface Mount Package offering excellent RF and thermal properties. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Functional Block Diagram/Board Layout



Pin Configuration

Pin No.	Function	Pin No.	Function
3	Ground	18	RF Output
4	RF Input	19	Ground
5	Ground	23	Drain bias for Stage 1-4
13	Gate bias for Stage 1-4	All other pins	Not Connected
17	Ground		

Ordering Information

Part Number	Package
XP1031-QK-0N00	bulk quantity
XP1031-QK-0N0T	tape and reel
XP1031-QK-EV1	XP1031-QK evaluation board

Absolute Maximum Ratings [1,2]

Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3V
Supply Current (Id)	800 mA
Gate Bias Voltage (Vg)	1.5V < Vg < 0V
Input Power (Pin)	+10 dBm
Abs. Max Junction/Channel Temp	MTTF Graph 1
Max. Operating Junction/Channel Temp	175 °C
Continuous Power Dissipation (Pdiss) at 85 °C	2.80 W
Thermal Resistance (Tchannel=150 °C)	23 °C/W
Operating Temperature (Ta)	-40 °C to +85 °C
Storage Temperature (Tstg)	-65 °C to +150 °C
Mounting Temperature	See solder reflow profile
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL3

(1) Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
(2) For saturated performance it is recommended that the sum of (2*Vdd + abs(Vgg)) <9V

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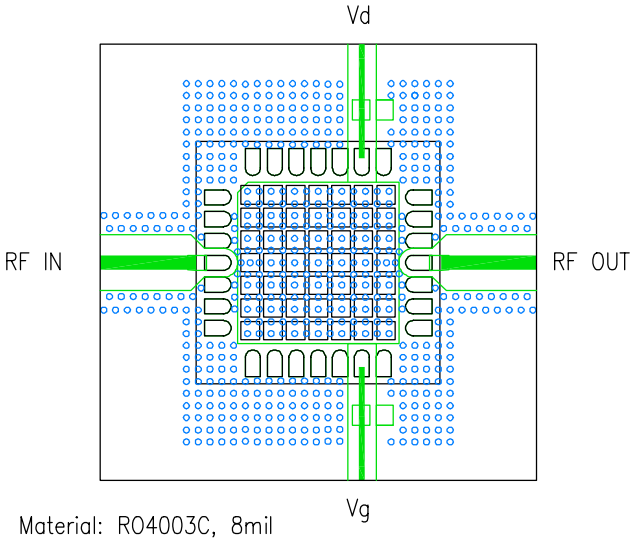
Visit www.macomtech.com for additional data sheets and product information.

Electrical Specifications: 37-40 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	10.0	14.0	-
Output Return Loss (S22)	dB	4.0	8.0	-
Small Signal Gain (S21)	dB	23.0	25.0	-
Gain Flatness (ΔS21)	dB	-	+/-1.0	-
Reverse isolation (S12)	dB	40	50	-
Output Power for 1dB Compression Point (P1dB)	dBm	-	25.0	-
Output IMD3 with Pout (scl) = 18 dBm	dBc	28.0	35.0	-
Output IMD3 with Pout (scl) = 15 dBm	dBc	38.0	41.0	-
Drain Bias Voltage (Vd)	VDC	-	3.5	4.0
Gate Bias Voltage (Vg)	VDC	-1.0	-0.3	-0.1
Supply Current (Id1) (Vd=4.0V, Vg=-0.3V)	mA	-	600	675

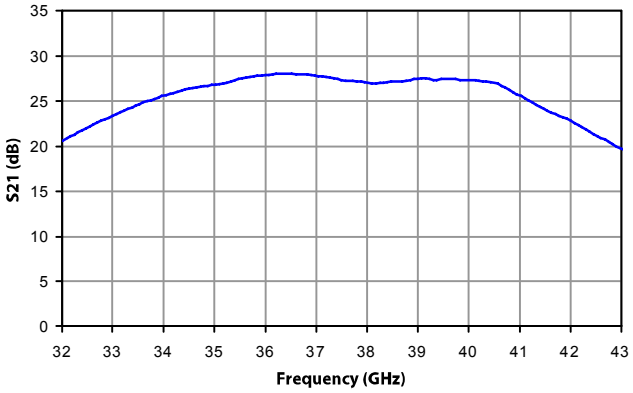
Recommended Layout



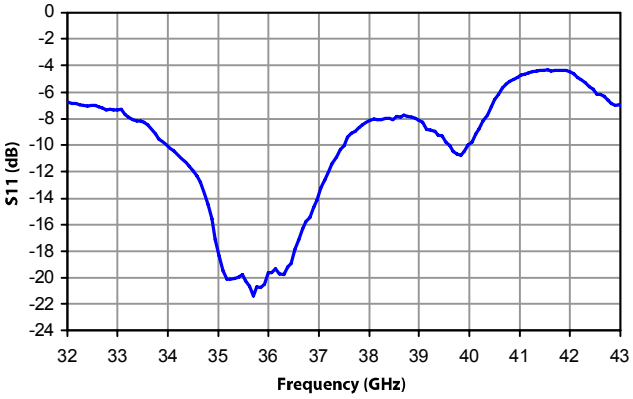
Material: RO4003C, 8mil
Capacitors: 10nF/1uF

Typical Performance Curves

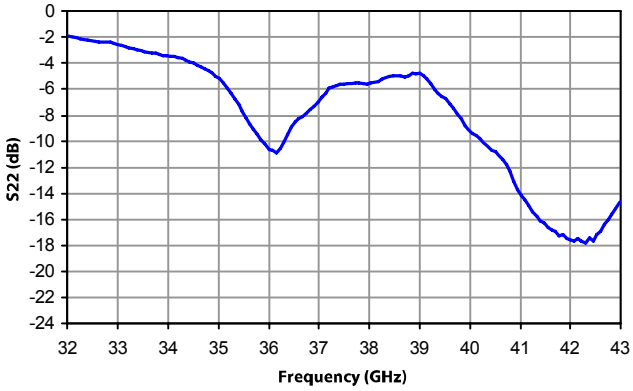
XP1031-QK-0N00: Small Signal Gain (S21)
Vd=4.0V, Id=600mA



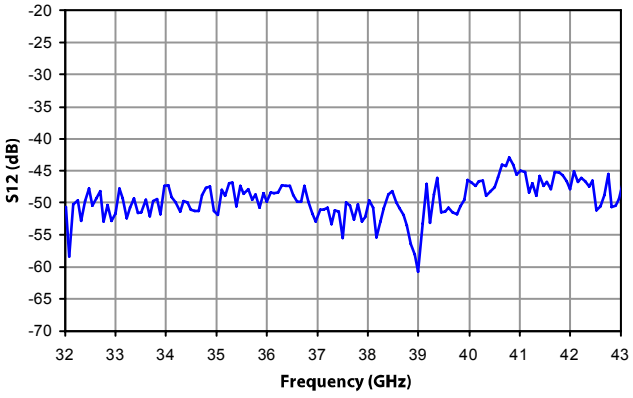
XP1031-QK-0N00: Input Return Loss (S11)
Vd=4.0V, Id=600mA



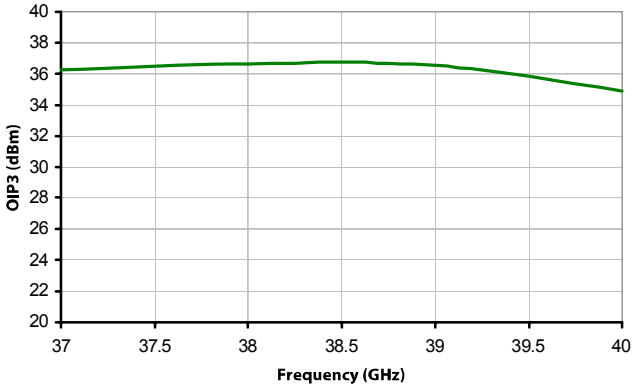
XP1031-QK-0N00: Output Return Loss (S22)
Vd=4.0V, Id=600mA



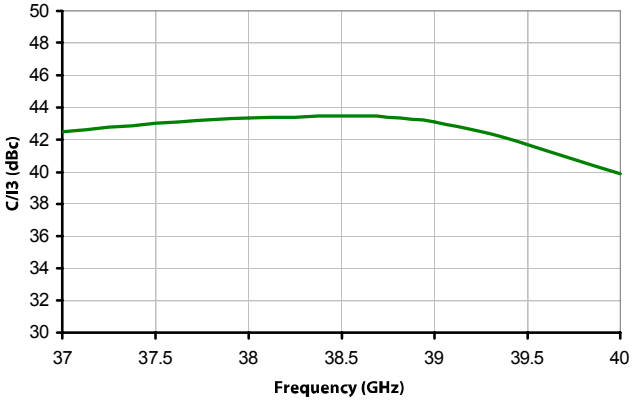
XP1031-QK-0N00: Reverse Isolation (S12)
Vd=4.0V, Id=600mA



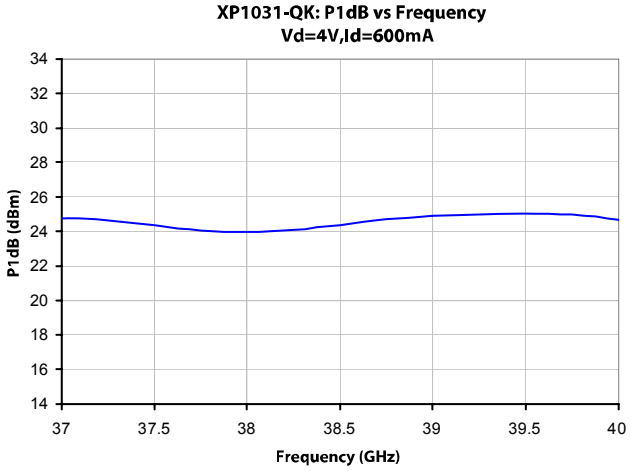
XP1031-QK-0N00: OIP3 vs Frequency
Pscl=15dBm,Vd=4V,Id=600mA

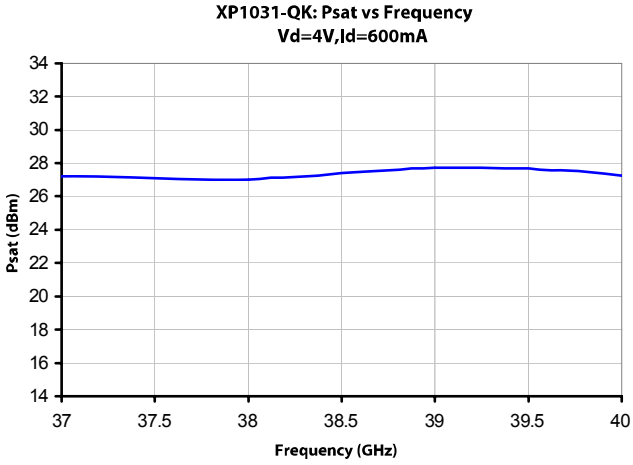


XP1031-QK-0N00: C/I3 vs Frequency
Pscl=15dBm,Vd=4V,Id=600mA



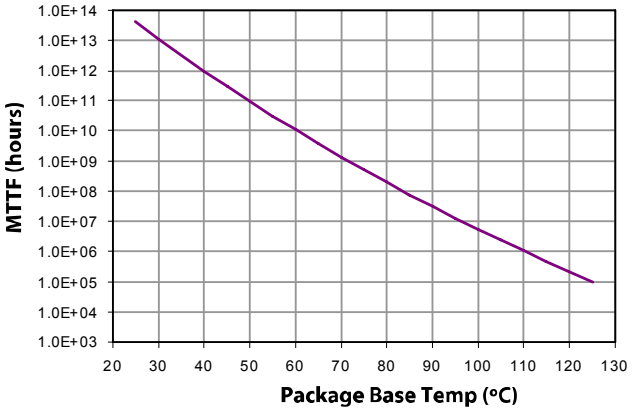
Typical Performance Curves



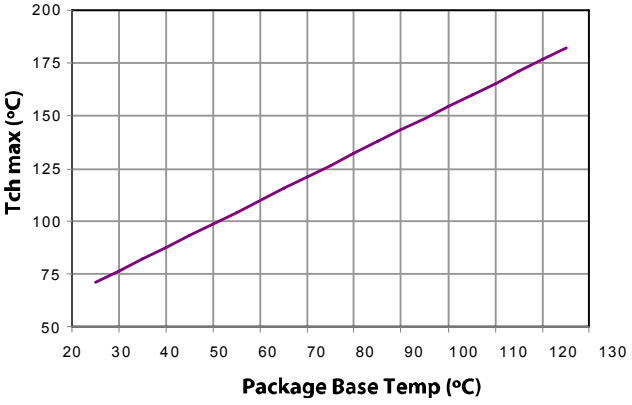


MTTF

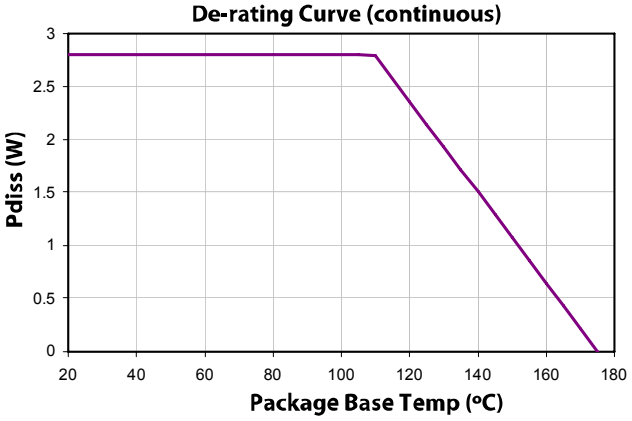
XP1031-QK: MTTF hours vs. Package Base Temperature
Vd=4V, Ids = 600 mA



XP1031-QK: Tch(max) vs. Package Base Temperature
Vd=4V, Ids = 600 mA



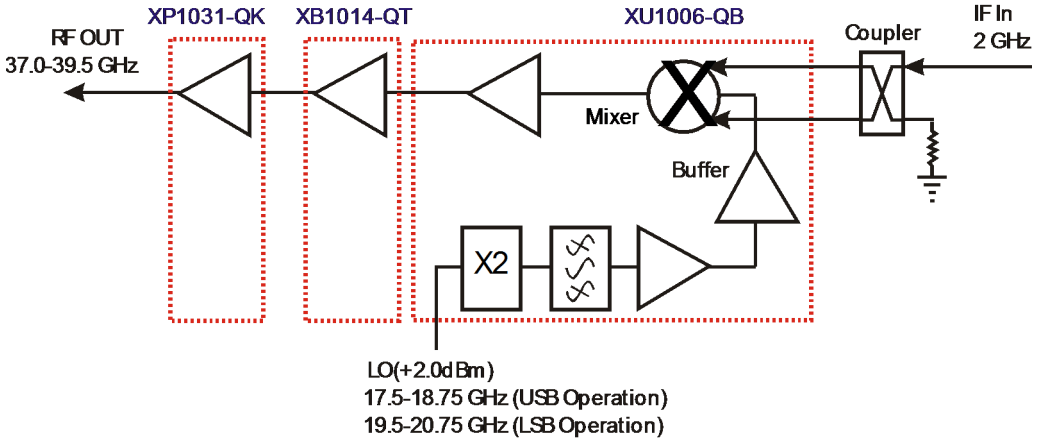
XP1031-QK-0N00: Operating Power De-rating Curve (continuous)



App Note [1] Biasing - It is recommended to bias the amplifier with Vd=4.0V and Id=600mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

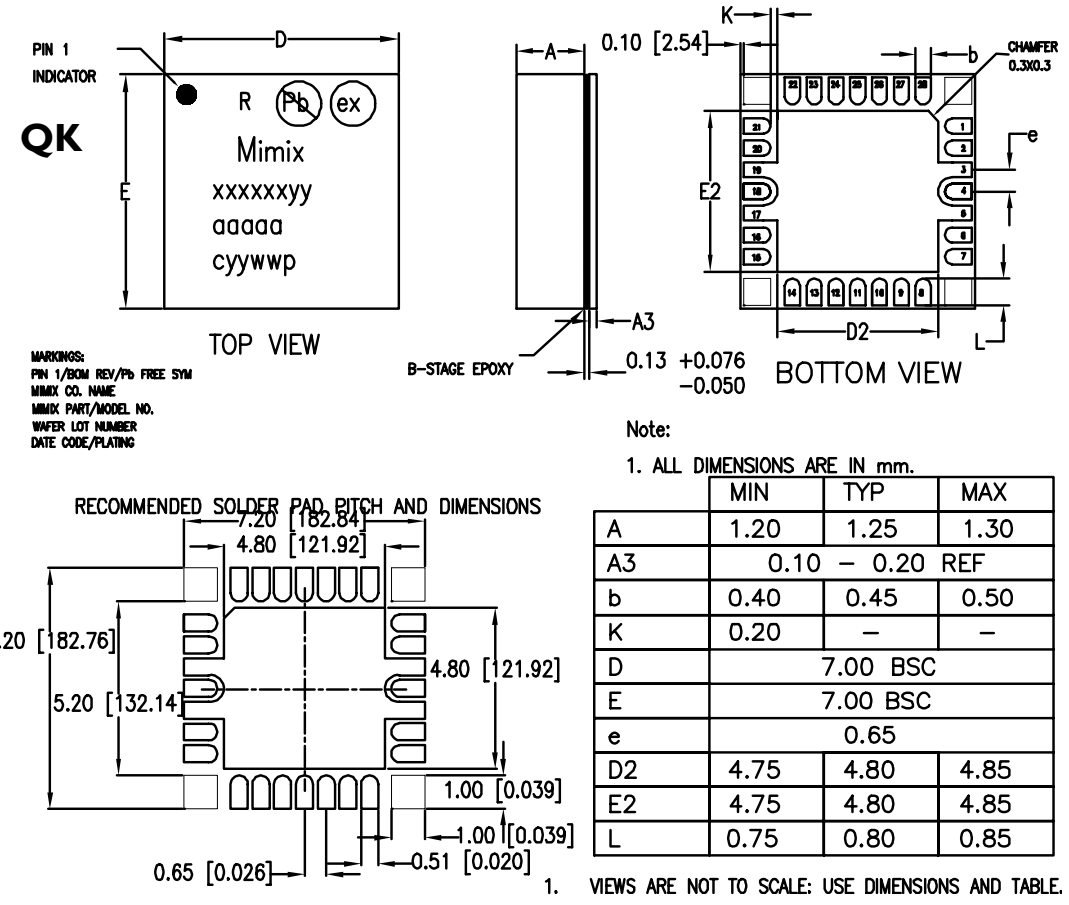
App Note [2] Bias Arrangement - Each DC pin (Vd and Vg) needs to have DC bypass capacitance (10 nF/1 uF) as close to the package as possible.

Typical Application



MMIC-based 37.0-40.0 GHz Transmitter Block Diagram

Lead-Free Package Dimensions/Layout



Note:

1. ALL DIMENSIONS ARE IN mm.

	MIN	TYP	MAX
A	1.20	1.25	1.30
A3	0.10 – 0.20 REF		
b	0.40	0.45	0.50
K	0.20	–	–
D	7.00 BSC		
E	7.00 BSC		
e	0.65		
D2	4.75	4.80	4.85
E2	4.75	4.80	4.85
L	0.75	0.80	0.85

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.