PM50CBS060

FEATURE

a) Adopting 4th generation IGBT chip, which performance is improved by 1μm fine rule process.
   For example, typical Vce(sat)=1.7V
b) Using new Diode which is designed to get soft reverse recovery characteristics.
c) Over-temperature protection by detecting Tj of the IGBT chips
- 3φ 50A, 600V Current-sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage
- Acoustic noise-less 3.7kW class inverter application

APPLICATION

Servo drives and other motor controls

**PACKAGE OUTLINES**   **Dimensions in mm**

φ5.5
MOUNTING HOLES

R7
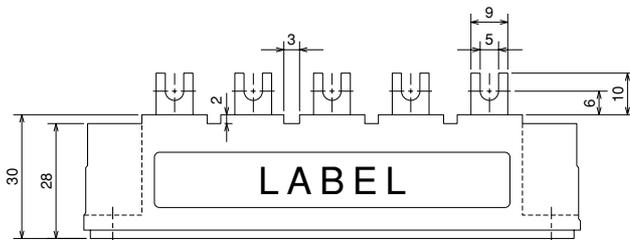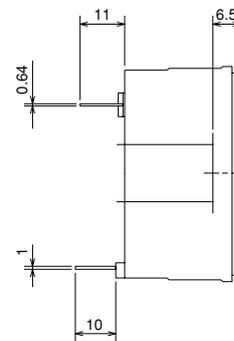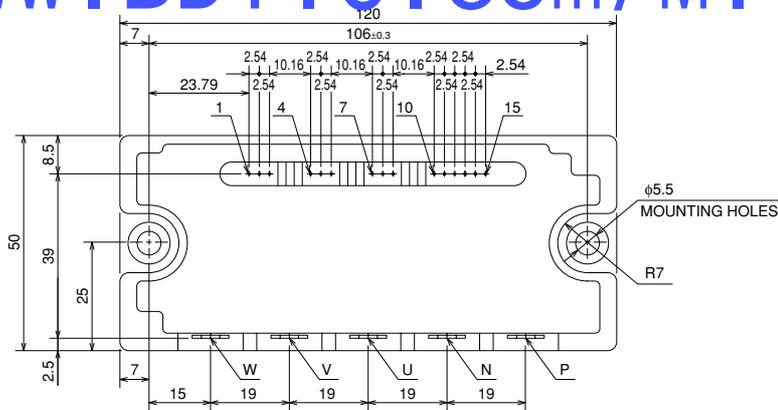
Terminal code

1. VWPC	9. VUP1
2. WP	10. VNC
3. VWP1	11. VN1
4. VVPC	12. WN
5. VP	13. VN
6. VVP1	14. UN
7. VUPC	15. Fo
8. UP	
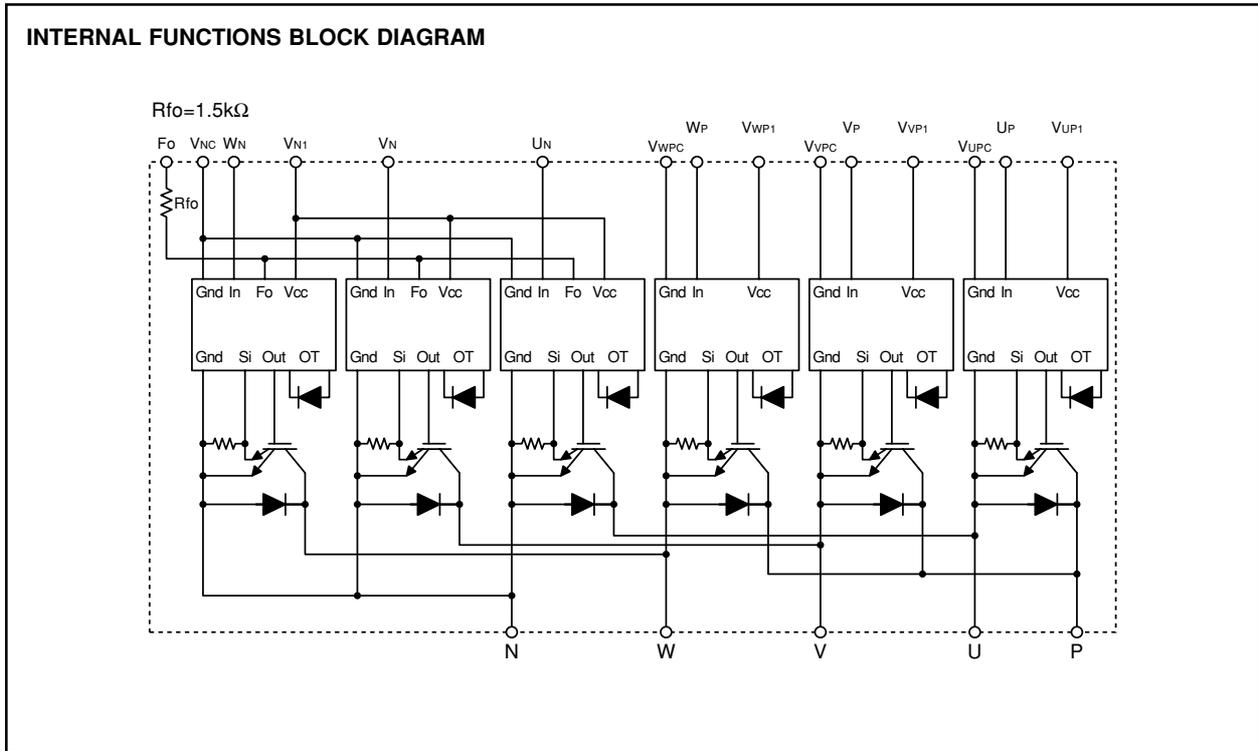
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**FLAT-BASE TYPE
INSULATED PACKAGE**

INTERNAL FUNCTIONS BLOCK DIAGRAM

Rfo=1.5kΩ

MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)
INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	$V_D = 15V$, $V_{CIN} = 15V$	600	V
$\pm I_C$	Collector Current	$T_C = 25°C$	50	A
$\pm I_{CP}$	Collector Current (Peak)	$T_C = 25°C$	100	A
P_C	Collector Dissipation	$T_C = 25°C$	152	W
T_j	Junction Temperature		$-20 \sim +150$	°C

CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
V_D	Supply Voltage	Applied between : V_{UP1}-V_{UPC} V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC} W_P-V_{WPC}, $U_N \cdot V_N \cdot W_N$-V_{NC}	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : F_O-V_{NC}	$V_D+0.5$	V
I_{FO}	Fault Output Current	Sink current at F_O terminal	20	mA

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FLAT-BASE TYPE
INSULATED PACKAGE

TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by OC & SC	V_D = 13.5 ~ 16.5V, Inverter Part, T_j = 125°C Start	400	V
$V_{CC(surge)}$	Supply Voltage (Surge)	Applied between : P-N, Surge value	500	V
T_C	Module Case Operating Temperature	(Note-1)	−20 ~ +110	°C
T_{stg}	Storage Temperature		−40 ~ +125	°C
V_{iso}	Isolation Voltage	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	V_{rms}

(Note-1) Tc(under the chip) measurement point is below.

(Unit : mm)

Arm Axis	U_P		V_P		W_P		U_N		V_N		W_N	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	83.3	83.3	41.8	41.8	16.8	16.8	70.8	70.8	54.3	54.3	29.3	29.3
Y	2.7	−3.8	2.7	−3.8	2.7	−3.8	−3.4	−9.8	−3.4	−9.8	−3.4	−9.8

Bottom view

P N U V W
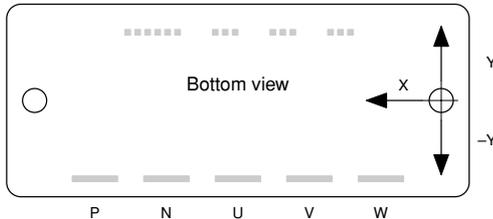
THERMAL RESISTANCES

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c')Q}$	Junction to case Thermal Resistances	Tc measured point is just under the chips Inverter IGBT part (per 1/6 module)	—	—	0.82*	°C/W
$R_{th(j-c')F}$		Tc measured point is just under the chips Inverter FWDi part (per 1/6 module)	—	—	1.51*	°C/W
$R_{th(c-f)}$	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	—	—	0.046	°C/W

*: If you use this value, $R_{th(f-a)}$ should be measured just under the chips.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)
INVERTER PART

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_D = 15V, I_C = 50A V_{CIN} = 0V, Pulsed (Fig. 1)	T_j = 25°C	—	1.7	2.3	V
			T_j = 125°C	—	1.7	2.3	
V_{EC}	FWDi Forward Voltage	−I_C = 50A, V_D = 15V, V_{CIN} = 15V (Fig. 2)		—	2.2	3.3	V
t_{on}	Switching Time	V_D = 15V, V_{CIN} = 15V↔0V V_{CC} = 300V, I_C = 50A T_j = 125°C Inductive Load (Fig. 3)		0.8	1.2	2.4	µs
t_{rr}				—	0.15	0.3	µs
$t_{c(on)}$				—	0.4	1.0	µs
t_{off}				—	2.4	3.3	µs
$t_{c(off)}$				—	0.5	1.0	µs
I_{CES}	Collector-Emitter Cutoff Current	V_{CE} = V_{CES}, V_D = 15V (Fig. 4)	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

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FLAT-BASE TYPE
INSULATED PACKAGE

CONTROL PART

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
ID	Circuit Current	VD = 15V, VCIN = 15V	VN1-VNC	—	40	60	mA
			VXP1-VXPC	—	13	18	
Vth(ON)	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC		1.2	1.5	1.8	V
Vth(OFF)	Input OFF Threshold Voltage	UN • VN • WN-VNC		1.7	2.0	2.3	V
OC	Over Current Trip Level	VD = 15V (Fig. 5,6)	Tj = −20°C	—	—	180	A
			Tj = 25°C	85	110	150	
			Tj = 125°C	65	—	—	
SC	Short Circuit Trip Level	−20≤ Tj ≤ 125°C, VD = 15V (Fig. 5,6)		—	132	—	A
toff(OC)	Over Current Delay Time	VD = 15V (Fig. 5,6)		—	10	—	μs
OT	Over Temperature protection	Detect Tj of IGBT chip	Trip level	135	145	155	°C
OTr			Reset level	—	125	—	°C
UV	Supply Circuit Under-Voltage Protection	−20 ≤ Tj ≤ 125°C	Trip level	11.5	12.0	12.5	V
UVr			Reset level	—	12.5	—	V
IFO(H)	Fault Output Current	VD = 15V, VFO = 15V (Note-2)		—	—	0.01	mA
IFO(L)				—	10	15	mA
tFO	Minimum Fault Output Pulse Width	VD = 15V (Note-2)		1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal OC, SC, OT & UV protection.
Fault output of OC, SC, OT & UV protection operate by lower arm.
Fault output of OC, SC protection given pulse.
Fault output of OT, UV protection given pulse while over trip level.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
—	Mounting torque	Main terminal	screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part	screw : M5	2.5	3.0	3.5	N • m
—	Weight	—		—	400	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Conditions	Recommended value	Unit
VCC	Supply Voltage	Applied across P-N terminals	≤ 400	V
VD	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC (Note-3)	15.0 ± 1.5	V
VCIN(ON)	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC	≤ 0.8	V
VCIN(OFF)	Input OFF Voltage	UN • VN • WN-VNC	≥ 4.0	V
fPWM	PWM Input Frequency	Using Application Circuit of Fig.8	≤ 20	kHz
tdead	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

(Note-3) With ripple satisfying the following conditions
dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

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PRECAUTIONS FOR TESTING

1. Before appling any control supply voltage (VD), the input terminals should be pulled up by resistores, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.

2. When performing "OC" and "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above VCES rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)
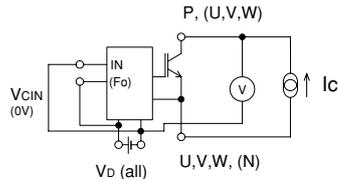
Fig. 1 VCE(sat) Test
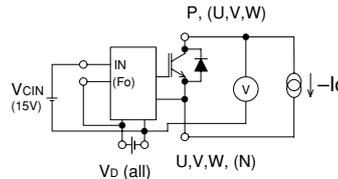
Fig. 2 VEC Test

a) Lower Arm Switching
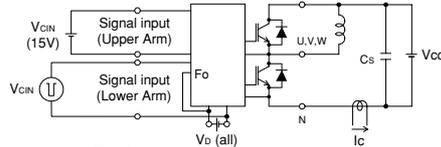
b) Upper Arm Switching
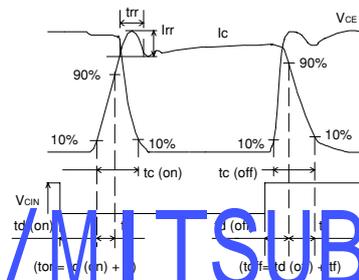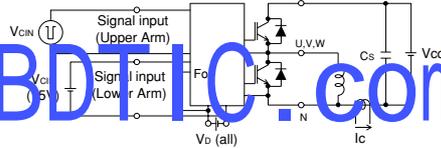
Fig. 3 Switching time Test circuit and waveform
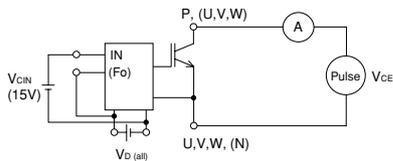
Fig. 4 ICES Test
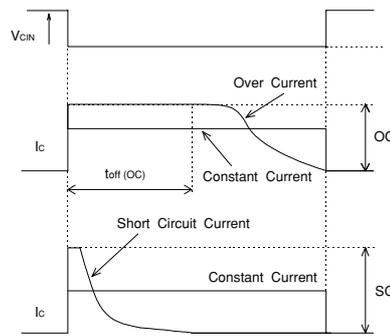
Fig. 5 OC and SC Test

Fig. 6 OC and SC Test waveform
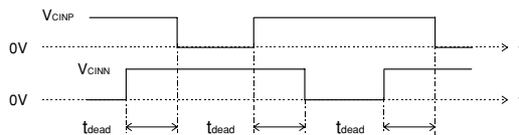
Fig. 7 Dead time measurement point example

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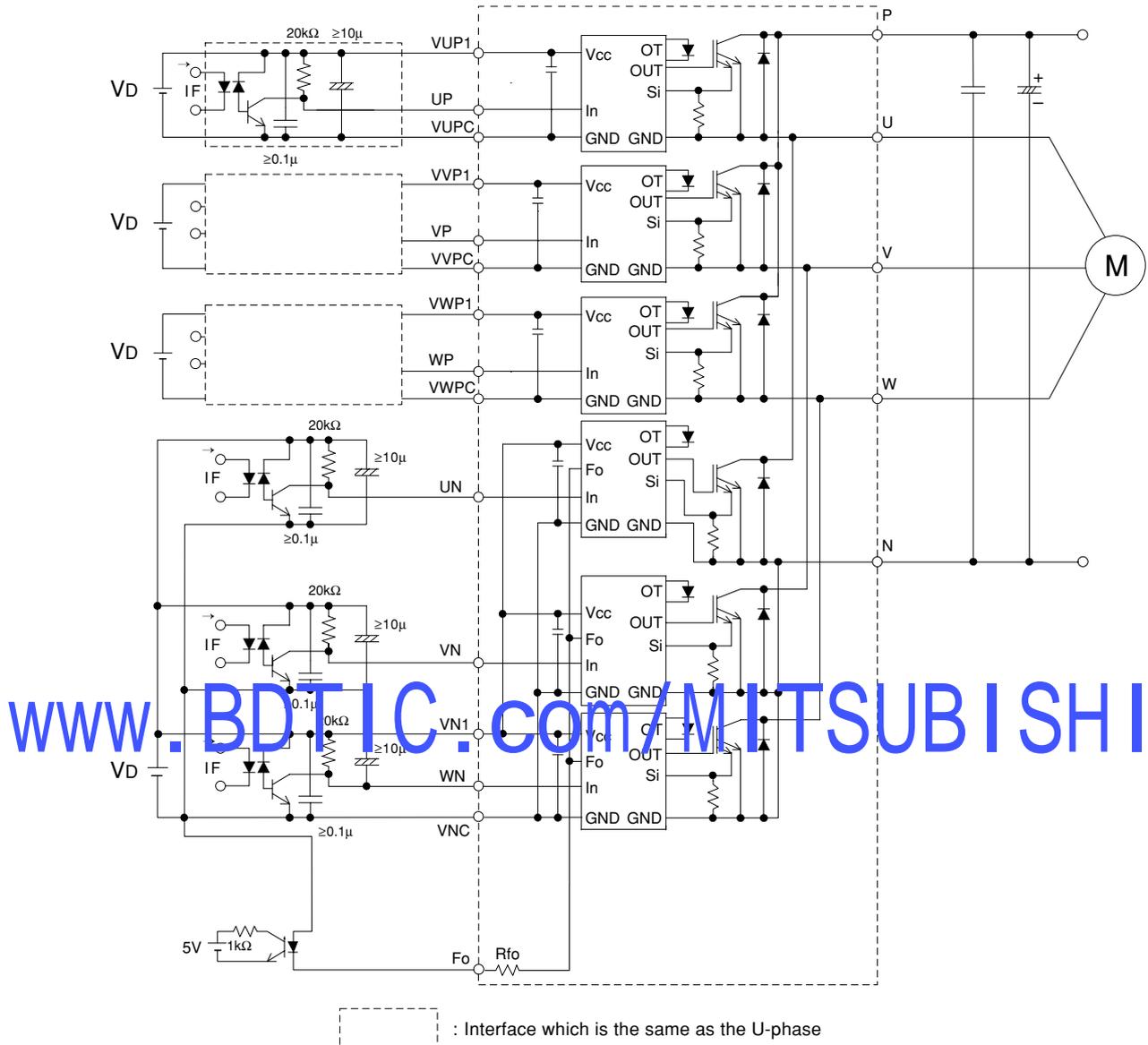
Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : tPLH, tPHL ≤ 0.8μs, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

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