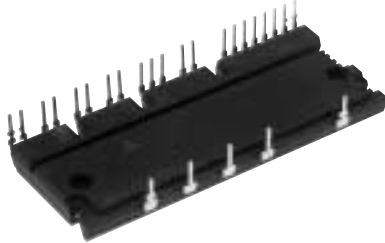


PS21869-P/AP

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21869



INTEGRATED POWER FUNCTIONS

600V/50A CSTBT inverter bridge for three phase
DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

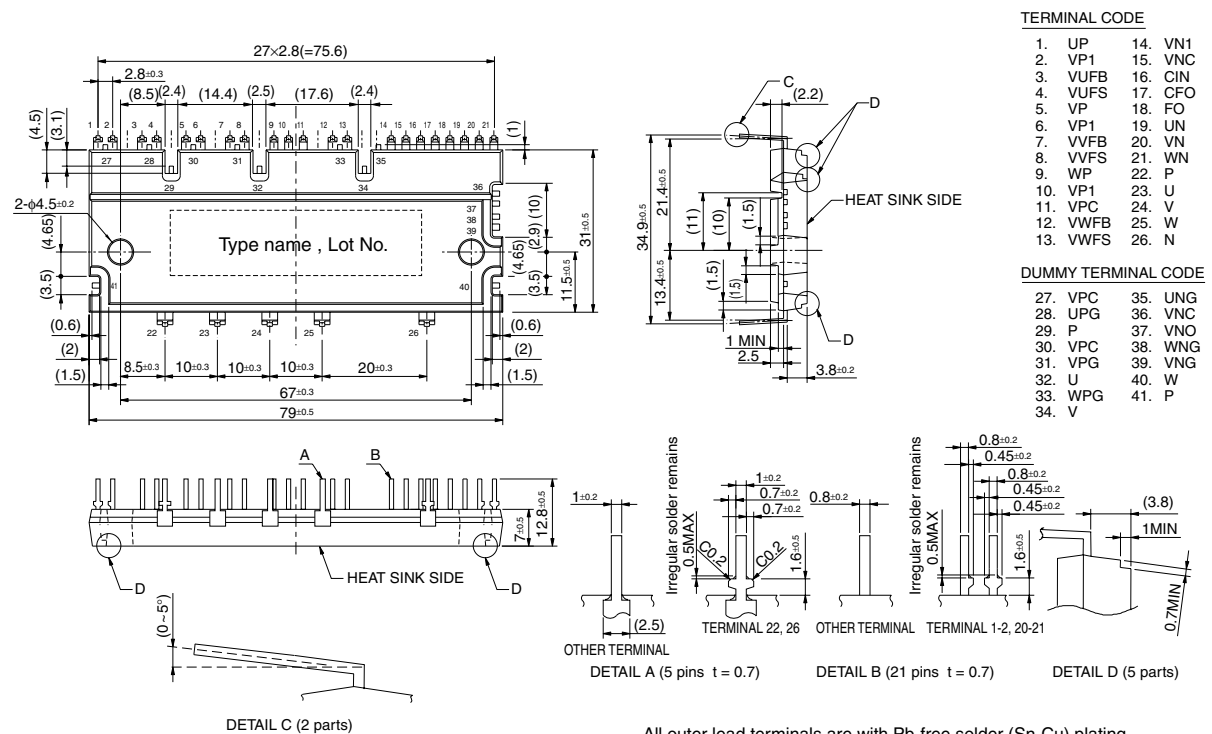
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3, 5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (Short-pin type : PS21869-P) Refer Fig. 6 for long-pin type : PS21869-AP.

Dimensions in mm



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-N	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-N	500	V
V _{CES}	Collector-emitter voltage		600	V
±I _C	Each IGBT collector current	T _f = 25°C	50	A
±I _{CP}	Each IGBT collector current (peak)	T _f = 25°C, less than 1ms	100	A
P _C	Collector dissipation	T _f = 25°C, per 1 chip	70.4	W
T _j	Junction temperature	(Note 1)	-20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ T_f ≤ 100°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to T_{j(ave)} ≤ 125°C (@ T_f ≤ 100°C).

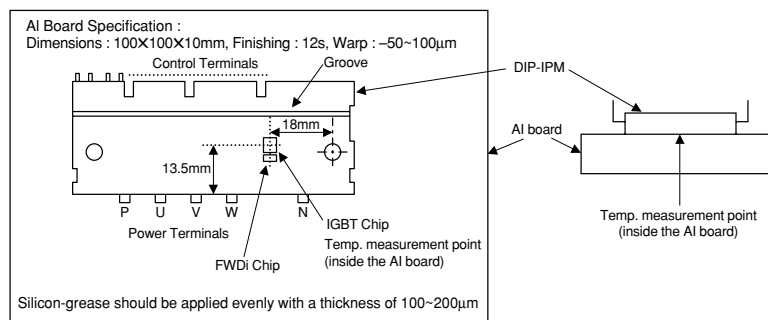
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between Fo-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at Fo terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(PROT)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part T _j = 125°C, non-repetitive, less than 2 μs	400	V
T _f	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	V _{rms}

Note 2 : T_f measurement point



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THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-f)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	1.42	°C/W
$R_{th(j-f)F}$		Inverter FWDi part (per 1/6 module)	—	—	2.00	°C/W

Note 3 : Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15V$ $V_{IN} = 5V$	—	1.50	2.00	V
V_{EC}	FWDi forward voltage	$T_j = 25^\circ C, -I_C = 50A, V_{IN} = 0V$	—	1.70	2.20	V
t_{on}	Switching times	$V_{CC} = 300V, V_D = V_{DB} = 15V$ $I_C = 50A, T_j = 125^\circ C, V_{IN} = 0 \leftrightarrow 5V$ Inductive load (upper-lower arm)	0.70	1.30	1.90	μs
t_{rr}			—	0.30	—	μs
$t_{c(on)}$			—	0.40	0.60	μs
t_{off}			—	2.00	2.60	μs
$t_{c(off)}$			—	0.65	0.90	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$ $T_j = 25^\circ C$	—	—	1	mA
		$T_j = 125^\circ C$	—	—	10	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_D	Circuit current	$V_D = V_{DB} = 15V$ $V_{IN} = 5V$	—	—	7.00	mA
		Total of V_{P1-VPC}, V_{N1-VNC}	—	—	0.55	mA
		$V_D = V_{DB} = 15V$ $V_{IN} = 0V$	—	—	7.00	mA
		Total of V_{P1-VPC}, V_{N1-VNC}	—	—	0.55	mA
V_{FOH}	Fault output voltage	$V_{SC} = 0V, F_o$ circuit pull-up to 5V with 10kΩ	4.9	—	—	V
V_{FOL}		$V_{SC} = 1V, I_{FO} = 1mA$	—	—	0.95	V
$V_{SC(ref)}$	Short circuit trip level	$T_f = -20 \sim 100^\circ C, V_D = 15V$ (Note 4)	0.45	—	0.52	V
I_{IN}	Input current	$V_{IN} = 5V$	1.0	1.5	2.0	mA
UV_{DBt}	Control supply under-voltage protection	$T_j \leq 125^\circ C$	10.0	—	12.0	V
UV_{DBr}			10.5	—	12.5	V
UV_{Dt}			10.3	—	12.5	V
UV_{Dr}			10.8	—	13.0	V
t_{FO}	Fault output pulse width	$C_{FO} = 22nF$ (Note 5)	1.0	1.8	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	2.1	2.3	2.6	V
$V_{th(off)}$	OFF threshold voltage		0.8	1.4	2.1	V

Note 4 : Short circuit protection is functioning only for the low-arms. Please select the external shunt resistor such that the SC trip-level is less than 2.0 times of the current ratings.

5 : Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO} [F]$.

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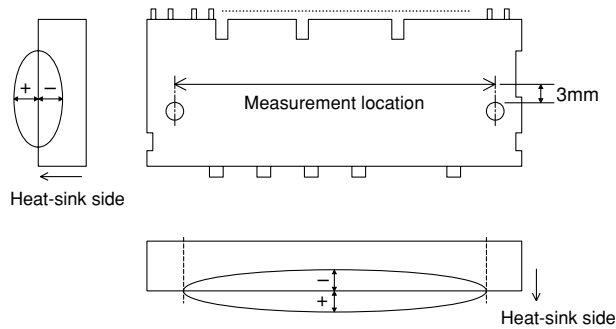
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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4 Recommended : 1.18 N·m	0.98	—	1.47	N·m
Weight		—	65	—	g
Heat-sink flatness	(Note 6)	-50	—	100	μm

Note 6 : Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Recommended value			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.0	15.0	18.5	V
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs
t _{dead}	Arm shoot-through blocking time	For each input signal, T _f ≤ 100°C	2	—	—	μs
f _{PWM}	PWM input frequency	T _f ≤ 100°C, T _j ≤ 125°C	—	—	20	kHz
I _O	Allowable r.m.s. current	V _{CC} = 300V, V _D = V _{DB} = 15V, P.F = 0.8, sinusoidal output T _f ≤ 100°C, T _j ≤ 125°C (Note 7)	—	—	23.6	Arms
		f _{PWM} = 5kHz	—	—	23.6	
		f _{PWM} = 15kHz	—	—	13.8	
PW _{IN(on)}		(Note 8)	0.3	—	—	μs
PW _{IN(off)}	Allowable minimum input pulse width	200 ≤ V _{CC} ≤ 350V, 13.5 ≤ V _D ≤ 16.5V, 13.0 ≤ V _{DB} ≤ 18.5V, -20°C ≤ T _f ≤ 100°C, N-line wiring inductance less than 10nH (Note 9)	Below rated current	3.0	—	
			Between rated current and 1.7 times of rated current	5.0	—	
			Between 1.7 times and 2.0 times of rated current	5.9	—	
V _N	V _N variation	between V _N -N (including surge)	-5.0	—	5.0	V

Note 7 : The allowable r.m.s. current value depends on the actual application conditions.

8 : The input pulse width less than PW_{IN(on)} might make no response.

9 : IPM might make delayed response (less than 2μsec) or no response for the input signal with off pulse width less than PW_{IN(off)}. Please refer Fig. 4 for details.

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Fig. 4 CURRENT OUTPUT WHEN INPUT SIGNAL IS LESS THAN ALLOWABLE MINIMUM INPUT PULSE WITH PWIN(off) (P-side only)

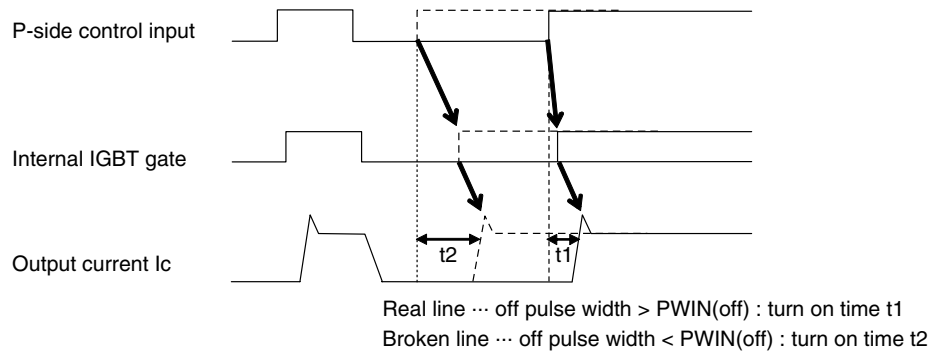
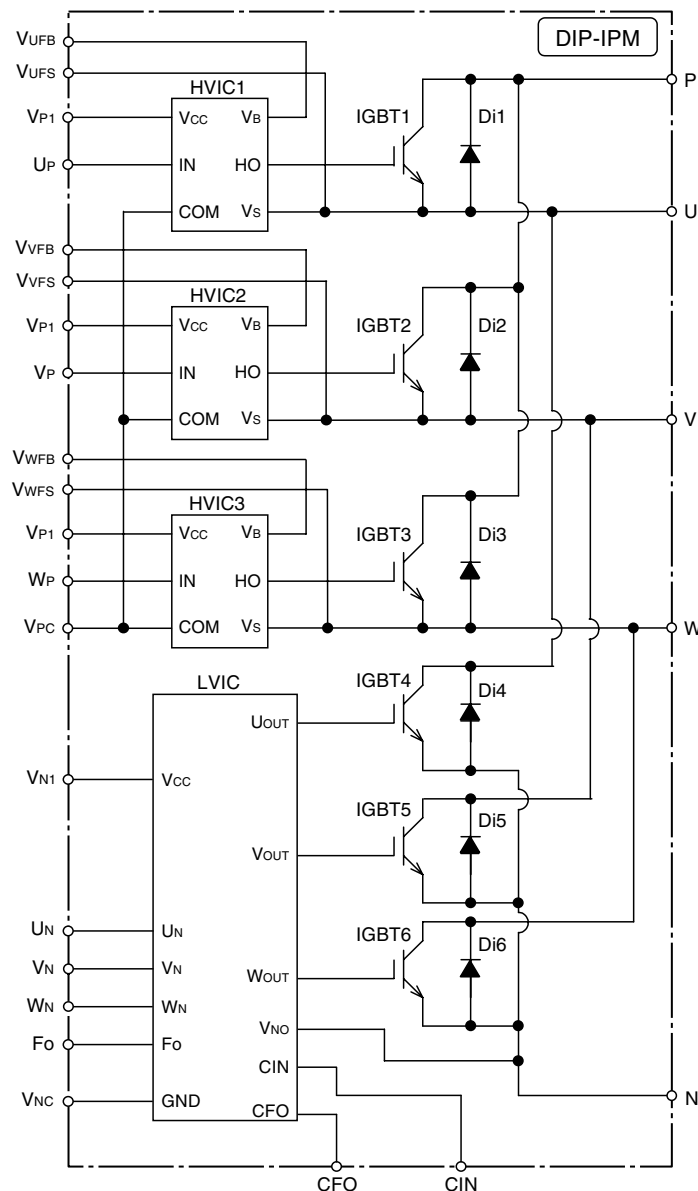


Fig. 5 THE DIP-IPM INTERNAL CIRCUIT

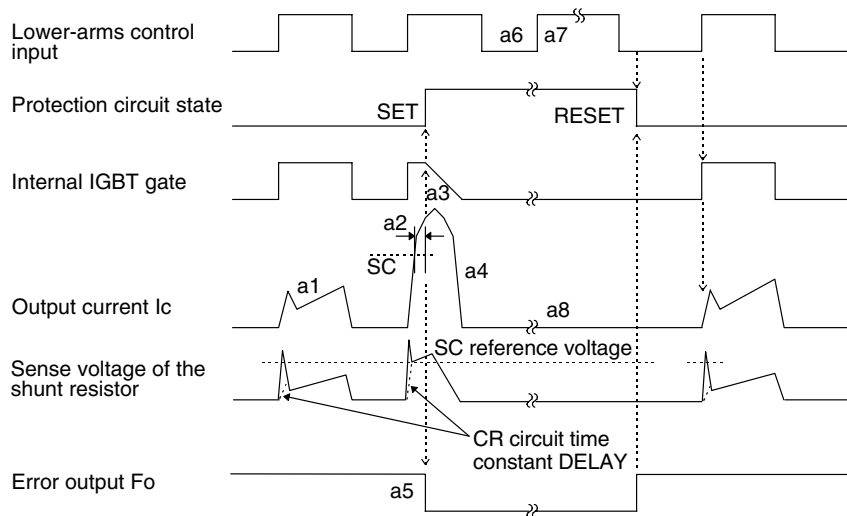


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Fig. 7 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

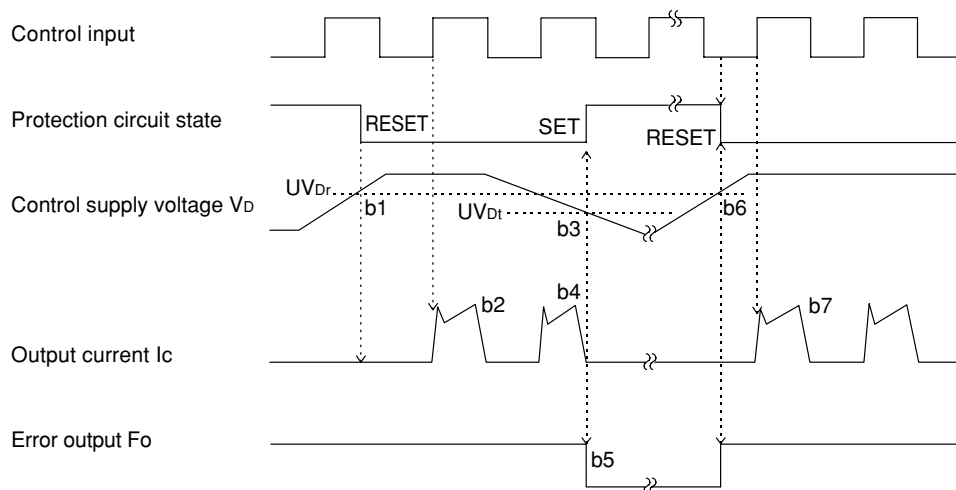
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. FO timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a6. Input "L" : IGBT OFF.
- a7. Input "H" : IGBT ON.
- a8. IGBT OFF in spite of input "H".



[B] Under-Voltage Protection (Lower-arm, UVd)

- b1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. FO operation starts.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-arm, UVDB)

- c1. Control supply voltage rises : Operation starts soon after UVDBr.
- c2. Protection circuit state reset : IGBT ON : Currents output.
- c3. Normal operation : IGBT ON and carrying current.
- c4. Under voltage trip (UVDBt).
- c5. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- c6. Under voltage reset (UVDBr).
- c7. Normal operation : IGBT ON and carrying current.

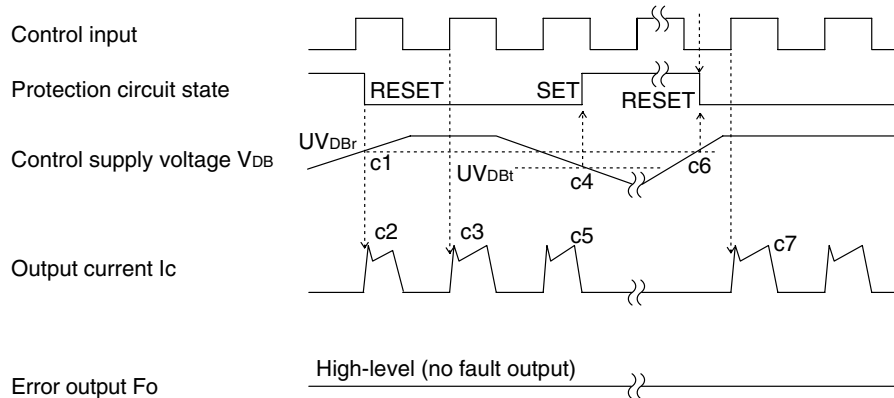
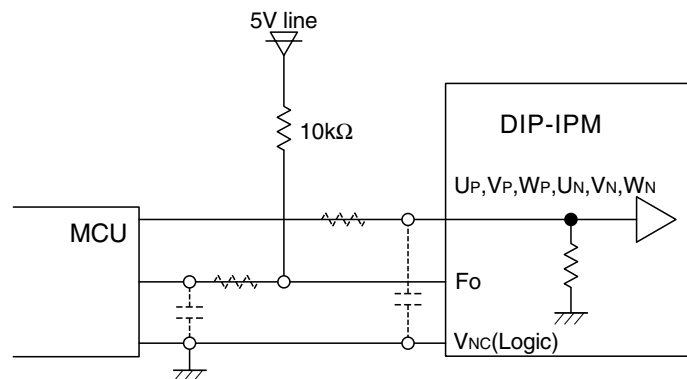


Fig. 8 RECOMMENDED CPU I/O INTERFACE CIRCUIT



Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using a external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

Fig. 9 WIRING CONNECTION OF SHUNT RESISTOR

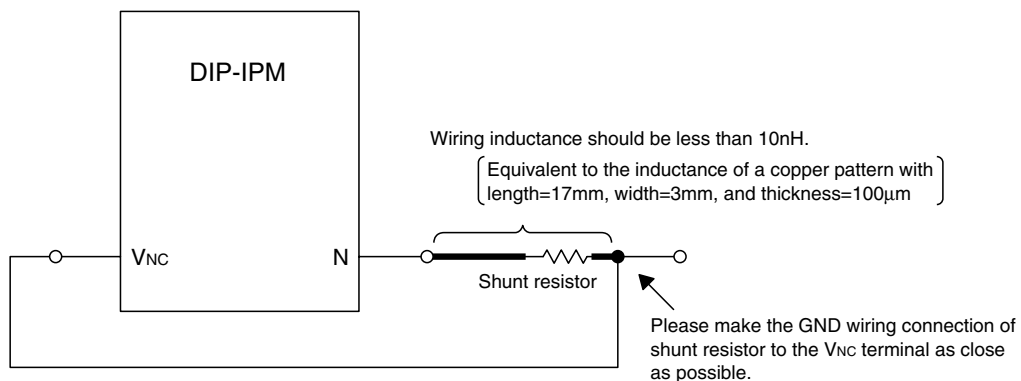
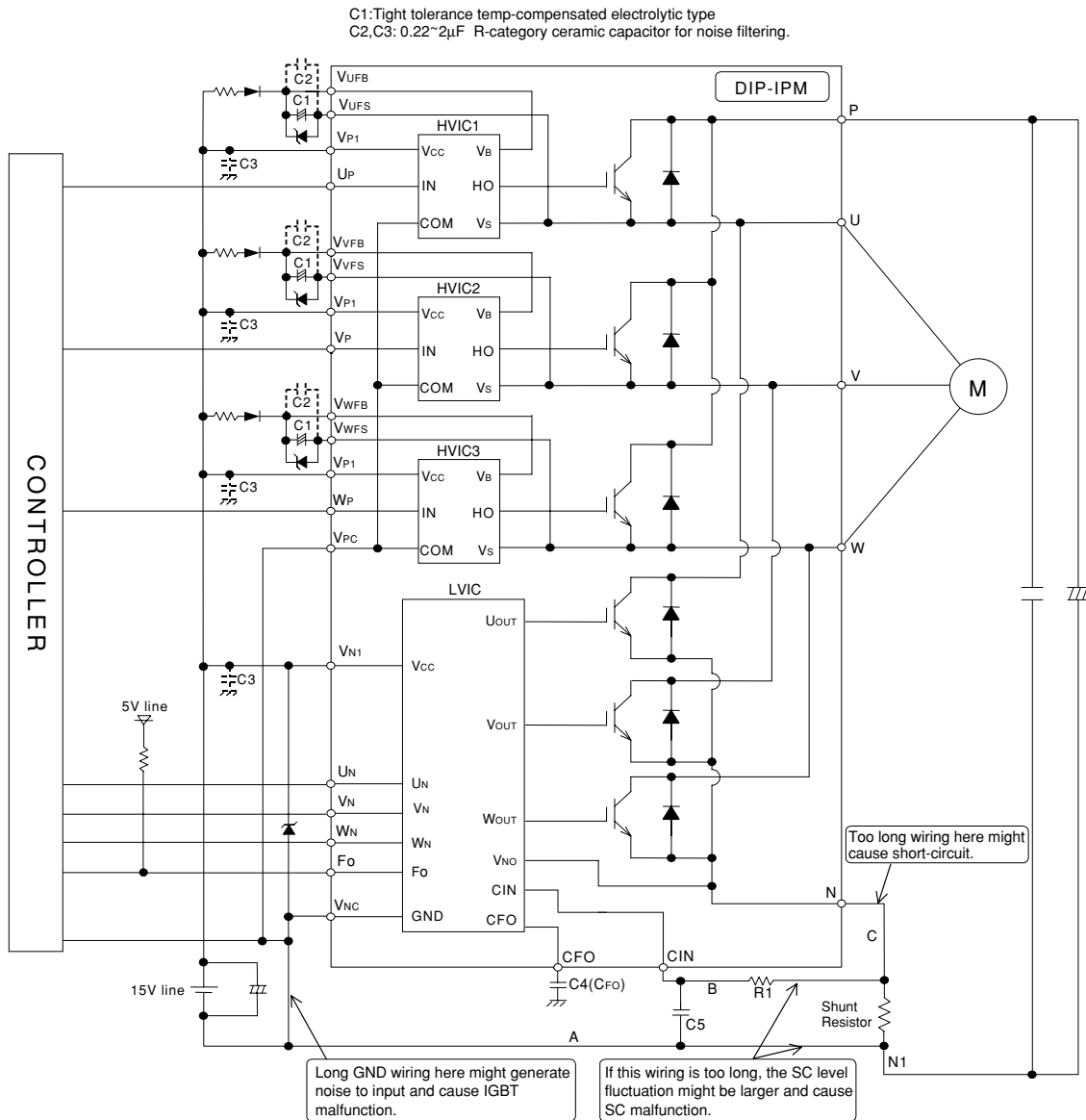


Fig. 10 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



Note 1: To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2cm)

2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.

3: Fo output is open drain type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.

4: Fo output pulse width is determined by the external capacitor between Cfo and Vnc terminals (Cfo). (Example : Cfo = 22nF → tFo = 1.8ms (typ.))

5: The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

6: To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.

7: Please set the R1C5 time constant in the range 1.5~2μs.

8: Each capacitor should be located as nearby the pins of the DIP-IPM as possible.

9: To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P-N1 pins is recommended.

10: It is recommended to insert a Zener diode (24V/1W) nearby each pair of supply terminals to prevent surge destruction.