

**CM100RX-12A**

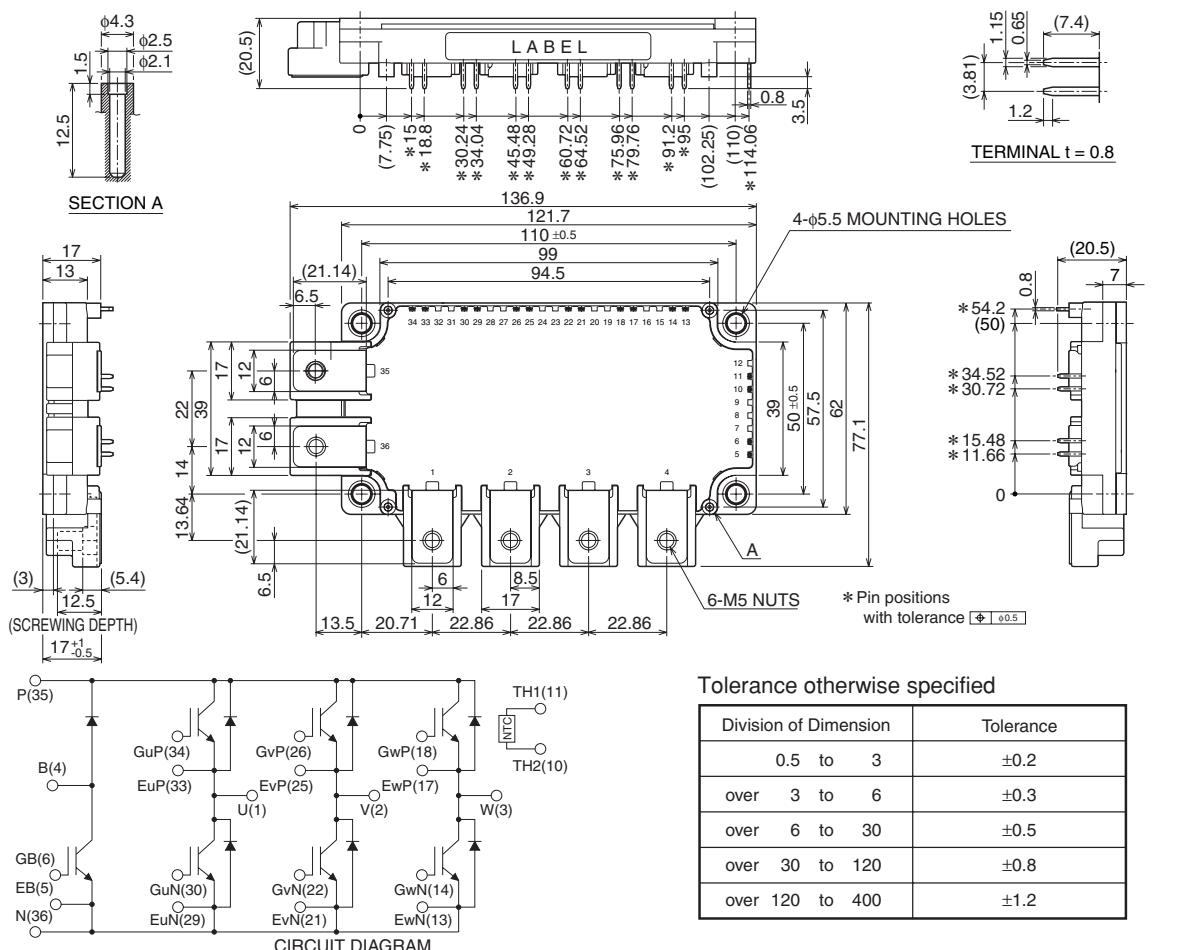
HIGH POWER SWITCHING USE

**CM100RX-12A**

- $I_C$  ..... 100A
- $V_{CES}$  ..... 600V
- 7pack (3-phase Inverter + Brake)
- Flatbase Type / Insulated Package / Copper (non-plating) base plate
- RoHS Directive compliant

**APPLICATION**

General purpose Inverters, Servo Amplifiers

**OUTLINE DRAWING & CIRCUIT DIAGRAM**

Jan. 2009

**ABSOLUTE MAXIMUM RATINGS ( $T_j = 25^\circ\text{C}$ , unless otherwise specified)****INVERTER PART**

Symbol	Parameter	Conditions	Rating	Unit
V <sub>CES</sub>	Collector-emitter voltage	G-E Short	600	V
V <sub>GES</sub>	Gate-emitter voltage	C-E Short	$\pm 20$	
I <sub>C</sub>	Collector current	DC, $T_c = 75^\circ\text{C}$	(Note. 1)	A
I <sub>CRM</sub>		Pulse	(Note. 4)	
P <sub>C</sub>	Maximum collector dissipation	$T_c = 25^\circ\text{C}$	(Note. 1, 5)	W
I <sub>E</sub> (Note.3)	Emitter current	$T_c = 25^\circ\text{C}$	(Note. 1)	100
I <sub>ERM</sub> (Note.3)	(Free wheeling diode forward current)	Pulse	(Note. 4)	200

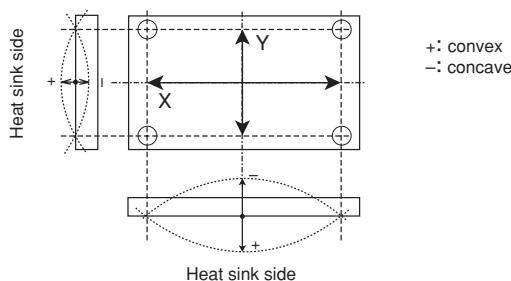
**BRAKE PART**

Symbol	Parameter	Conditions	Rating	Unit
V <sub>CES</sub>	Collector-emitter voltage	G-E Short	600	V
V <sub>GES</sub>	Gate-emitter voltage	C-E Short	$\pm 20$	
I <sub>C</sub>	Collector current	DC, $T_c = 97^\circ\text{C}$	(Note. 1)	A
I <sub>CRM</sub>		Pulse	(Note. 4)	
P <sub>C</sub>	Maximum collector dissipation	$T_c = 25^\circ\text{C}$	(Note. 1, 5)	W
V <sub>RRM</sub> (Note.3)	Repetitive peak reverse voltage		600	V
I <sub>F</sub> (Note.3)	Forward current	$T_c = 25^\circ\text{C}$	(Note. 1)	50
I <sub>FRM</sub> (Note.3)		Pulse	(Note. 4)	100

**MODULE**

Symbol	Parameter	Conditions	Rating	Unit
T <sub>j</sub>	Junction temperature		$-40 \sim +150$	°C
T <sub>stg</sub>	Storage temperature		$-40 \sim +125$	
V <sub>iso</sub>	Isolation voltage	Terminals to base plate, f = 60Hz, AC 1 minute	2500	Vrms
—	Base plate flatness	On the centerline X, Y (Note. 8)	$\pm 0 \sim +100$	μm
—	Torque strength	Main terminals M5 screw	2.5 ~ 3.5	N·m
—	Torque strength	Mounting M5 screw	2.5 ~ 3.5	
—	Weight	(Typical)	330	g

Note. 8: The base plate flatness measurement points are in the following figure.



**HIGH POWER SWITCHING USE****ELECTRICAL CHARACTERISTICS ( $T_j = 25^\circ\text{C}$ , unless otherwise specified)****INVERTER PART**

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
ICES	Collector cutoff current	VCE = VCES, VGE = 0V	—	—	1	mA
VGE(th)	Gate-emitter threshold voltage	IC = 10mA, VCE = 10V	5	6	7	V
IGES	Gate leakage current	$\pm VGE = VGES, VCE = 0V$	—	—	0.5	$\mu\text{A}$
VCE(sat)	Collector-emitter saturation voltage	IC = 100A, VGE = 15V (Note. 6)	$T_j = 25^\circ\text{C}$	—	1.7	2.1
			$T_j = 125^\circ\text{C}$	—	1.9	—
		IC = 100A, VGE = 15V	Chip	—	1.6	—
Cies	Input capacitance	VCE = 10V VGE = 0V (Note. 6)	—	—	13.3	nF
Coes	Output capacitance		—	—	1.4	
Cres	Reverse transfer capacitance		—	—	0.45	
QG	Total gate charge	VCC = 300V, IC = 100A, VGE = 15V	—	270	—	nC
td(on)	Turn-on delay time	VCC = 300V, IC = 100A $VGE = \pm 15V, R_G = 6.2\Omega$ Inductive load (IE = 100A)	—	—	100	ns
tr	Turn-on rise time		—	—	100	
td(off)	Turn-off delay time		—	—	300	
tf	Turn-off fall time		—	—	600	
trr (Note.3)	Reverse recovery time		—	—	200	
Qrr (Note.3)	Reverse recovery charge		—	4.8	—	$\mu\text{C}$
VEC(Note.3)	Emitter-collector voltage	IE = 100A, VGE = 0V (Note. 6)	$T_j = 25^\circ\text{C}$	—	2.0	2.8
			$T_j = 125^\circ\text{C}$	—	1.95	—
		IE = 100A, VGE = 0V	Chip	—	1.9	—
Rth(j-c)Q	Thermal resistance (Note. 1) (Junction to case)	per IGBT	—	—	0.31	K/W
Rth(j-c)R		per free wheeling diode	—	—	0.59	
RGint	Internal gate resistance	TC = 25°C, per switch	—	0	—	$\Omega$
RG	External gate resistance		6	—	62	

**BRAKE PART**

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
ICES	Collector cutoff current	VCE = VCES, VGE = 0V	—	—	1	mA
VGE(th)	Gate-emitter threshold voltage	IC = 5mA, VCE = 10V	5	6	7	V
IGES	Gate leakage current	$\pm VGE = VGES, VCE = 0V$	—	—	0.5	$\mu\text{A}$
VCE(sat)	Collector-emitter saturation voltage	IC = 50A, VGE = 15V (Note. 6)	$T_j = 25^\circ\text{C}$	—	1.7	2.1
			$T_j = 125^\circ\text{C}$	—	1.9	—
		IC = 50A, VGE = 15V	Chip	—	1.6	—
Cies	Input capacitance	VCE = 10V VGE = 0V (Note. 6)	—	—	9.3	nF
Coes	Output capacitance		—	—	1.0	
Cres	Reverse transfer capacitance		—	—	0.3	
QG	Total gate charge	VCC = 300V, IC = 50A, VGE = 15V	—	200	—	nC
Irrm(Note.3)	Repetitive peak reverse current	VR = VRM	—	—	1	mA
Vfm(Note.3)	Forward voltage drop	IF = 50A (Note. 6)	$T_j = 25^\circ\text{C}$	—	2.0	2.8
			$T_j = 125^\circ\text{C}$	—	1.95	—
		IF = 50A	Chip	—	1.9	—
Rth(j-c)Q	Thermal resistance (Note. 1) (Junction to case)	per IGBT	—	—	0.44	K/W
Rth(j-c)R		per Clamp diode	—	—	0.85	
RGint	Internal gate resistance	TC = 25°C	—	0	—	$\Omega$
RG	External gate resistance		13	—	130	

**HIGH POWER SWITCHING USE****NTC THERMISTOR PART**

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
R	Zero power resistance	T <sub>C</sub> = 25°C	4.85	5.00	5.15	kΩ
ΔR/R	Deviation of resistance	T <sub>C</sub> = 100°C, R <sub>100</sub> = 493Ω	-7.3	—	+7.8	%
B(25/50)	B constant	Approximate by equation (Note. 7)	—	3375	—	K
P <sub>25</sub>	Power dissipation	T <sub>C</sub> = 25°C	—	—	10	mW

**MODULE**

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
R <sub>th(c-f)</sub>	Contact thermal resistance (Case to fin) (Note. 1)	Thermal grease applied per 1 module (Note. 2)	—	0.015	—	K/W

Note. 1: Case temperature (T<sub>c</sub>), heat sink temperature (T<sub>r</sub>) measured point is just under the chips. (Refer to the figure of the chip location.)

2: Typical value is measured by using thermally conductive grease of  $\lambda = 0.9\text{W}/(\text{m}\cdot\text{K})$ .

3: I<sub>E</sub>, I<sub>ERM</sub>, V<sub>EC</sub>, t<sub>r</sub> and Q<sub>rr</sub> represent ratings and characteristics of the anti-parallel, emitter-collector free wheeling diode (FWDi).

I<sub>F</sub>, I<sub>FRM</sub>, V<sub>F</sub>, V<sub>RRM</sub> and I<sub>RRM</sub> represent ratings and characteristics of the Clamp diode of Brake part.

4: Pulse width and repetition rate should be such that the device junction temperature (T<sub>j</sub>) dose not exceed T<sub>jmax</sub> rating.

5: Junction temperature (T<sub>j</sub>) should not increase beyond 150°C.

6: Pulse width and repetition rate should be such as to cause negligible temperature rise.

(Refer to the figure of the test circuit for V<sub>CE(sat)</sub> and V<sub>EC</sub>)

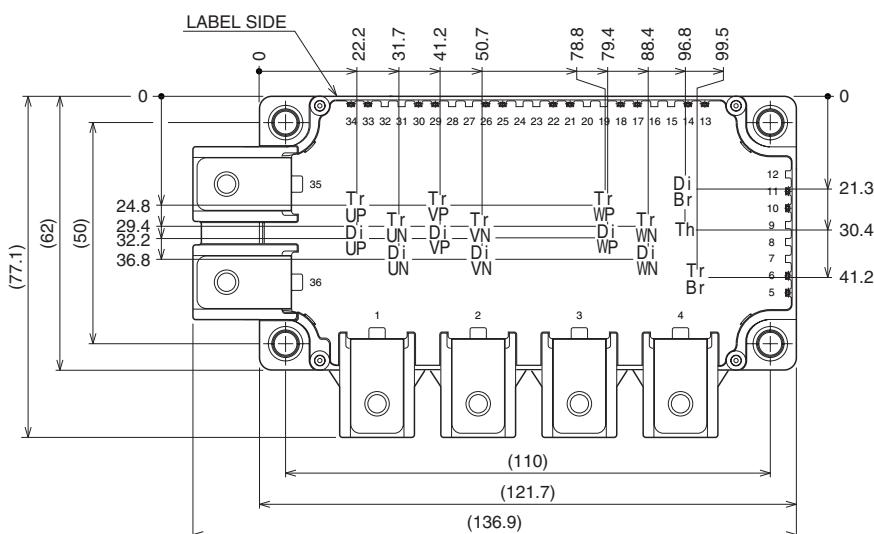
$$7: B(25/50) = \ln\left(\frac{R_{25}}{R_{50}}\right) / \left(\frac{1}{T_{25}} - \frac{1}{T_{50}}\right)$$

R<sub>25</sub>: resistance at absolute temperature T<sub>25</sub> [K]; T<sub>25</sub> = 25 [°C] + 273.15 = 298.15 [K]

R<sub>50</sub>: resistance at absolute temperature T<sub>50</sub> [K]; T<sub>50</sub> = 50 [°C] + 273.15 = 323.15 [K]

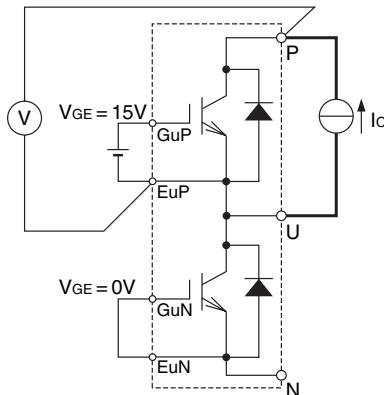
**Chip Location (Top view)**

Dimensions in mm (tolerance: ±1mm)

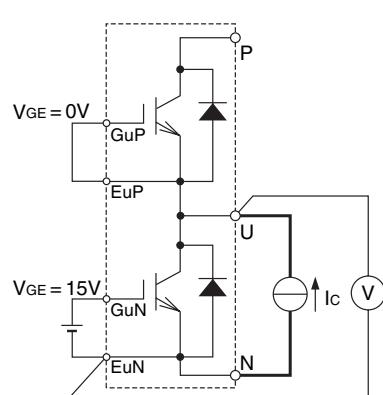


Each mark points the center position of each chip. Tr\*\*: IGBT, Di\*\*: FWDi (DiBr: Clamp diode), Th: NTC thermistor

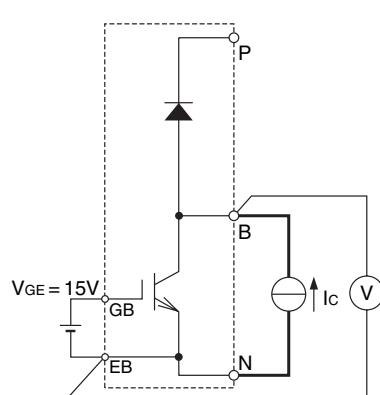
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**HIGH POWER SWITCHING USE**

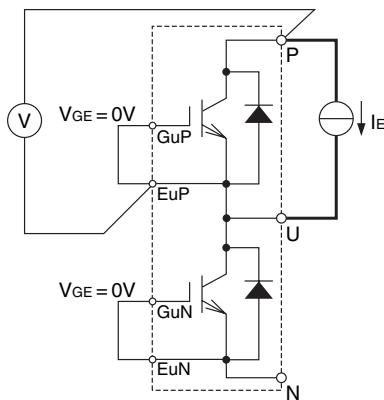
P side Inverter part Tr  
(example of U arm)  
 $V_{GE} = 0V(GvP-EvP, GwP-EwP, GvN-EvN,  
GwN-EwN, GB-EB)$



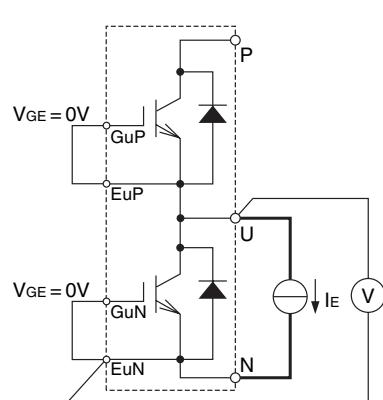
N side Inverter part Tr  
(example of U arm)  
 $V_{GE} = 0V(GvP-EvP, GwP-EwP, GvN-EvN,  
GwN-EwN, GB-EB)$



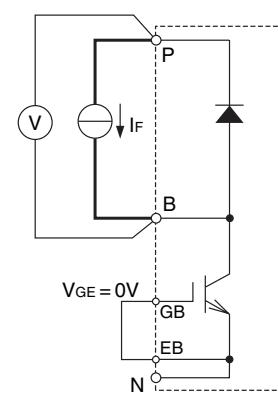
Br Tr  
 $V_{GE} = 0V(GuP-EuP, GvP-EvP, GwP-EwP,  
GuN-EuN, GvN-EvN, GwN-EwN)$

 **$V_{CE(sat)}$  test circuit**

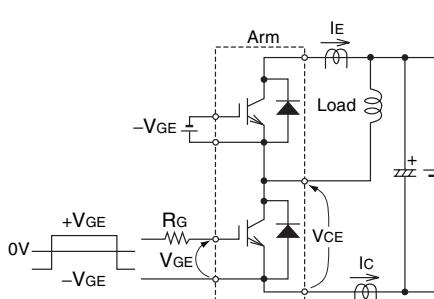
P side Inverter part Di  
(example of U arm)  
 $V_{GE} = 0V(GvP-EvP, GwP-EwP, GvN-EvN,  
GwN-EwN, GB-EB)$



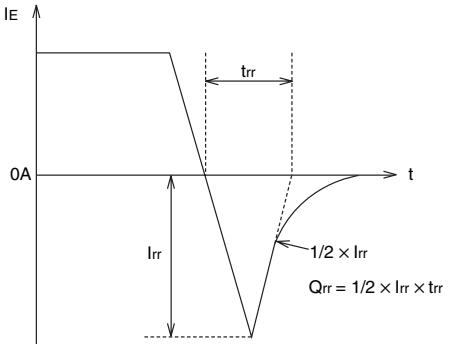
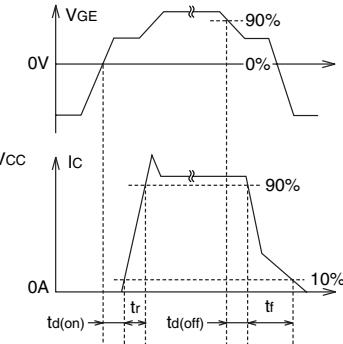
N side Inverter part Di  
(example of U arm)  
 $V_{GE} = 0V(GvP-EvP, GwP-EwP, GvN-EvN,  
GwN-EwN, GB-EB)$



Br Di  
 $V_{GE} = 0V(GuP-EuP, GvP-EvP, GwP-EwP,  
GuN-EuN, GvN-EvN, GwN-EwN)$

 **$V_{EC}/V_{FM}$  test circuit**

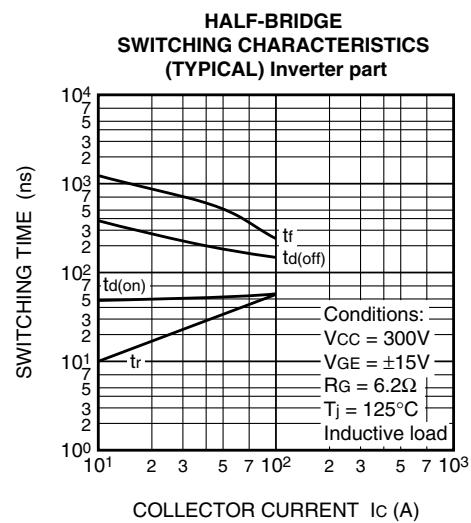
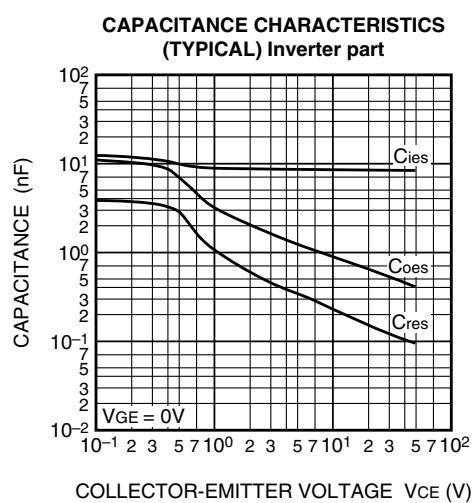
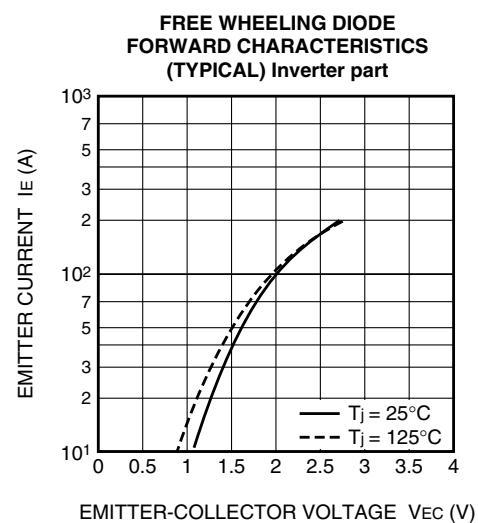
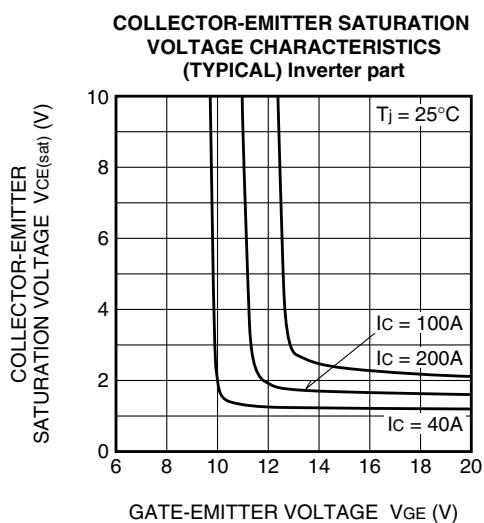
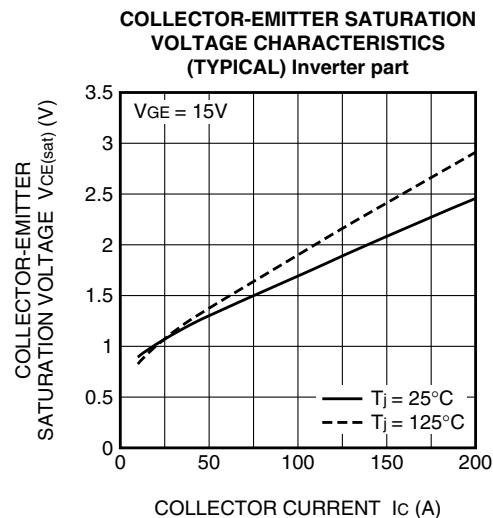
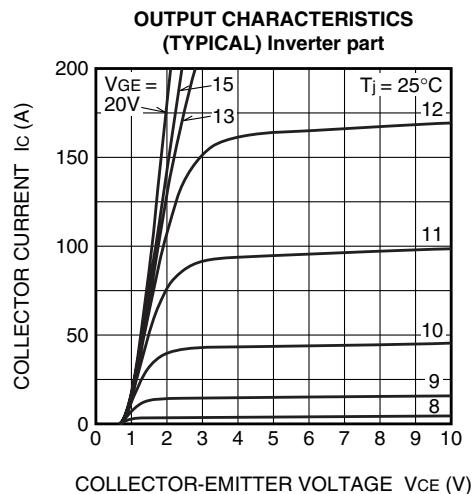
Switching time test circuit and waveforms

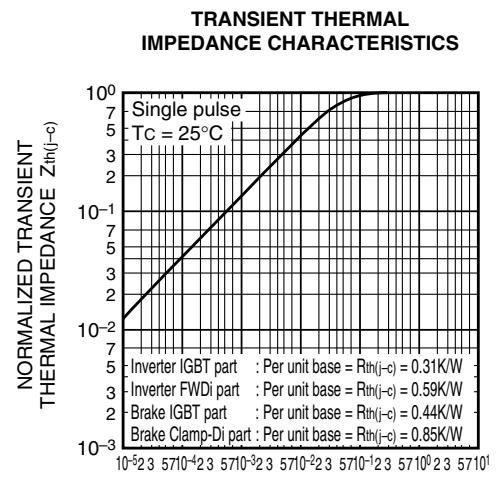
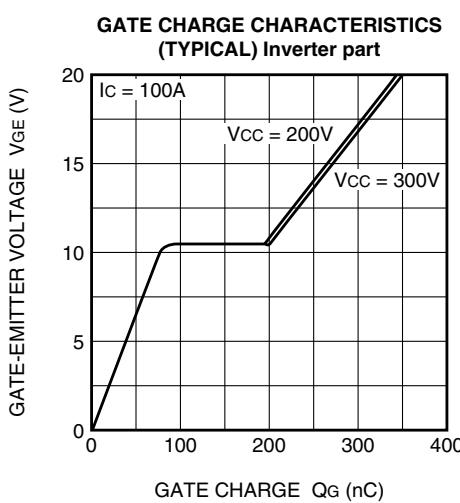
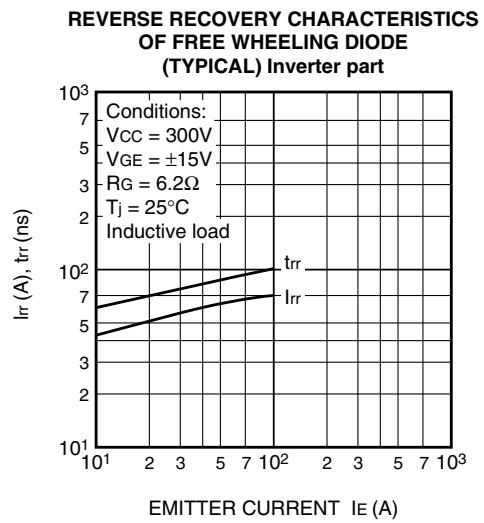
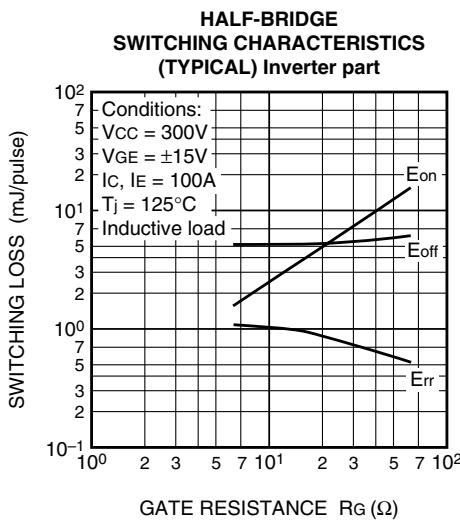
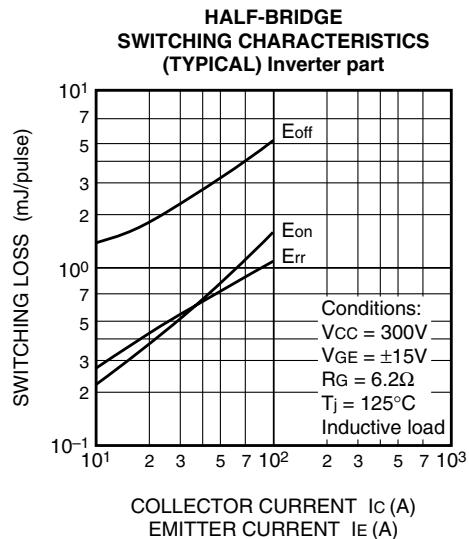
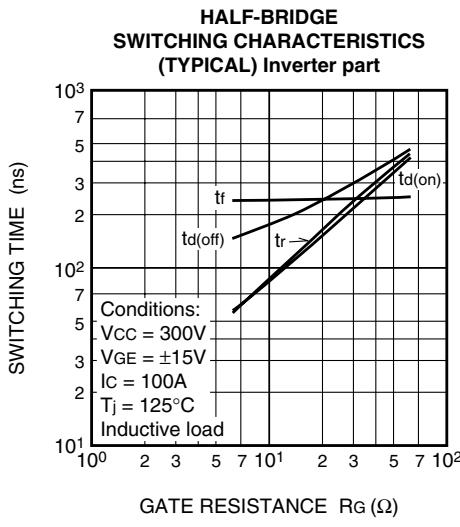


$t_{rr}, Q_{rr}$  test waveform

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## PERFORMANCE CURVES



**HIGH POWER SWITCHING USE**

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