Darlington Silicon Power Transistors

Designed for general-purpose amplifier and low speed switching applications.

• High DC Current Gain -

 $h_{FE} = 3500 \text{ (Typ)} @ I_C = 4.0 \text{ Adc}$

• Collector-Emitter Sustaining Voltage - @ 200 mAdc

 $V_{CEO(sus)} = 60 \text{ Vdc (Min)} - 2N6667$ = 80 Vdc (Min) - 2N6668

• Low Collector-Emitter Saturation Voltage -

 $V_{CE(sat)} = 2.0 \text{ Vdc (Max)} @ I_C = 5.0 \text{ Adc}$

• Monolithic Construction with Built-In Base-Emitter Shunt Resistors

• TO-220AB Compact Package

• Complementary to 2N6387, 2N6388

• Pb-Free Packages are Available*

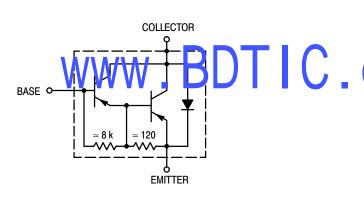


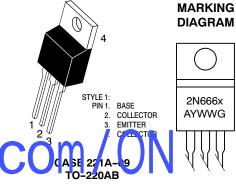
Figure 1. Darlington Schematic



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PNP SILICON DARLINGTON POWER TRANSISTORS 10 A, 60–80 V, 65 W



x = 7 or 8

A = Assembly Location

/ = Year

WW = Work Week

G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
2N6667	TO-220AB	50 Units/Rail
2N6667G	TO-220AB (Pb-Free)	50 Units/Rail
2N6668	TO-220AB	50 Units/Rail
2N6668G	TO-220AB (Pb-Free)	50 Units/Rail

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	2N6667	2N6668	Unit
Collector-Emitter Voltage	V _{CEO}	60	80	Vdc
Collector-Base Voltage	V _{CB}	60	80	Vdc
Emitter-Base Voltage	V _{EB}	5.0		Vdc
Collector Current - Continuous - Peak	lc	10 15		Adc
Base Current	I _B	250		mAdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D		65 52	W W/°C
Total Device Dissipation @ T _A = 25°C Derate above 25°C	P _D		.0 016	W W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	—65	to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{ heta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{ heta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (Note 1) ($T_C = 25$ °C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 2) 2N6667 (I _C = 200 mAdd (V _{CEN} (s is)	60 80	- -	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) 2N6668	CEO	-	1.0 1.0	mAdc
	ICEX	- - -	300 300 3.0 3.0	μAdc mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	-	5.0	mAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain ($I_C = 5.0$ Adc, $V_{CE} = 3.0$ Vdc) ($I_C = 10$ Adc, $V_{CE} = 3.0$ Vdc)	h _{FE}	1000 100	20000	-
Collector-Emitter Saturation Voltage ($I_C = 5.0$ Adc, $I_B = 0.01$ Adc) ($I_C = 10$ Adc, $I_B = 0.1$ Adc)	V _{CE(sat)}	-	2.0 3.0	Vdc
Base–Emitter Saturation Voltage(I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)	V _{BE(sat)}	-	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain - Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc, f _{test} = 1.0 MHz)	h _{fe}	20	-	-
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	-	200	pF

- 1. Indicates JEDEC Registered Data.
- 2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

Small-Signal Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$, f = 1.0 kHz)

 $h_{\text{fe}} \\$

1000

 R_B & R_C varied to obtain desired current levels $D_1,$ MUST be fast recovery types e.g., $1N5825 \text{ USED ABOVE I}_B \approx 100 \text{ mA} \\ \text{MSD6100 USED BELOW I}_B \approx 100 \text{ mA}$

FOR t_d and t_r , D_1 is disconnected and V_2 = 0 $t_r,\,t_f\,\leq\,$ 10 ns duty cycle = 1.0%

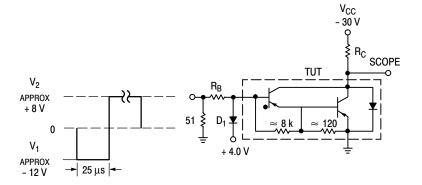


Figure 2. Switching Times Test Circuit

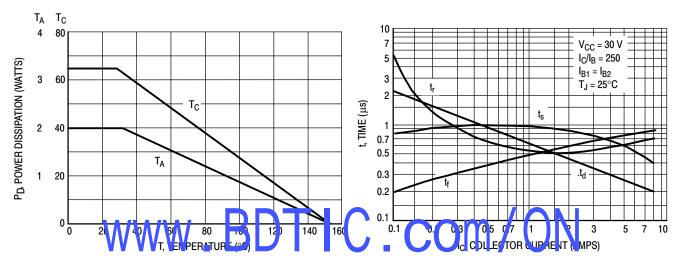


Figure 3. Power Derating

Figure 4. Typical Switching Times

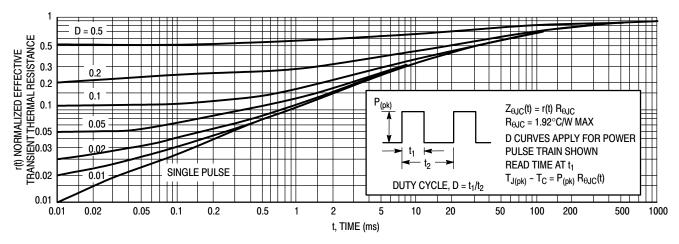


Figure 5. Thermal Response

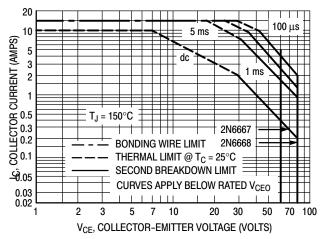


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_{C} is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

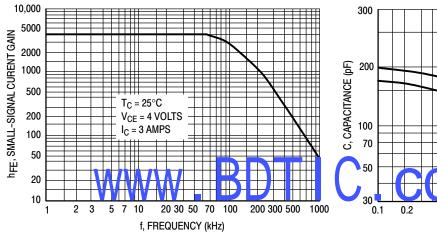


Figure 7. Typical Small-Signal Current Gain

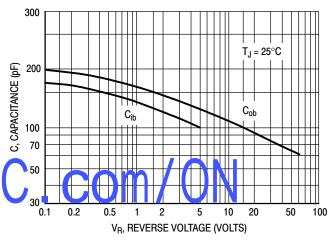


Figure 8. Typical Capacitance

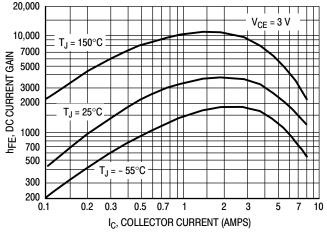


Figure 9. Typical DC Current Gain

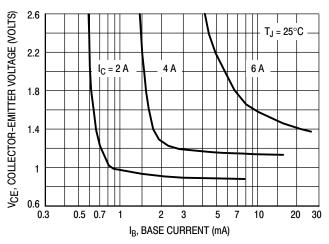
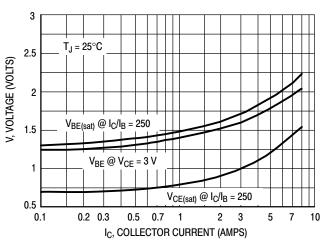


Figure 10. Typical Collector Saturation Region



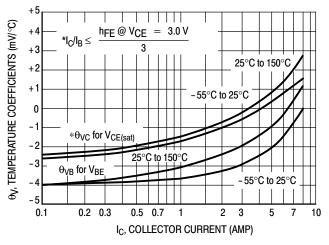


Figure 11. Typical "On" Voltages

Figure 12. Typical Temperature Coefficients

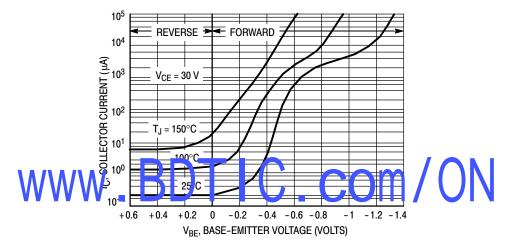
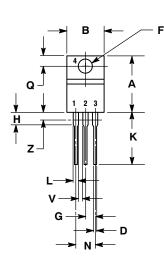
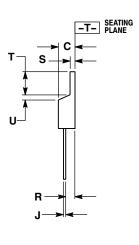


Figure 13. Typical Collector Cut-Off Region

PACKAGE DIMENSIONS

TO-220 CASE 221A-09 ISSUE AE





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 V14 FM 1092
- 2. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

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