Ordering number : EN2158B

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

2SD1835 — NPN Epitaxial Planar Silicon Transistor
Driver Applications

Applications

- Voltage regulators, relay drivers, lamp drivers, electrical equipment

Features

- Adoption of FBET, MBIT processes
- Low collector-to-emitter saturation voltage
- Large current capacity
- Fast switching time

Specifications

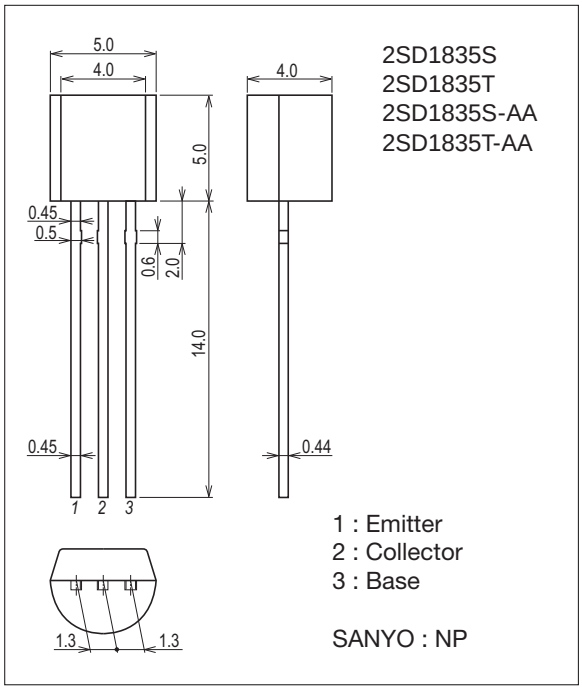
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		60	V
Collector-to-Emitter Voltage	V_{CEO}		50	V
Emitter-to-Base Voltage	V_{EBO}		6	V
Collector Current	I_C		2	A
Collector Current (Pulse)	I_{CP}		3	A
Collector Dissipation	P_C		0.75	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Package Dimensions

unit : mm (typ)

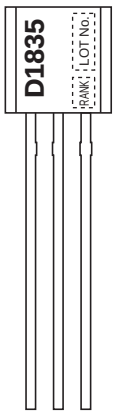
7522-002



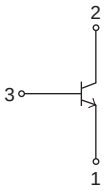
Product & Package Information

- Package : NP
- JEITA, JEDEC : SC-34A, TO-92, TO-226AA, SOT-54
- Minimum Packing Quantity : 1,500 pcs./box, 500pcs./bag

Marking



Electrical Connection



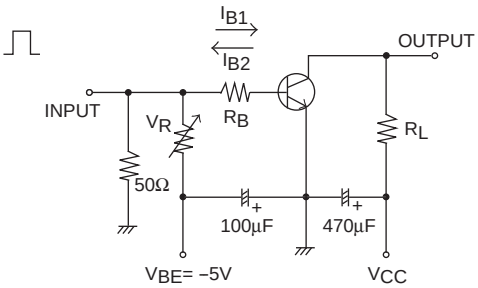
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=50V, I_E=0A			100	nA
Emitter Cutoff Current	I_{EBO}	V_{EB}=4V, I_C=0A			100	nA
DC Current Gain	$h_{FE}1$	V_{CE}=2V, I_C=100mA	100*		560*	
	$h_{FE}2$	V_{CE}=2V, I_C=1.5A	40			
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=50mA		150		MHz
Output Capacitance	Cob	V_{CB}=10V, f=1MHz		12		pF
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=1A, I_B=50mA		0.15	0.4	V
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=1A, I_B=50mA		0.9	1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0A	60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, R_{BE}=∞	50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0A	6			V
Turn-ON Time	t_{on}	See specified Test Circuit.		60		ns
Storage Time	t_{stg}			550		ns
Fall Time	t_f			30		ns

* : The 2SD1835 is classified by 100mA h_{FE} as follows :

Rank	R	S	T	U
h_{FE}	100 to 200	140 to 280	200 to 400	280 to 560

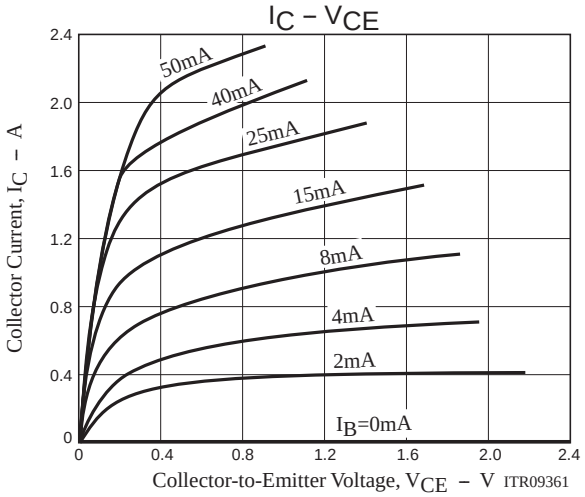
Switching Time Test Circuit

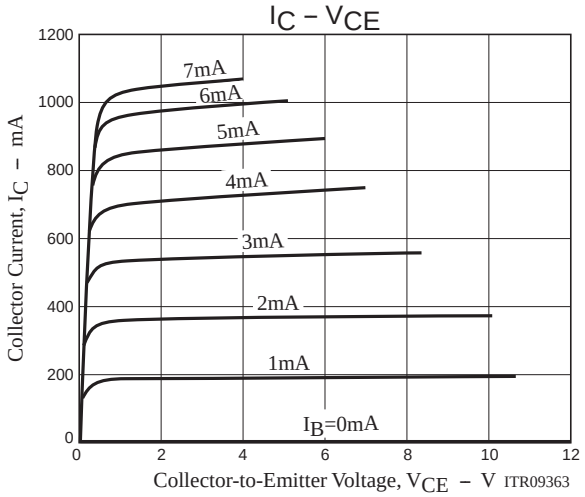


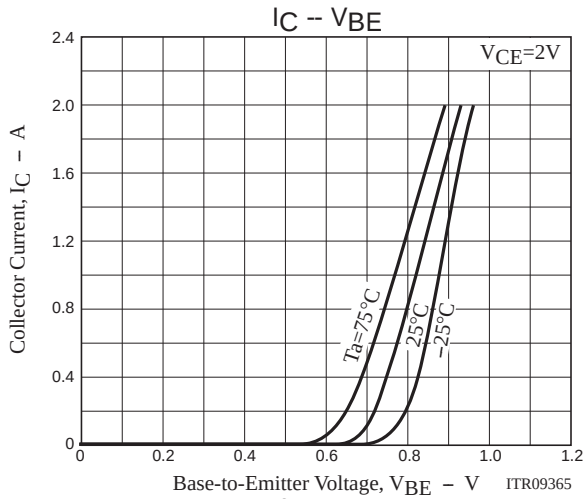
I_C=10I_{B1}= −10I_{B2}=500mA, V_{CC}=25V

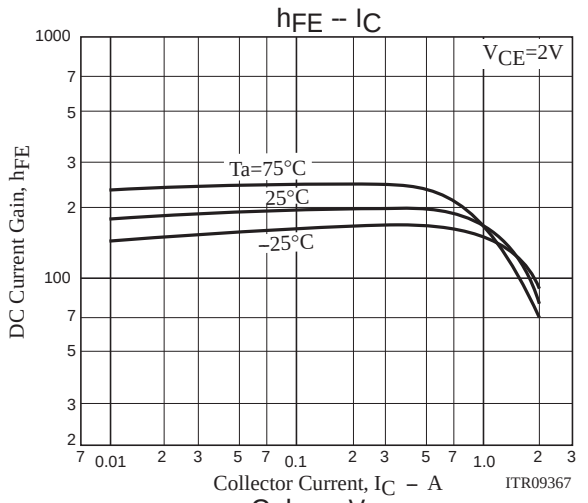
Ordering Information

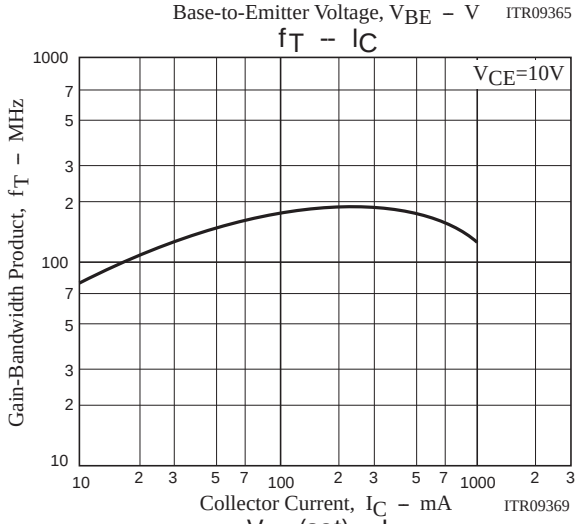
Device	Package	Shipping	memo
2SD1835S	NP	500pcs./bag	Pb Free
2SD1835T	NP	500pcs./bag	
2SD1835S-AA	NP	1,500pcs./box	
2SD1835T-AA	NP	1,500pcs./box	

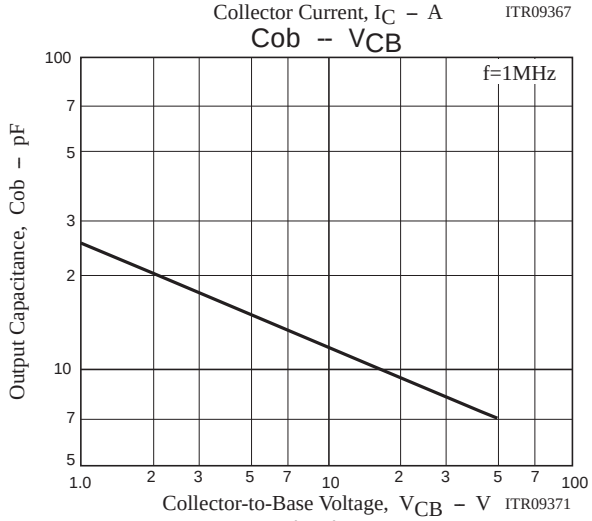


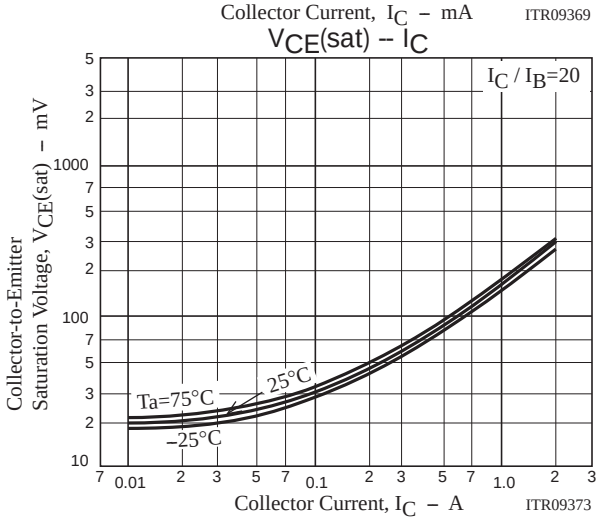


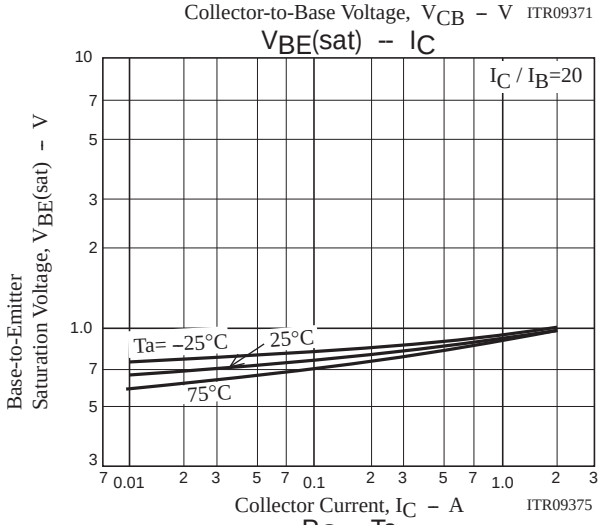

IC -- VBE
VCE=2V
Collector Current, IC – A
Base-to-Emitter Voltage, VBE – V
Ta=75°C
25°C
–25°C
ITR09365

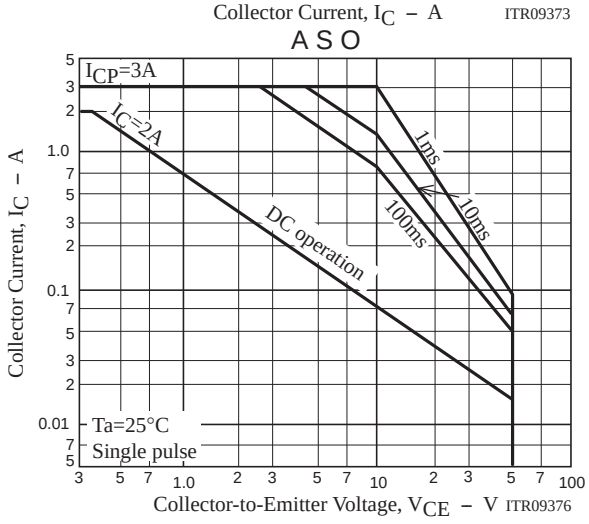

hFE -- IC
VCE=2V
DC Current Gain, hFE
Collector Current, IC – A
Ta=75°C
25°C
–25°C
ITR09367

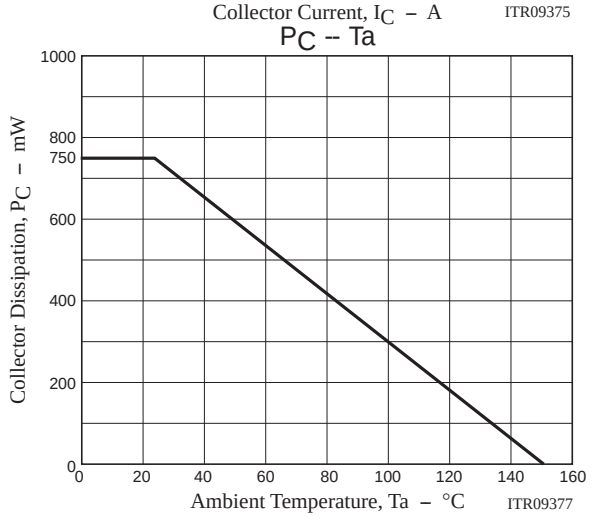

fT – IC
VCE=10V
Gain-Bandwidth Product, fT – MHz
Collector Current, IC – mA
ITR09369


Cob -- VCB
f=1MHz
Output Capacitance, Cob – pF
Collector-to-Base Voltage, VCB – V
ITR09371


VCE(sat) -- IC
IC / IB=20
Collector-to-Emitter Saturation Voltage, VCE(sat) – mV
Collector Current, IC – A
Ta=75°C
25°C
–25°C
ITR09373


VBE(sat) -- IC
IC / IB=20
Base-to-Emitter Saturation Voltage, VBE(sat) – V
Collector Current, IC – A
Ta= –25°C
25°C
75°C
ITR09375


A S O
ICP=3A
IC=2A
1ms
10ms
100ms
DC operation
Ta=25°C
Single pulse
Collector Current, IC – A
Collector-to-Emitter Voltage, VCE – V
ITR09376


PC -- Ta
Collector Dissipation, PC – mW
Ambient Temperature, Ta – °C
ITR09377

Taping Specification

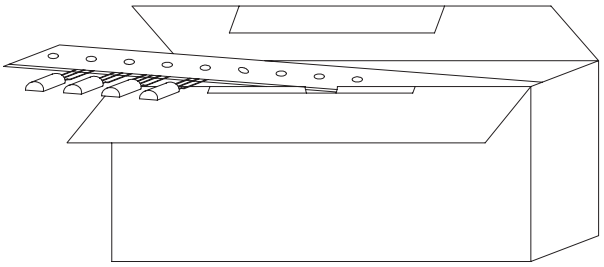
2SD1835S-AA, 2SD1835T-AA

1. Packing Format

Package Name	Packing Type	Maximum Number of devices contained (pcs)		Packing format
		Inner BOX (C-2)	number of contained	Outer BOX (C-6)
NP	AA	Dimensions:mm (external) 330×45×145	1,500	16 inner boxes contained (24,000pcs) Dimensions:mm (external) 585×345×200

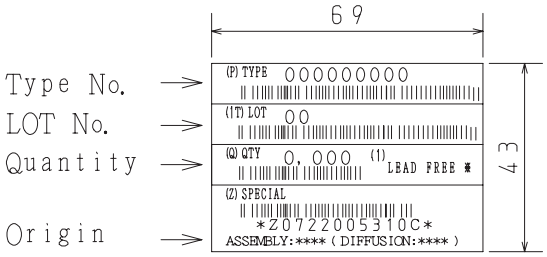
Packing method

Put zigzag folding in an inner box.



Inner box label

(unit:mm)



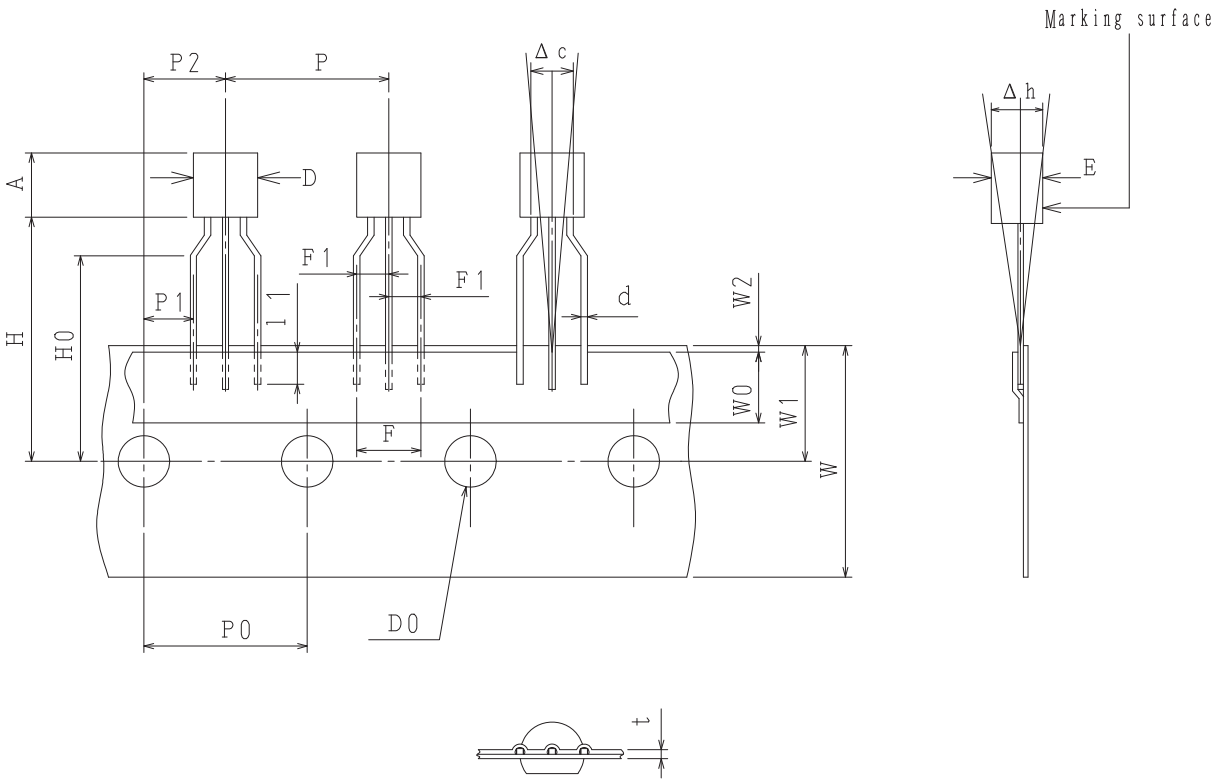
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping specifications

2-1. Carrier tape size



2-2. Taping size standard

unit:mm

Item	Symbol	Standard	Tolerance	
Work piece outside diameter	D	5.0	±0.2	
	E	4.0	±0.2	
Work piece height	A	5.0	±0.2	
Lead wire diameter	d	0.45×0.44t	±0.1	
Bonded lead wire	l1	2.0MIN		
Pitch between products	P	12.7	±0.5	
Pitch between perforations	P0	12.7	±0.2	
Distance between lead wire	F	5.0	+0.8 −0.2	
Lead wire pitch distance	F1	2.5	+0.2 −0.1	
Product inclination	△h	0	±2.0	
Displacement of perforations	P1	3.85	±0.3	Measurement position is the bottom of the clinch
	P2	6.35	±0.3	
Displacement of tape	W2	0.5MAX		Not to be displaced to the outside of the board

Item	Symbol	Standard	Tolerance
Tape width	W	18.0	+1.0 −0.5
Adhesive tape	W0	6.0	±1.5
Displacement of perforations	W1	9.0	±0.5
Work piece bottom surface position	H	19.0	±1.0
Insert stopper position	H0	16.0	±0.5
Work piece upper limit position	H1	24.5	±1.5
Perforations diameter	D0	φ4.0	±0.2
Tape thickness	t	0.6	±0.2
Product inclination	△c	0	±1.0

Bag Packing Specification

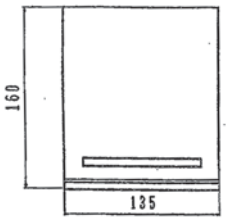
2SD1835S, 2SD1835T

1 . Packing condition

Storange package outline name	Maximum number of devices contained (pcs.)			Packing condition	
	Bags	Inner box	Devices contained	Outer box (A−1)	Outer box (A−2)
NP	500	B−1 Inner box dimensions : mm (external) 445×225×55	10,000	5 inner boxes contained 50,000 Outer box dimensions : mm (external) 470 × 250 × 300	3 inner boxes contained 30,000 Outer box dimensions : mm (external) 470 × 250 × 190

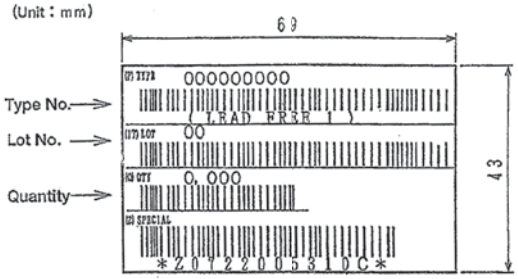
2. Bag dimensions

(Unit : mm)



3. Bar code label

(Unit : mm)



*LEAD FREE 1:
Lead-free External terminal surface treatment product.

Outline Drawing

2SD1835S, 2SD1835T

Mass (g)	Unit
0.269 * For reference	mm