CAT884

Quad Voltage Supervisor

Description

The CAT884 is a four−channel power supply supervisory circuit with high accuracy reset thresholds and very low power consumption. The device features an active−low open−drain output with manual reset to perform basic system reset and voltage monitoring functions for a wide range of electronic products.

CAT884 monitors four system voltages maintaining its reset output active until all the power supply voltages exceed the specified threshold values. The four threshold voltages are user controlled and can be set for system specific requirements over a range of 0.635 V to 5.5 V using external resistor dividers.

The CAT884 lowers system costs and saves board space by integrating four channels into a single, small SOIC 8−lead package and operates over the industrial temperature range of −40°C to +85°C.

Features

- Quad Voltage Monitoring
- Adjustable Threshold Voltages down to 0.635 V with ±2% Accuracy
- Low Supply Current: 3 μA (typ)
- $\overline{\text{RESET}}$ Valid to V_{CC} = 1 V
- Immune to Short Supply Transients
- Operating Temperature Range: −40°C to +85°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Monitoring of Multiple Power Supply Voltages in μP Based Systems

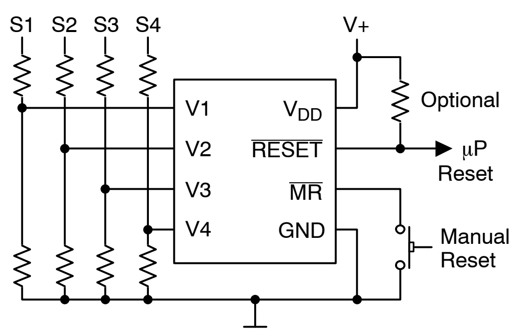

Figure 1. Typical Application Circuit

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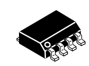
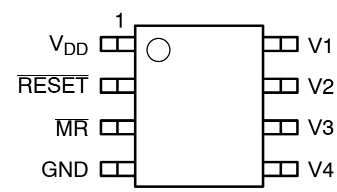


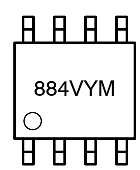
SOIC−8
V SUFFIX
CASE 751BD

PIN CONNECTIONS



(Top View)

MARKING DIAGRAM



884V = Device Code
Y = Production Year (Last Digit)
M = Production Month: 1−9, A, B, C

ORDERING INFORMATION

Device	Package	Shipping†
CAT884RVI−GT3	SOIC−8 (Pb−Free)	3,000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

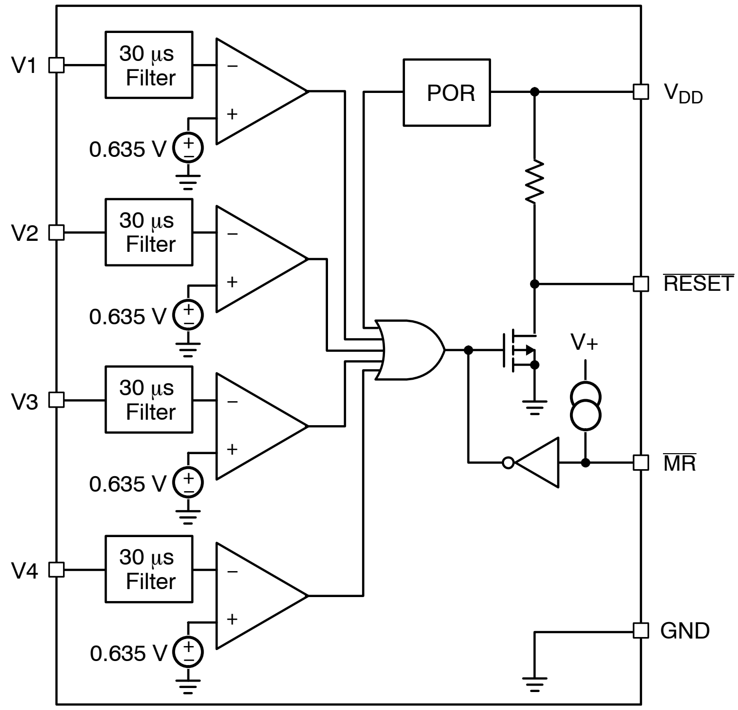


Figure 2. CAT884 Block Diagram

Table 1. PIN FUNCTION

Pin Number	Pin Name	Function
1	VDD	Chip power supply
2	$\overline{\text{RESET}}$	Open Drain active LOW reset output
3	$\overline{\text{MR}}$	Manual Reset
4	GND	Ground
5	V4	Fourth adjustable under−voltage detector input
6	V3	Third adjustable under−voltage detector input
7	V2	Second adjustable under−voltage detector input
8	V1	First adjustable under−voltage detector input

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
V_{DD}, V1−V4, $\overline{\text{MR}}$, $\overline{\text{RESET}}$ to GND	−0.3 to +6.0	V
Continuous $\overline{\text{RESET}}$ Current	20	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	+150	°C
Lead Temperature (soldering, 10 s)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS
(V_{DD} = 1.0 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.0 V to 3.3 V, T_A = +25°C. (Note 1))

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Operating Voltage		1.5		5.5	V
I_{DD}	Supply Current	V_{DD} = 5 V		3	9	μA
$V_{POR\_}$	V_{DD} Input Voltage Threshold	V_{DD} low → High		2.6		V
		V_{DD} High → Low		2.4		
RESET OUTPUT						
V_{OL}	$\overline{\text{RESET}}$ Output Low	$V_{CC} \geq 5$ V, I_{SINK} = 2.5 mA		0.05	0.4	V
		V_{CC} < 3.3 V, I_{SINK} = 1.5 mA		0.05	0.4	
RIN	Internal Pull−Up Resistor			20		kΩ
TCV_{TH}	Reset Threshold Temperature Coefficient			60		ppm/°C
t_{RPD}	Delay; V_{IN} to Reset	V_{IN} falling at 10 mV/μs from V_{TH} to (V_{TH} – 50 mV)	1	1.5		μs
VOLTAGE THRESHOLD						
V_{TH}	Adjustable Threshold	Monitored voltage decreasing	0.619	0.635	0.651	V
V_{HYST}	Reset Threshold Hysteresis	Monitored voltage increasing compared to monitored voltage decreasing		10		mV
V_{TH_VAR}	Variance of V_{TH} voltages	V_{TH} (max) – V_{TH} (min) (Note 4)		1.8		mV
t_{FIL}	Glitch Filter Delay	V_{MON} glitch to RST low Filter		30		μs
t_{RD}	Delay; V_{MON} to Reset	V_{MON} falling at 10 mV/μs from V_{TH} to (V_{TH} – 50 mV)	1	2		μs
MANUAL RESET INPUT						
VTHL	$\overline{\text{MR}}$ Input Voltage Low				0.8	V
VTHH	$\overline{\text{MR}}$ Input Voltage High		VDD – 0.6			V
T_{PW}	$\overline{\text{MR}}$ Minimum Pulse Width		20			ns
IPU	Pull−Up Current			10		μA
t_{MD}	$\overline{\text{MR}}$ to Deassert Reset output delay			40		ns
t_{MR}	$\overline{\text{MR}}$ to Assert Reset output delay			30		ns

1. 100% production tested at T_A = +25°C. Limits over temperature guaranteed by design.
2. The devices are powered from V_{DD}.
3. The $\overline{\text{RESET}}$ output is guaranteed to be in the correct state for V_{DD} down to 1 V.
4. Not tested in production but guaranteed by design.

TYPICAL CHARACTERISTICS

(V_{DD} = 3.0 V, T_A = +25°C, unless specified otherwise.)

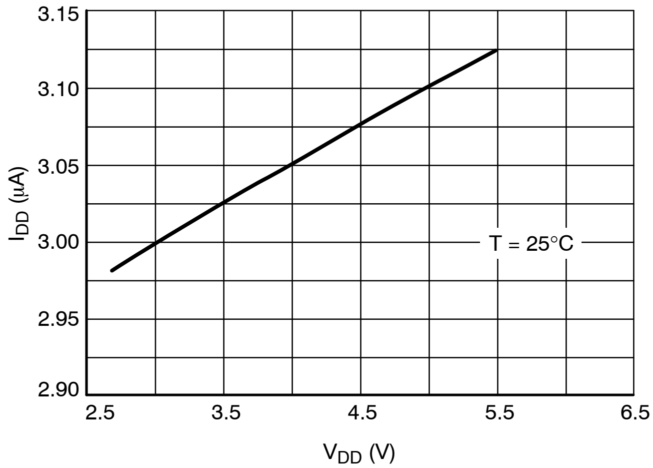


Figure 3. I_{DD} Input Current vs. Temperature

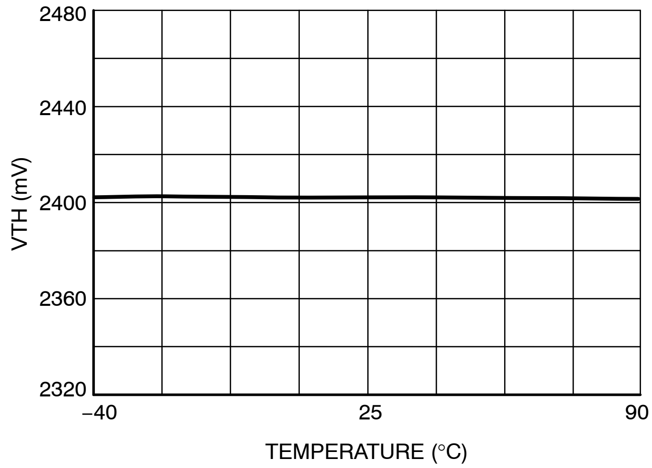


Figure 4. V_{DD} Input Voltage Threshold (High to Low)

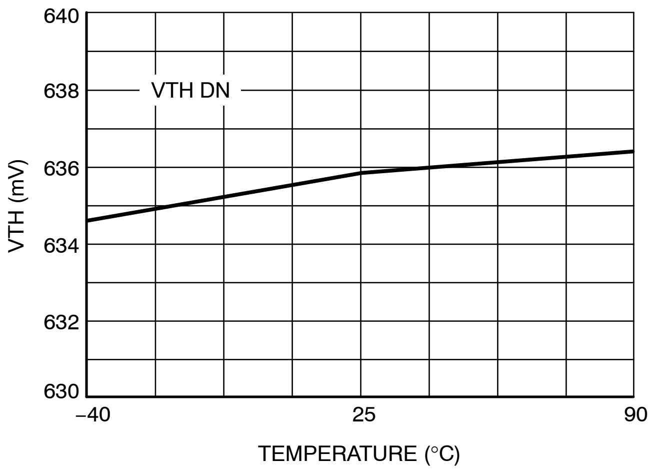


Figure 5. Monitored Voltages Decreasing

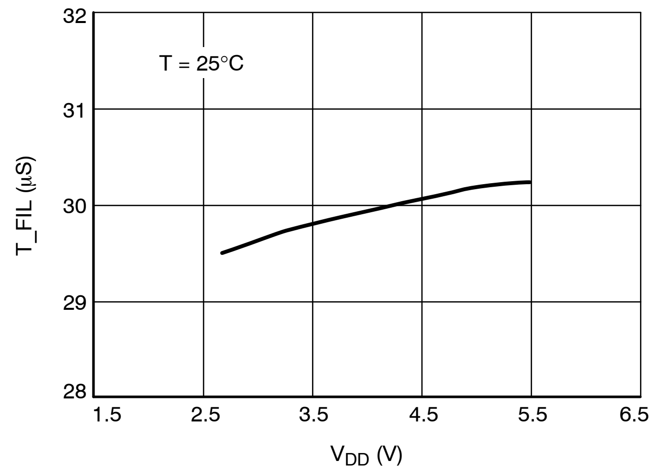


Figure 6. Glitch Filter Delay for Voltage Monitors

Detailed Description

The CAT884 is a space−saving, low−power, quad voltage microprocessor supervisory circuit designed monitor 4 voltage supplies.

Applications Information

Reset Output

CAT884 provides an active LOW system reset signal via an open drain output which requires an external pull−up resistor to an external power supply. This supply can be less than or greater than V_{DD}, but should not exceed 5.5 V. When the external pull−up voltage is greater than V_{DD} reverse current flow from the external pull−up voltage to V_{DD} is prevented by CAT884's internal circuitry.

V_{DD} is also a monitored voltage in CAT884 with thresholds set for 2.6 V rising and 2.4 V falling. When any monitored supply drops below its threshold, the reset output asserts LOW and remains LOW as long as V_{DD} is above 1.0 V.

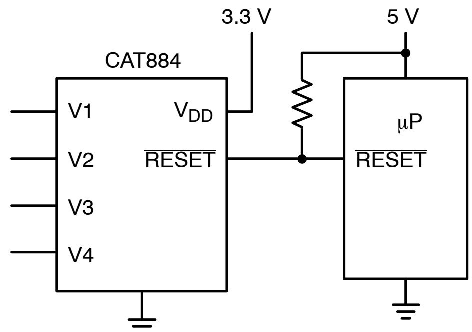


Figure 7. Interfacing to Different Logic−Supply Voltage

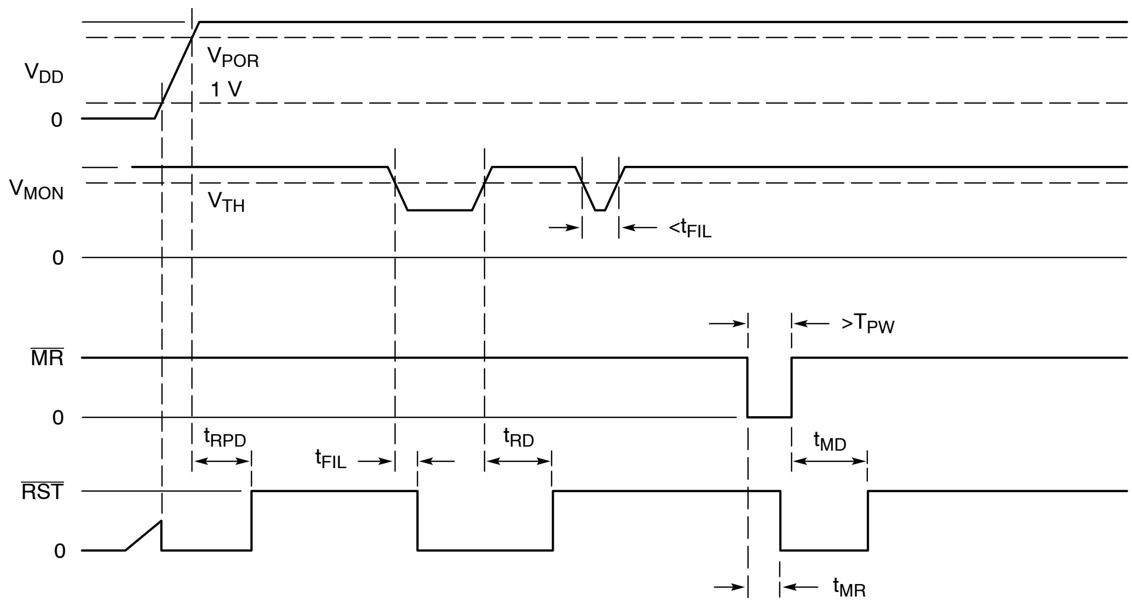


Figure 8. Operational Timing Diagram

Adjustable Thresholds

CAT884 allows users to create 4 custom voltage thresholds. The threshold voltage at each adjustable input is typically 0.635 V. Monitoring of voltages greater than 0.635 V requires a resistor−divider network to be connected to the circuit (Figure 9).

$$V_{IN} = 0.635\ \mathrm{V} \times \frac{(R1 + R2)}{R2}$$

or, written in terms of R1:

$$R1 = R2\left(\left(\frac{V_{IN}}{0.635\ \mathrm{V}}\right) - 1\right)$$

Because the CAT884 has a guaranteed input current of less than 50 nA on the monitoring inputs, resistor values up to 1,000 kΩ can be used for R2 with < 1% error.

Each of the 4 monitor inputs is also equipped with a glitch canceling circuit which filters out noise spikes and transients 30 μs or shorter in duration. For applications where greater noise immunity is required, connect a capacitor between each input pin and ground (in parallel with R2), placing the capacitor and resistor very close to CAT884's package.

Unused Inputs

Connect any unused monitor inputs to a supply voltage greater in magnitude than their specified threshold voltages; use V_{DD} for normal operation (device power−supply pin). Do not connect unused monitor inputs to ground or allow them to float.

POR

Applying power to the CAT884 activates a POR circuit which activates the reset output (active LOW). At power−up POR prevents the system microprocessor from starting to operate with insufficient voltage and prior to stabilization of the clock oscillator. It ensures that operation is precluded until internal registers are properly loaded and FPGA's have downloaded their configuration data. The reset signal remains active until all monitored power supplies have risen above their minimum preset voltage levels.

Power−Supply Bypassing

While not required for proper operation it is good practice to bypass CAT884's power supply with a 0.1 μF capacitor placed close to the VDD pin.

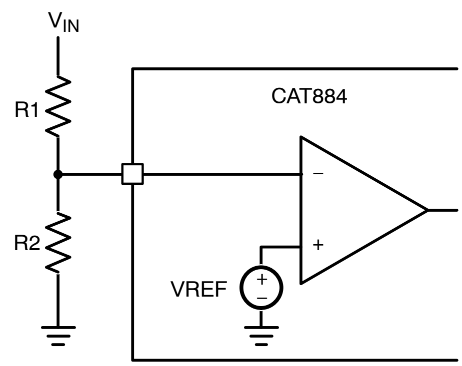
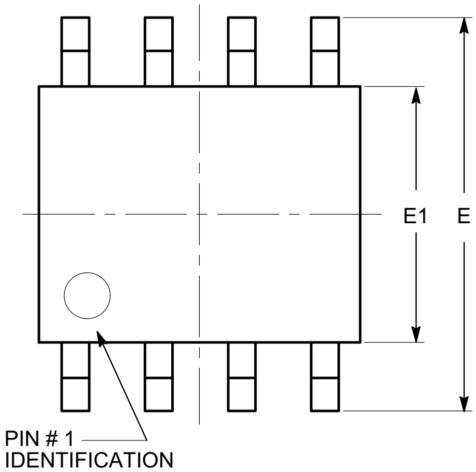


Figure 9. Setting Monitor Voltage

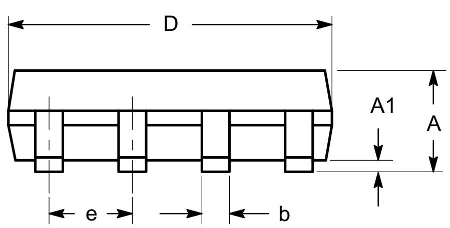
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

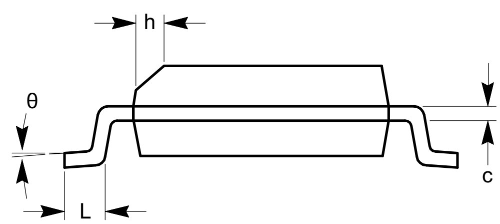


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



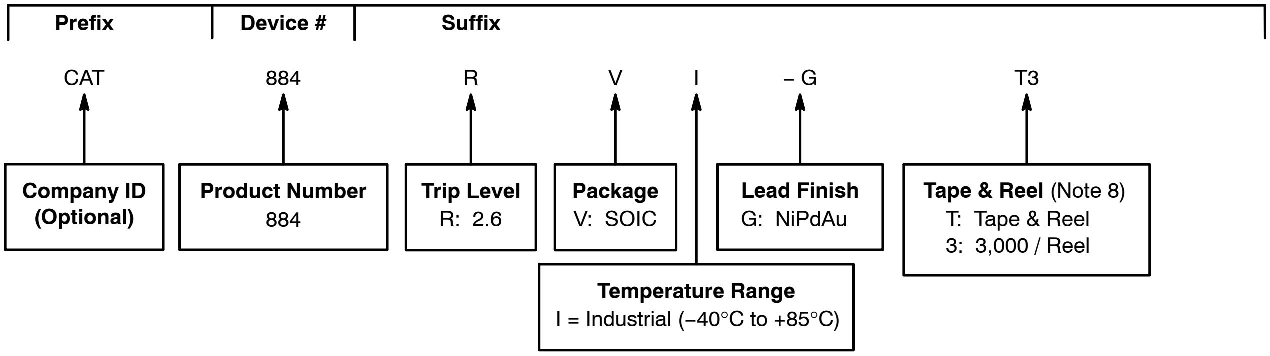
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Example of Ordering Information (Note 7)



5. All packages are RoHS−compliant (Lead−free, Halogen−free).
6. The standard plated finish is NiPdAu.
7. The device used in the above example is a CAT884RVI−GT3 (Trip Level, SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
8. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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