

CM1263-02SE

Low Capacitance ESD Protection for High-Speed Serial Interfaces

Features

- 2 Channels of ESD Protection
- 0.85 pF Loading Capacitance per Channel Typical
- Provides ESD Protection to IEC61000-4-2 Level 4:
 - ± 8 kV Contact Discharge
 - ± 15 kV Air Discharge
- 5-Pin SOT-553 Package
- These Devices are Pb-Free and are RoHS Compliant

Applications

- LCD and Camera Data Lines in Wireless Handsets that Use High-speed Serial Interfaces such as MDDI, MIPI, MVI and MPL
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules



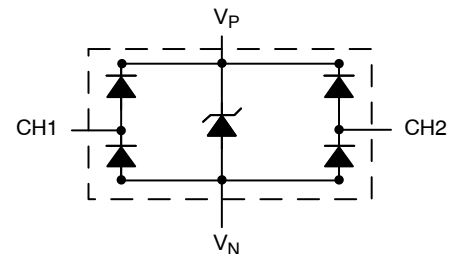
ON Semiconductor®

<http://onsemi.com>



SOT-553
SE SUFFIX
CASE 463B

BLOCK DIAGRAM



MARKING DIAGRAM



L63 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
CM1263-02SE	SOT-553 (Pb-Free)	5000/Tape & Reel

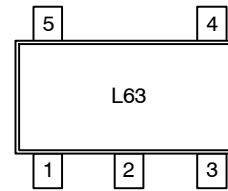
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. PIN DESCRIPTIONS

5-Pin, SOT-553 Package	
Pin	Description
1	V_P
2	V_N
3	NC
4	(CH1) ESD Channel #1
5	(CH2) ESD Channel #2

PACKAGE / PINOUT DIAGRAM



SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage ($V_P - V_N$)	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_N - 0.5)$ to $(V_P + 0.5)$	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

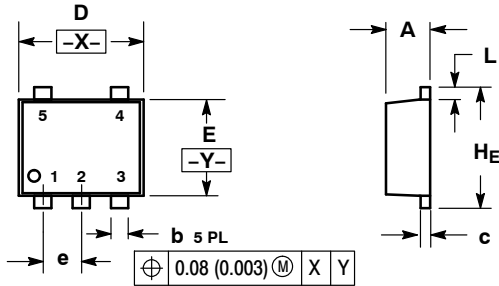
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P	Operating Supply Voltage ($V_P - V_N$)			3.3	5.5	V
I_P	Operating Supply Current	$(V_P - V_N) = 3.3\text{ V}$			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 8\text{ mA}$; $T_A = 25^\circ\text{C}$	0.60 0.60	0.80 0.80	0.95 0.95	V
I_{LEAK}	Channel Leakage Current	$T_A = 25^\circ\text{C}$; $V_P = 5\text{ V}$, $V_N = 0\text{ V}$, $V_{TEST} = 0\text{ to }5\text{ V}$		0.1	1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_P = 3.3\text{ V}$, $V_N = 0\text{ V}$, $V_{IN} = 1.65\text{ V}$		0.85	1.2	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, $V_P = 3.3\text{ V}$, $V_N = 0\text{ V}$, $V_{IN} = 1.65\text{ V}$		0.02		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system: a) Contact Discharge per IEC 61000-4-2 standard b) Air Discharge per IEC 61000-4-2 standard	$T_A = 25^\circ\text{C}$; (Notes 2 and 3) $T_A = 25^\circ\text{C}$; (Note 3)		± 8 ± 15		kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$, $I_{PP} = 1\text{ A}$, $t_P = 8/20\ \mu\text{S}$ (Note 3)		+9.96 -1.6		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1\text{ A}$, $t_P = 8/20\ \mu\text{S}$ Any I/O pin to Ground; (Note 3)		0.96 0.5		Ω

1. All parameters specified at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.
2. Standard IEC 61000-4-2 with $C_{Discharge} = 150\text{ pF}$, $R_{Discharge} = 330\ \Omega$, $V_P = 3.3\text{ V}$, V_N grounded.
3. These measurements performed with no external capacitor on V_P (V_P floating).

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PACKAGE DIMENSIONS

SOT-553, 5 LEAD
CASE 463B-01
ISSUE B

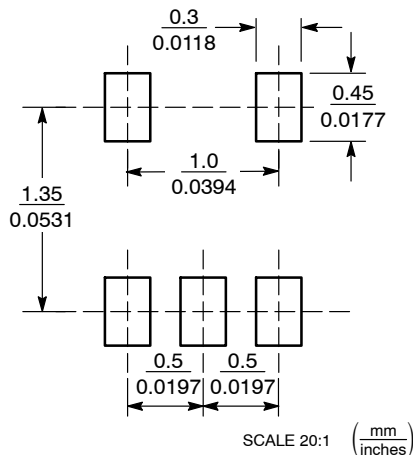


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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