LM339, LM239, LM2901, LM2901V, NCV2901, MC3302

Single Supply Quad Comparators

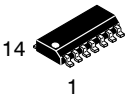
These comparators are designed for use in level detection, low−level sensing and memory applications in consumer, automotive, and industrial electronic applications.

Features

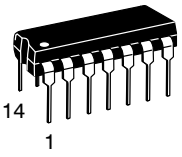
- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage
- Input Common Mode Voltage Range to GND
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

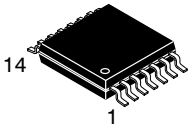
http://onsemi.com



SOIC−14
D SUFFIX
CASE 751A

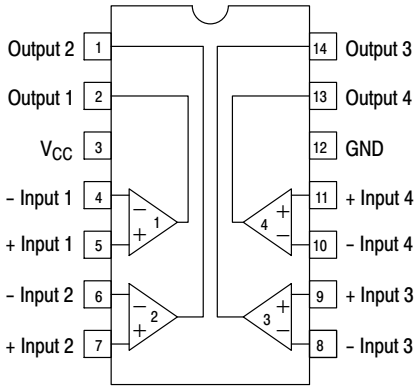


PDIP−14
N, P SUFFIX
CASE 646



TSSOP−14
DTB SUFFIX
CASE 948G

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

DEVICE MARKING INFORMATION

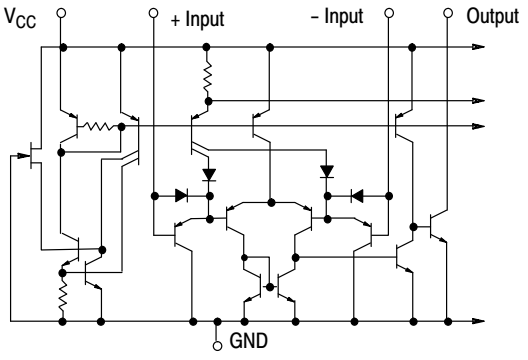
See general marking information in the device marking section on page 8 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage LM239/LM339/LM2901, V MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM239/LM339/LM2901, V MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	−0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Power Dissipation @ T_A = 25°C Plastic Package Derate above 25°C	P_D $1/R_{\theta JA}$	 1.0 8.0	 W mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range LM239 MC3302 LM2901 LM2901V, NCV2901 LM339	T_A	 −25 to +85 −40 to +85 −40 to +105 −40 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Protection at any Pin (Note 2) Human Body Model Machine Model	V_{ESD}	 1500 200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. V_{ESD} rating for NCV/SC devices is: Human Body Model − 2000 V; Machine Model − 200 V.



NOTE: Diagram shown is for 1 comparator.

Figure 1. Circuit Schematic

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

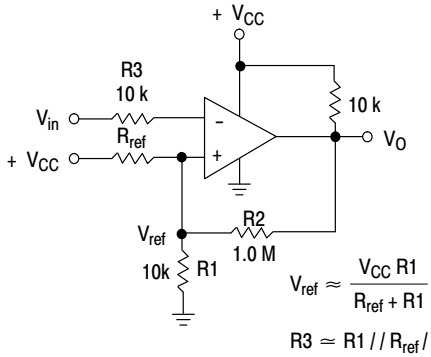
Characteristic	Symbol	LM239/339			LM2901/2901V/ NCV2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	±2.0	±5.0	–	±2.0	±7.0	–	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	25	250	–	25	250	–	25	500	nA
Input Offset Current (Note 4)	I_{IO}	–	±5.0	±50	–	±5.0	±50	–	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	V
Supply Current	I_{CC}										mA
R_L = ∞ (For All Comparators)		–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	
R_L = ∞, V_{CC} = 30 Vdc		–	1.0	2.5	–	1.0	2.5	–	1.0	2.5	
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	–	25	100	–	25	100	–	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	300	–	–	300	–	–	300	–	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	1.3	–	–	1.3	–	–	1.3	–	μs
Output Sink Current V_I (–) ≥ +1.0 Vdc, V_I(+) = 0, V_O ≤ 1.5 Vdc	I_{Sink}	6.0	16	–	6.0	16	–	6.0	16	–	mA
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	130	400	–	130	400	–	130	500	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = +5.0 Vdc	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	nA

3. (LM239) T_{low} = –25°C, T_{high} = +85°
   (LM339) T_{low} = 0°C, T_{high} = +70°C
   (MC3302) T_{low} = –40°C, T_{high} = +85°C
   (LM2901) T_{low} = –40°C, T_{high} = +105°
   (LM2901V & NCV2901) T_{low} = –40°C, T_{high} = +125°C
   NCV2901 is qualified for automotive use.
4. At the output switch point, $V_O \simeq$ 1.4 Vdc, R_S ≤ 100 Ω 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 7])

Characteristic	Symbol	LM239/339			LM2901/2901V/ NCV2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 8)	V_{IO}	–	–	±9.0	–	–	±15	–	–	±40	mVdc
Input Bias Current (Notes 8, 9) (Output in Analog Range)	I_{IB}	–	–	400	–	–	500	–	–	1000	nA
Input Offset Current (Note 8)	I_{IO}	–	–	±150	–	–	±200	–	–	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	V
Saturation Voltage $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $I_{sink} \leq 4.0$ mA	V_{sat}	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current $V_I(+) \geq +1.0$ Vdc, $V_I(-) = 0$, V_O = 30 Vdc	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	μA
Differential Input Voltage All $V_I \geq 0$ Vdc	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	Vdc

7. (LM239) T_{low} = –25°C, T_{high} = +85°
   (LM339) T_{low} = 0°C, T_{high} = +70°C
   (MC3302) T_{low} = –40°C, T_{high} = +85°C
   (LM2901) T_{low} = –40°C, T_{high} = +105°
   (LM2901V & NCV2901) T_{low} = –40°C, T_{high} = +125°C
   NCV2901 is qualified for automotive use.
8. At the output switch point, $V_O \simeq$ 1.4 Vdc, $R_S \leq 100\ \Omega$ 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
9. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
10. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.



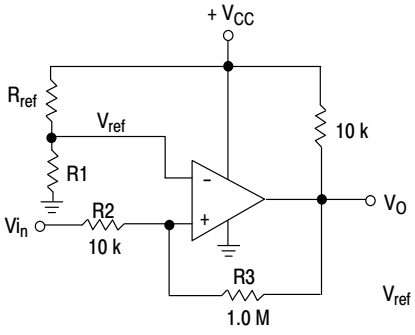
$$V_{ref} \simeq \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$$R3 \simeq R1\ //\ R_{ref}\ //\ R2$$

$$V_H = \frac{R1\ //\ R_{ref}}{R1//\ R_{ref} + R2}\ [V_{O(max)} - V_{O(min)}]$$

$$R2 \gg Rref\ //\ R1$$

Figure 2. Inverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$$R2 \simeq R1\ //\ R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\ [(V_{O(max)} - V_{O(min)}]$$

Figure 3. Noninverting Comparator with Hysteresis

Typical Characteristics
(V_{CC} = 15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

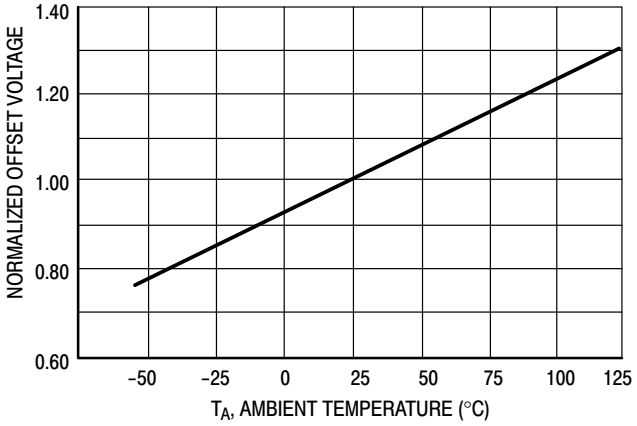


Figure 4. Normalized Input Offset Voltage

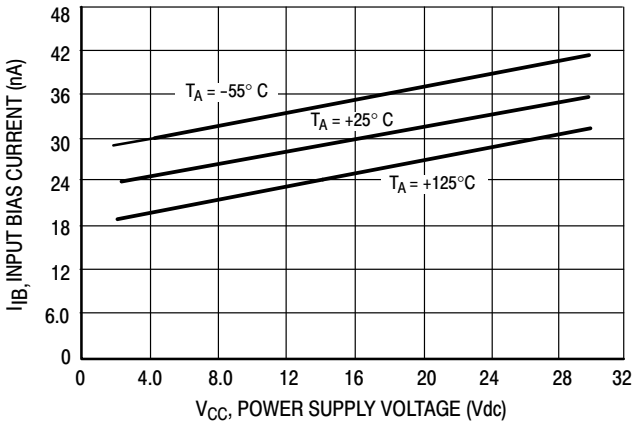


Figure 5. Input Bias Current

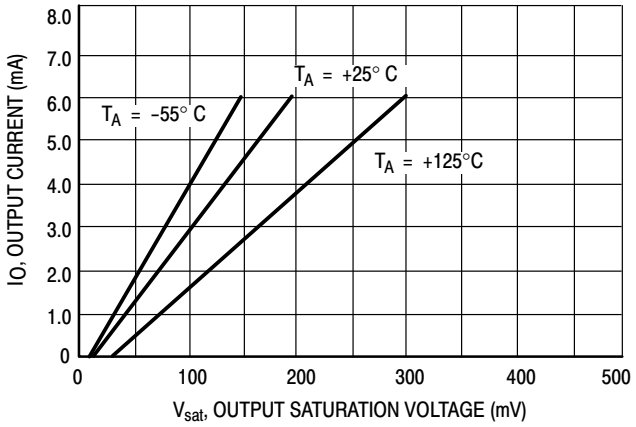
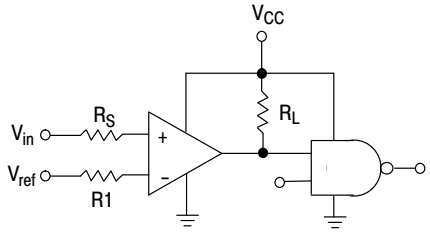


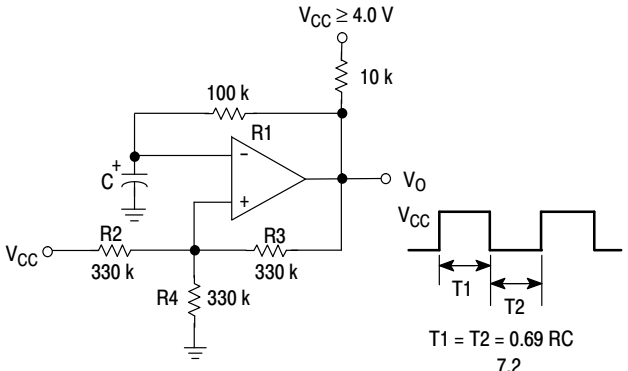
Figure 6. Output Sink Current versus Output Saturation Voltage



R_S = Source Resistance
R1 ≃ R_S

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 7. Driving Logic



T1 = T2 = 0.69 RC

$$f \approx \frac{7.2}{C(\mu F)}$$

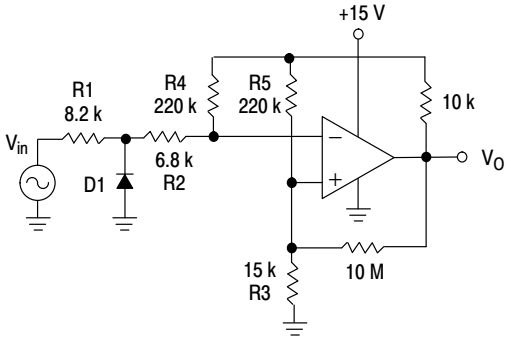
R2 = R3 = R4
R1 ≈ R2 // R3 // R4

Figure 8. Squarewave Oscillator

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than −300 mV should not be used.



D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

Figure 9. Zero Crossing Detector (Single Supply)

$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion ($\Delta\theta$).

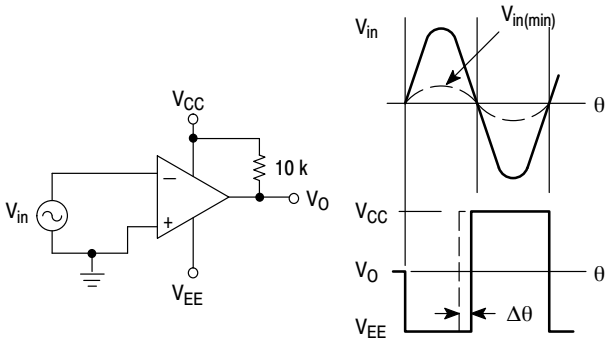


Figure 10. Zero Crossing Detector (Split Supplies)

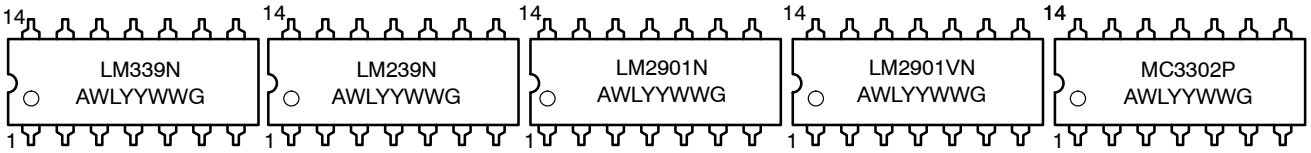
ORDERING INFORMATION

Device	Package	Shipping†
LM239DG	SOIC−14	55 Units/Tube
LM239DR2G	SOIC−14	2500 / Tape & Reel
LM239DTBR2G	TSSOP−14	
LM239NG	PDIP−14	25 Units/Rail
LM339DG	SOIC−14	55 Units/Tube
LM339DR2G	SOIC−14	2500 / Tape & Reel
LM339DTBR2G	TSSOP−14	
LM339NG	PDIP−14	25 Units/Rail
LM2901DG	SOIC−14	55 Units/Rail
LM2901DR2G	SOIC−14	2500 / Tape & Reel
LM2901DTBR2G	TSSOP−14	
LM2901NG	PDIP−14	25 Units/Rail
LM2901VDG	SOIC−14	55 Units/Tube
LM2901VDR2G	SOIC−14	2500 / Tape & Reel
LM2901VDTBR2G	TSSOP−14	
LM2901VNG	PDIP−14	25 Units/Rail
NCV2901DR2G	SOIC−14	2500 / Tape & Reel
NCV2901DTBR2G	TSSOP−14	
NCV2901CTR	Bare Die	6000 / Tape & Reel
MC3302DG	SOIC−14	55 Units/Tube
MC3302DR2G	SOIC−14	2500 / Tape & Reel
MC3302DTBR2G	TSSOP−14	
MC3302PG	PDIP−14	25 Units/Rail

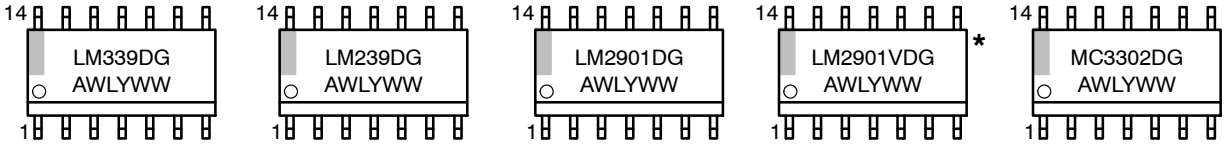
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

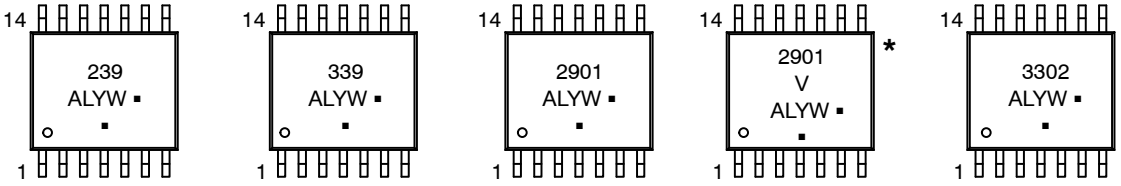
PDIP−14
N, P SUFFIX
CASE 646



SOIC−14
D SUFFIX
CASE 751A



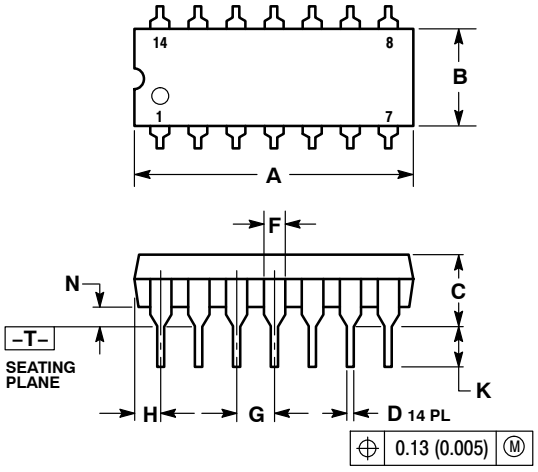
TSSOP−14
DTB SUFFIX
CASE 948G

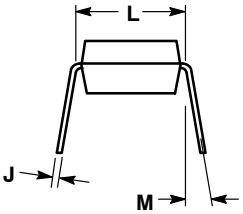


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)
*This marking diagram also applies to NCV2901.

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P



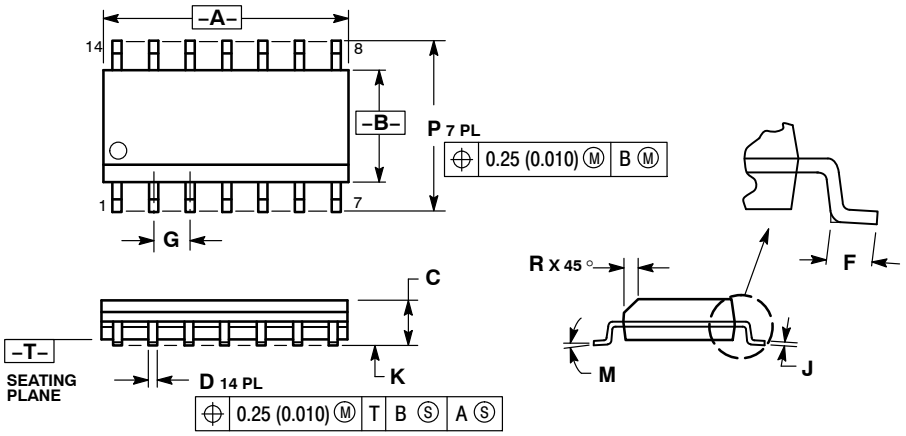


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

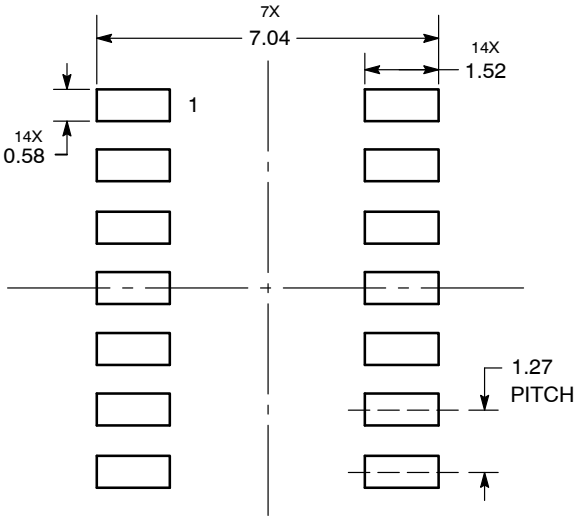
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

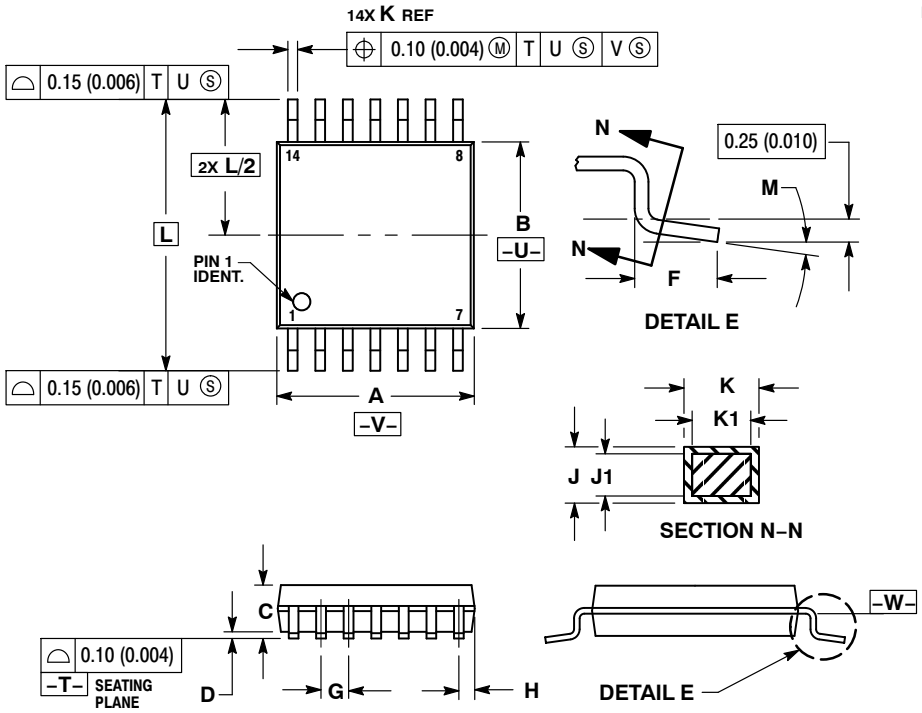


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

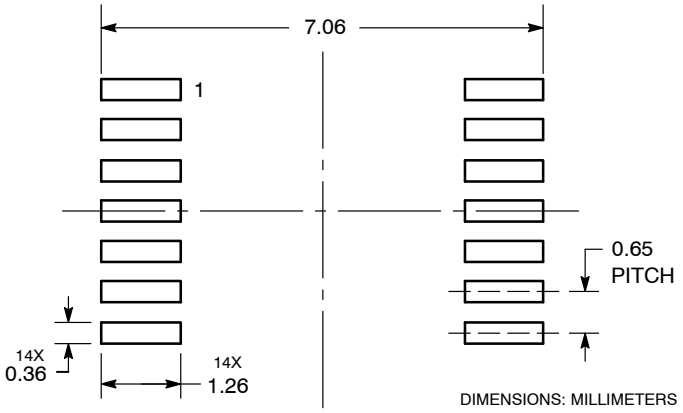
TSSOP−14
CASE 948G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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