

MAC4DLM

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Four-Quadrant Triggering
- Blocking Voltage to 600 V
- On-State Current Rating of 4.0 Amperes RMS at 93°C
- Low Level Triggering and Holding Characteristics
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Pb-Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T _J = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM} , V _{RRM}	600	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T _C = 93°C)	I _{T(RMS)}	4.0	A
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T _J = 110°C)	I _{TSM}	40	A
Circuit Fusing Consideration (t = 8.3 msec)	I ² t	6.6	A ² sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T _C = 93°C)	P _{GM}	2.0	W
Average Gate Power (t = 8.3 msec, T _C = 93°C)	P _{G(AV)}	1.0	W
Peak Gate Current (Pulse Width ≤ 20 μsec, T _C = 93°C)	I _{GM}	4.0	A
Peak Gate Voltage (Pulse Width ≤ 20 μsec, T _C = 93°C)	V _{GM}	5.0	V
Operating Junction Temperature Range	T _J	-40 to 110	°C
Storage Temperature Range	T _{stg}	-40 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

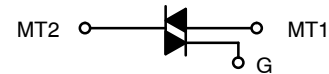
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



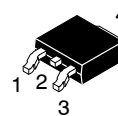
ON Semiconductor®

<http://onsemi.com>

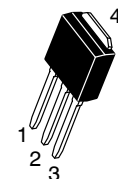
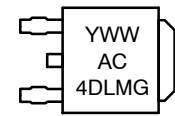
TRIACS 4.0 AMPERES RMS 600 VOLTS



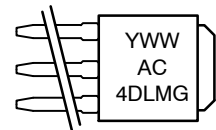
MARKING DIAGRAMS



**DPAK
CASE 369C
STYLE 6**



**DPAK-3
CASE 369D
STYLE 6**



Y = Year
WW = Work Week
AC4DLM = Device Code
G = Pb-Free Package

PIN ASSIGNMENT

1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAC4DLM

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction-to-Case – Junction-to-Ambient – Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.5 88 80	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes (Note 3)	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}$, V_{RRM} , Gate Open)	I_{DRM} , I_{RRM}	–	–	0.01	mA
		–	–	2.0	

ON CHARACTERISTICS

Peak On-State Voltage (Note 4) – ($I_{TM} = \pm 6.0 \text{ A}$)	V_{TM}	–	1.3	1.6	V
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ V}$, $R_L = 100 \Omega$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–) MT2(–), G(+)	I_{GT}	–	1.8 2.1 2.4 4.2	3.0 3.0 3.0 5.0	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ V}$, $R_L = 100 \Omega$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–) MT2(–), G(+)	V_{GT}	0.5 0.5 0.5 0.5	0.62 0.57 0.65 0.74	1.3 1.3 1.3 1.3	V
Gate Non-Trigger Voltage ($V_D = 12 \text{ V}$, $R_L = 100 \Omega$, $T_J = 110^{\circ}\text{C}$) MT2(+), G(+); MT2(+), G(–); MT2(–), G(–); MT2(–), G(+)	V_{GD}	0.1	0.4	–	V
Holding Current ($V_D = 12 \text{ V}$, Gate Open, Initiating Current = $\pm 200 \text{ mA}$)	I_H	–	1.5	15	mA
Latching Current MT2(+), G(+) ($V_D = 12 \text{ V}$, $I_G = 5.0 \text{ mA}$) MT2(+), G(–) ($V_D = 12 \text{ V}$, $I_G = 5.0 \text{ mA}$) MT2(–), G(–) ($V_D = 12 \text{ V}$, $I_G = 5.0 \text{ mA}$) MT2(–), G(+) ($V_D = 12 \text{ V}$, $I_G = 10 \text{ mA}$)	I_L	–	1.75 5.2 2.1 2.2	10 10 10 10	mA

DYNAMIC CHARACTERISTICS

Rate of Change of Commutating Current ($V_D = 200 \text{ V}$, $I_{TM} = 1.8 \text{ A}$, Commutating $dv/dt = 1.0 \text{ V}/\mu\text{sec}$, $T_J = 110^{\circ}\text{C}$, $f = 250 \text{ Hz}$, $CL = 5.0 \mu\text{fd}$, $LL = 80 \text{ mH}$, $RS = 56 \Omega$, $CS = 0.03 \mu\text{fd}$) With snubber see Figure 11	$di/dt(c)$	–	3.0	–	A/ms
Critical Rate of Rise of Off-State Voltage ($V_D = 0.67 \times \text{Rated } V_{DRM}$, Exponential Waveform, Gate Open, $T_J = 110^{\circ}\text{C}$)	dv/dt	10	–	–	V/ μs

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.
3. 1/8" from case for 10 seconds.
4. Pulse Test: Pulse Width $\leq 2.0 \text{ msec}$, Duty Cycle $\leq 2\%$.

ORDERING INFORMATION

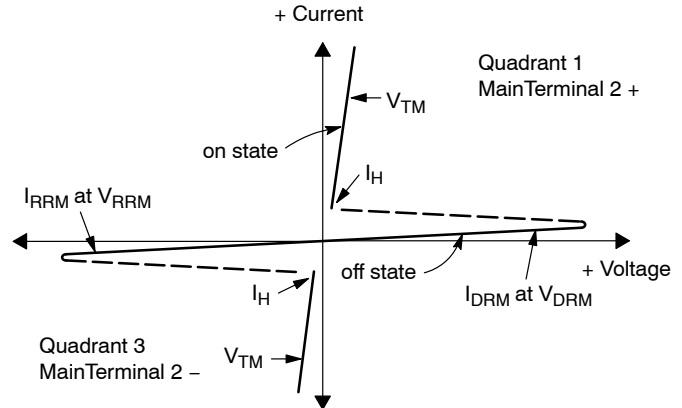
Device	Package Type	Package	Shipping†
MAC4DLM-001	DPAK-3	369D	75 Units / Rail
MAC4DLM-001G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MAC4DLMT4	DPAK	369C	2500 / Tape & Reel
MAC4DLMT4G	DPAK (Pb-Free)	369C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

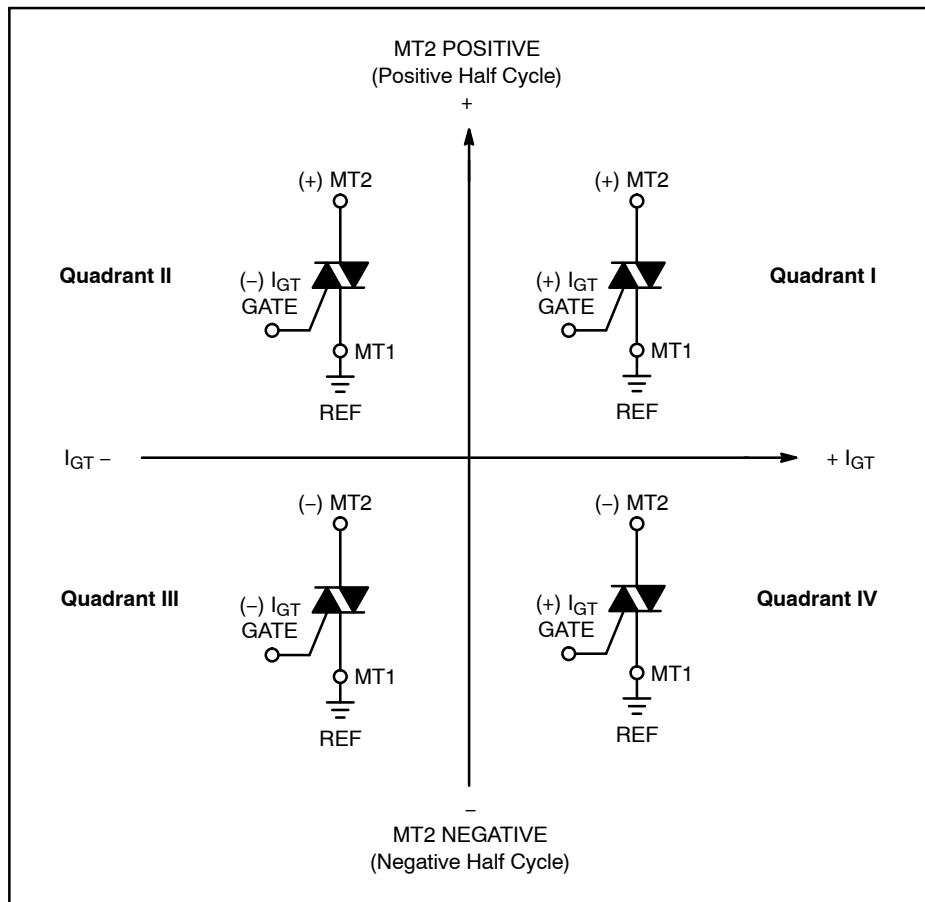
MAC4DLM

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off-State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off-State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On-State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used.

MAC4DLM

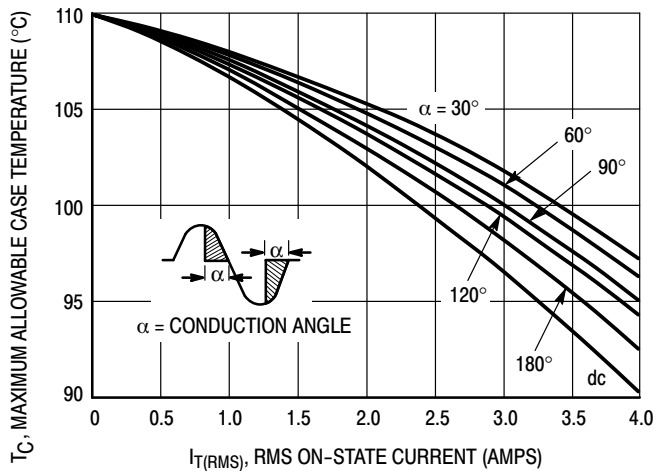


Figure 1. RMS Current Derating

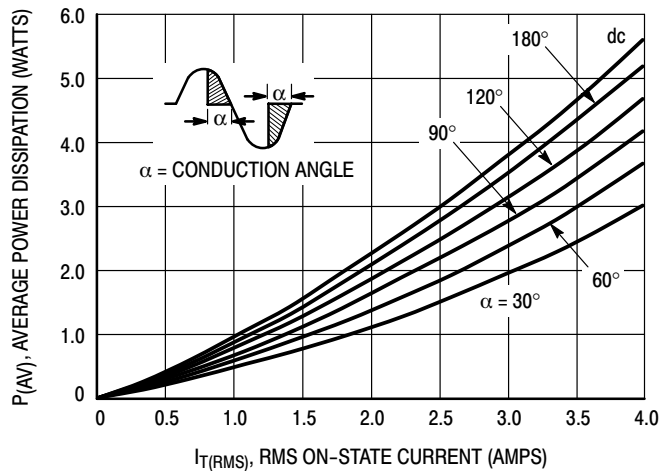


Figure 2. On-State Power Dissipation

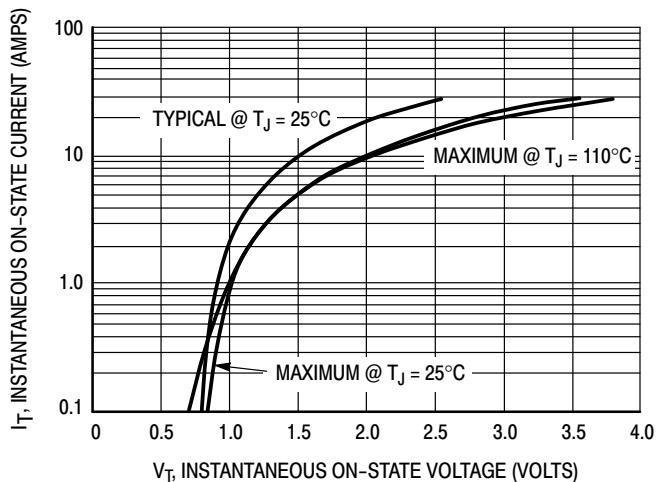


Figure 3. On-State Characteristics

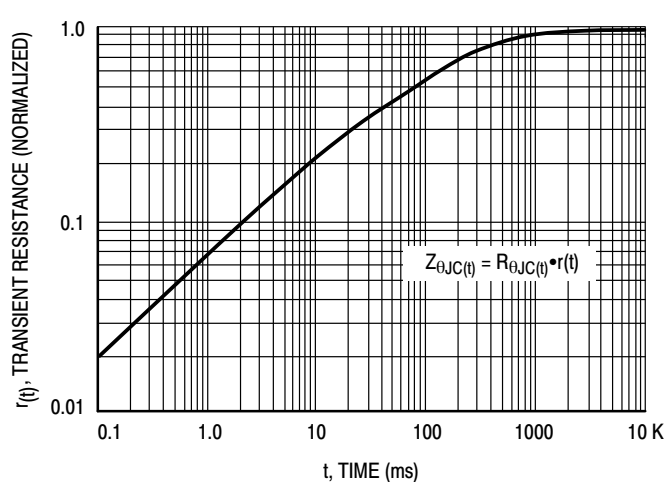


Figure 4. Transient Thermal Response

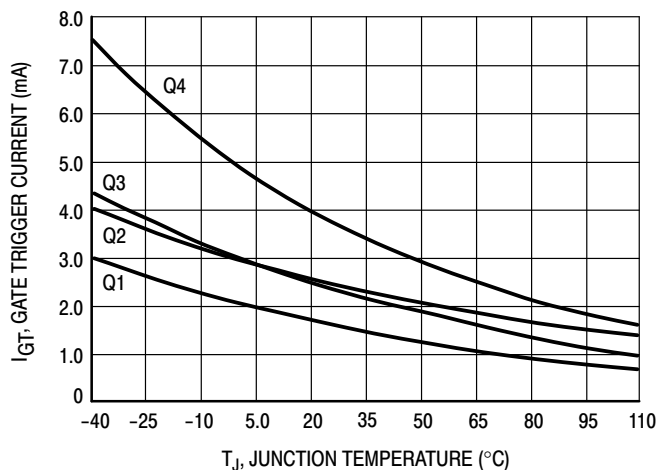


Figure 5. Typical Gate Trigger Current versus Junction Temperature

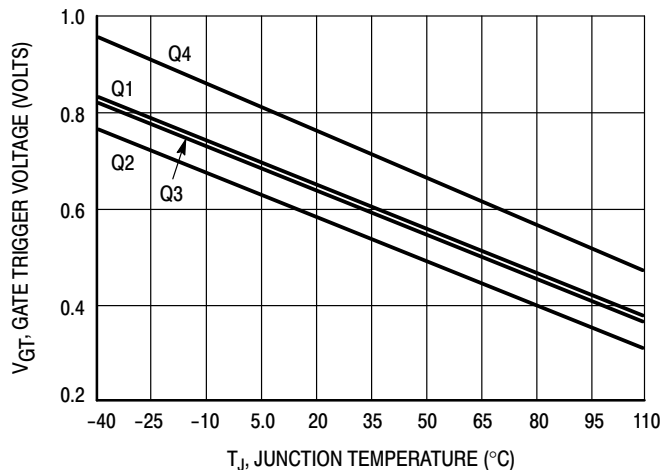


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

MAC4DLM

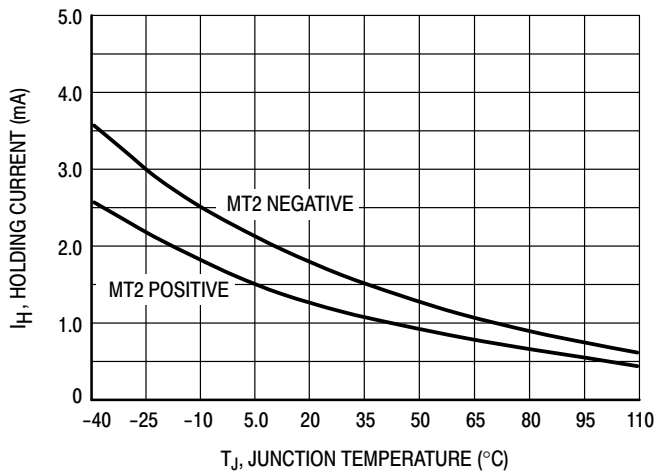


Figure 7. Typical Holding Current versus Junction Temperature

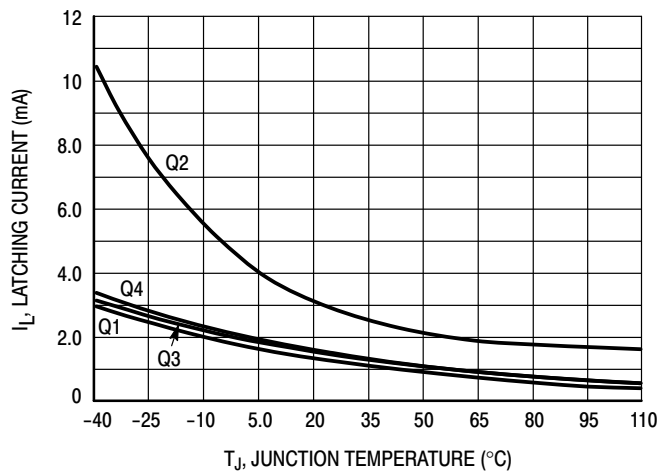


Figure 8. Typical Latching Current versus Junction Temperature

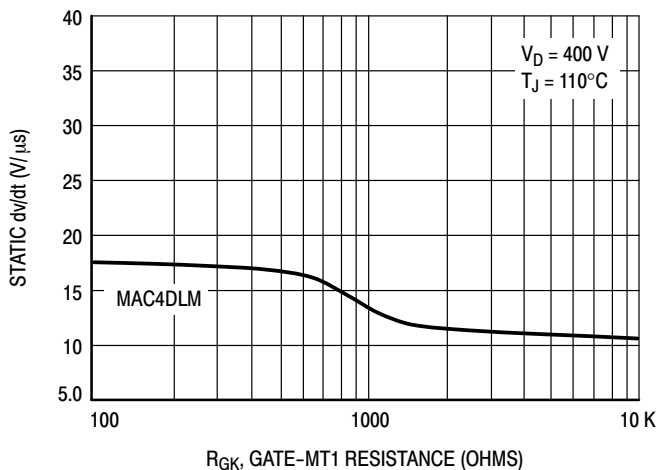


Figure 9. Minimum Exponential Static dv/dt versus Gate-MT1 Resistance

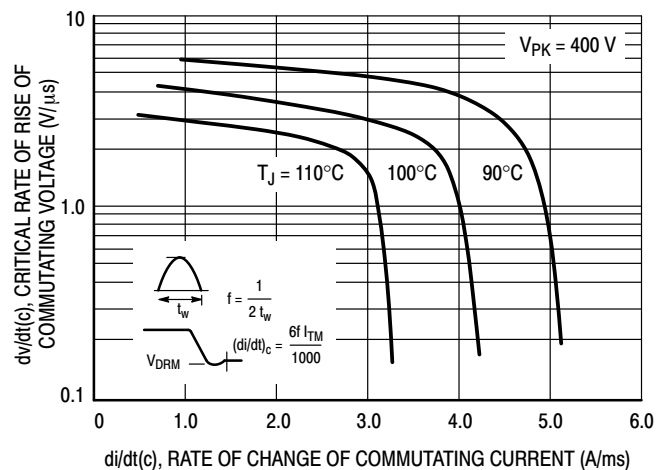
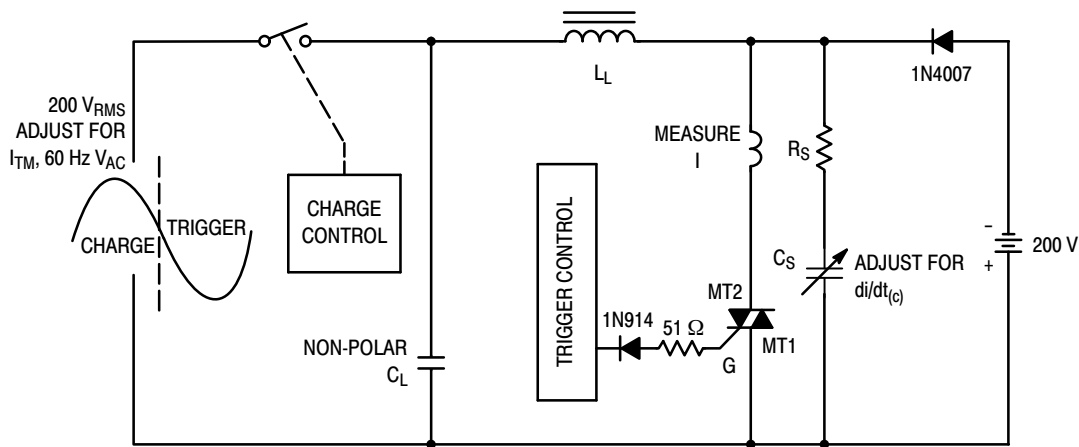


Figure 10. Critical Rate of Rise of Commutating Voltage



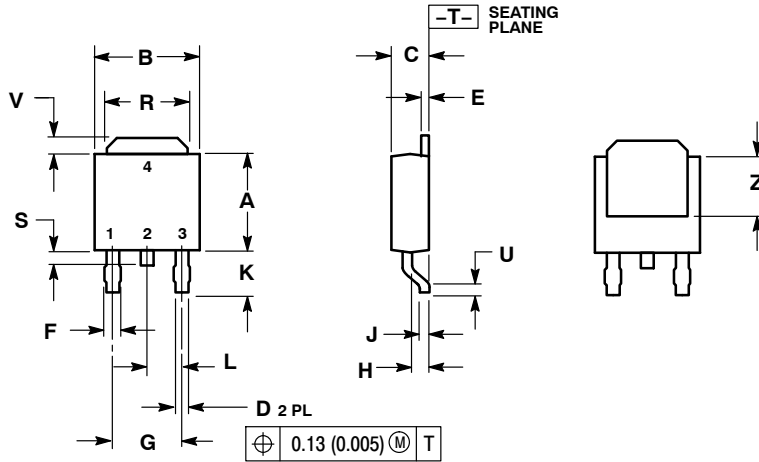
Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Figure 11. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$

MAC4DLM

PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

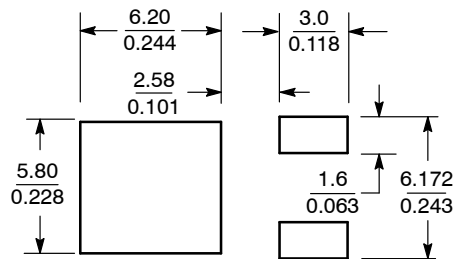


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

SOLDERING FOOTPRINT*



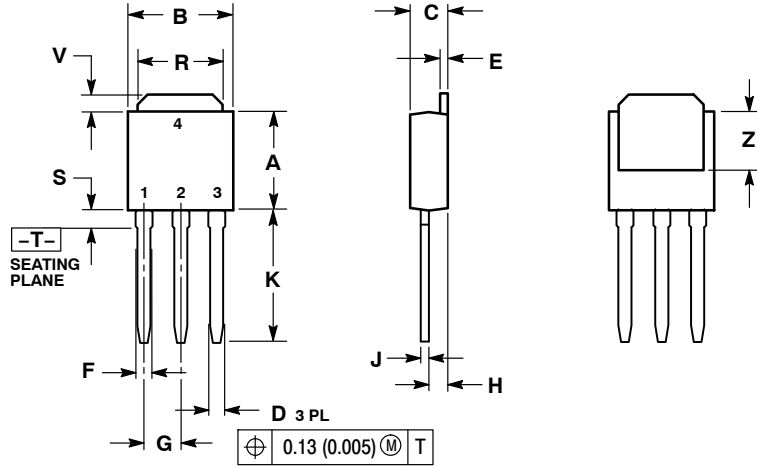
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAC4DLM

PACKAGE DIMENSIONS

DKPAK-3
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:

- PIN 1. MT1
2. MT2
3. GATE
4. MT2

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative