MC100E241

5V ECL 8-Bit Scannable Register

ON Semiconductor®

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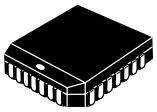


PLCC−28
FN SUFFIX
CASE 776

Description

The MC100E241 is an 8-bit shiftable register. Unlike a standard universal shift register such as the E141, the E241 features internal data feedback organized so that the SHIFT control overrides the HOLD/$\overline{\text{LOAD}}$ control. This enables the normal operations of HOLD and LOAD to be toggled with a single control line without the need for external gating. It also enables switching to scan mode with the single SHIFT control line.

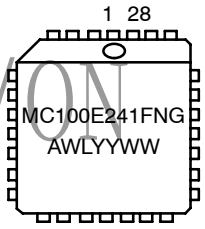
The eight inputs $D_0 - D_7$ accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the positive-going edge of CLK; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

The 100 Series contains temperature compensation.

Features

- SHIFT overrides HOLD/$\overline{\text{LOAD}}$ Control
- 1000 ps Max. CLK to Q
- Asynchronous Master Reset
- Pin-Compatible with E141
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −4.2 V to −5.7 V
- Internal Input 50 kΩ Pulldown Resistors
- ESD Protection: Human Body Model; > 1 kV, Machine Model; > 75 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level:
  Pb = 1
  Pb−Free = 3
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 529 devices
- Pb−Free Packages are Available*

MARKING DIAGRAM*



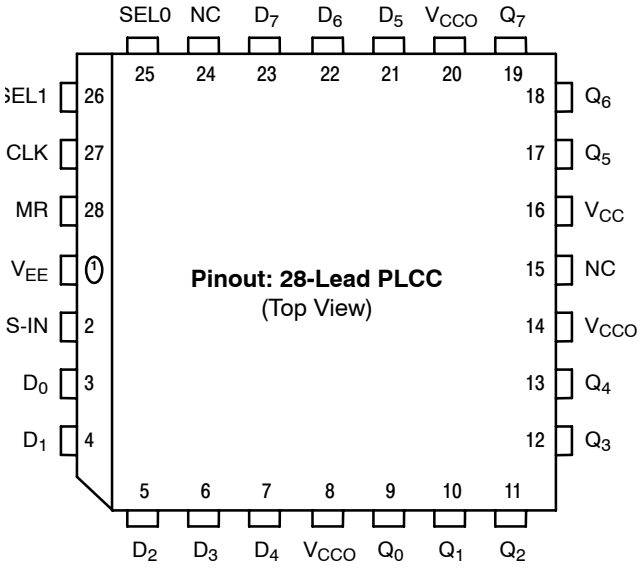
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout Assignment

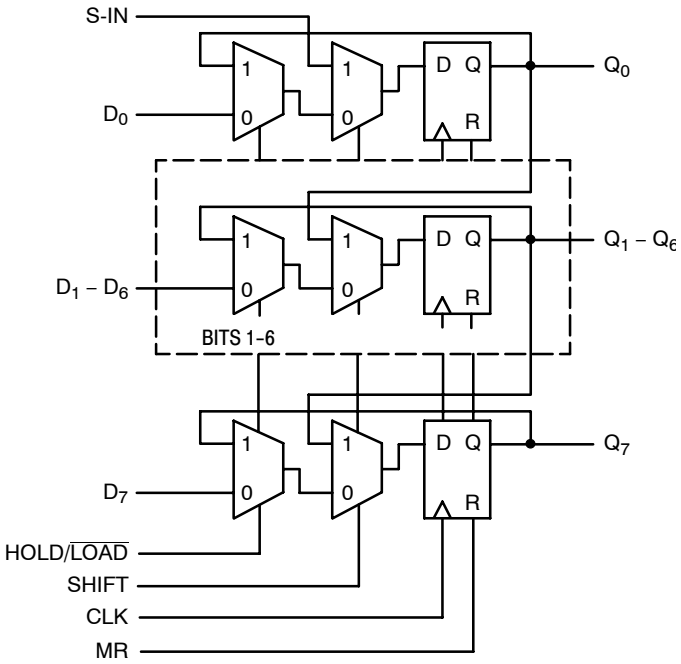


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
$D_0 – D_7$	ECL Parallel Date Inputs
S-IN	ECL Serial Data Inputs
SEL0	ECL SHIFT Control
SEL1	ECL HOLD/$\overline{\text{LOAD}}$ Control
CLK	ECL Clock
MR	ECL Master Reset
$Q_0 – Q_7$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

Table 2. FUNCTION TABLE

MR	SEL0	SEL1	Function
1	X	X	Outputs LOW
0	1	X	Shift Data
0	0	1	Hold Data
0	0	0	Load Data

X = Don't Care

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	PLCC–28 PLCC–28	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	Standard Board	PLCC–28	22 to 26	°C/W
T_{sol}	Wave Solder Pb Pb–Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. 100E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V, V_{EE} = 0.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		125	150		125	150		144	173	mA
V_{OH}	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary –0.46 V / +0.8 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.

Table 5. 100E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 3)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		125	150		125	150		144	173	mA
V_{OH}	Output HIGH Voltage	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	–1165	–1025	–880	–1165	–1025	–880	–1165	–1025	–880	mV
V_{IL}	Input LOW Voltage (Single–Ended)	–1810	–1645	–1475	–1810	–1645	–1475	–1810	–1645	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary –0.46 V / +0.8 V.
4. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.

Table 6. AC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 5)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		900			900			900		GHz
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	CLK	625	750	975	625	750	975	625	750	975	
	MR	600	725	975	600	725	975	600	725	975	
t_s	Setup Time										ps
	D	175	25		175	25		175	25		
	SEL0 (SHIFT)	350	200		350	200		350	200		
	SEL1 (HOLD/$\overline{\text{LOAD}}$)	400	250		400	250		400	250		
	S-IN	125	−100		125	−100		125	−100		
t_h	Hold Time										ps
	D	200	−25		200	−25		200	−25		
	SEL0 (SHIFT)	100	−200		100	−200		100	−200		
	SEL1 (HOLD/$\overline{\text{LOAD}}$)	50	−250		50	−250		50	−250		
	S-IN	300	100		300	100		300	100		
t_{RR}	Reset Recovery Time	900	600		900	600		900	600		ps
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 6)		60			60			60		ps
t_{JITTER}	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	525	800	300	525	800	300	525	800	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. 100 Series: V_{EE} can vary −0.46 V / +0.8 V.
6. Within-device skew is defined as identical transitions on similar paths through a device.

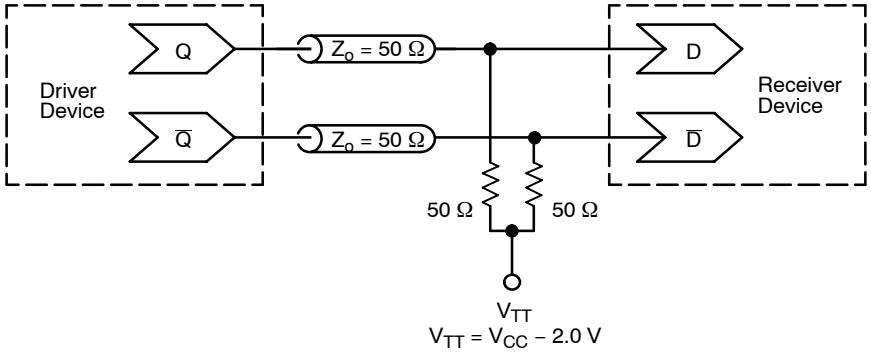


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100E241FN	PLCC–28	37 Units / Rail
MC100E241FNG	PLCC–28 (Pb–Free)	37 Units / Rail
MC100E241FNR2	PLCC–28	500 / Tape & Reel
MC100E241FNR2G	PLCC–28 (Pb–Free)	500 / Tape & Reel

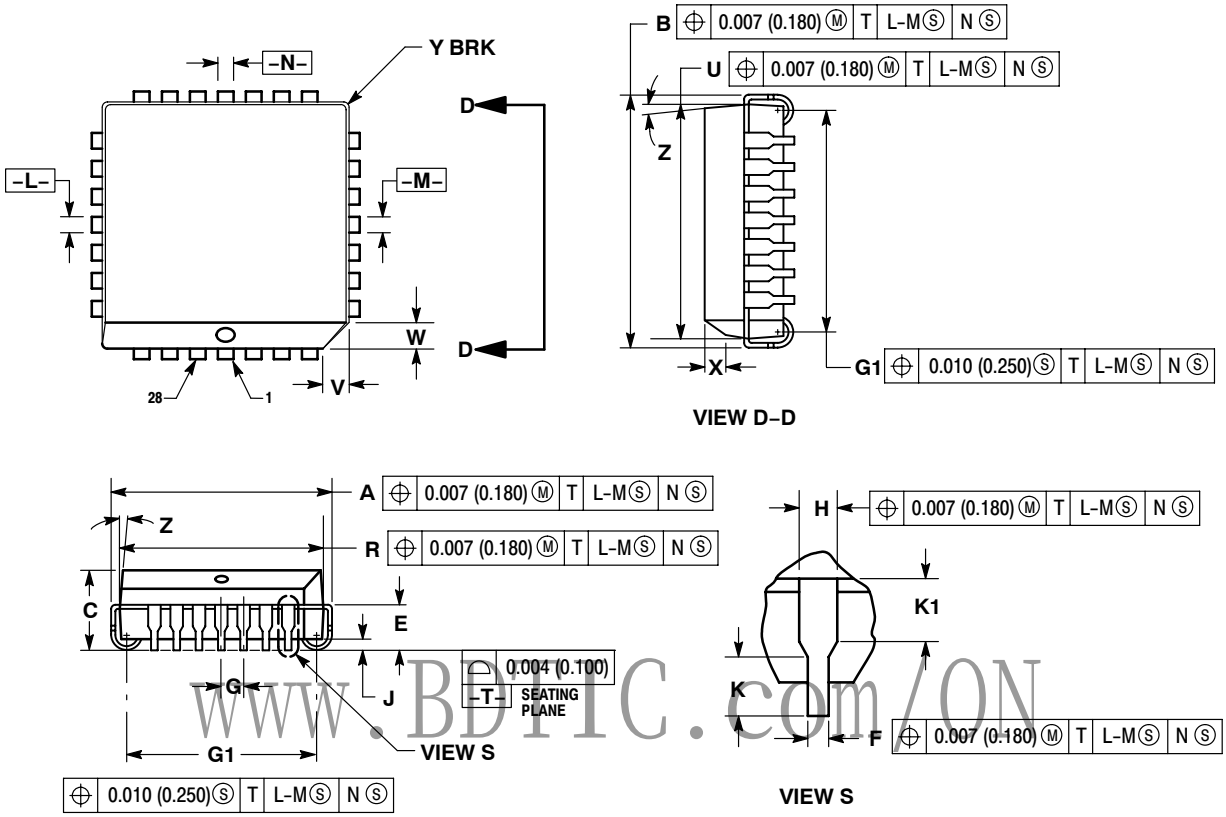
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques
AN1406/D – Designing with PECL (ECL at +5.0 V)
AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D – Metastability and the ECLinPS Family
AN1568/D – Interfacing Between LVDS and ECL
AN1672/D – The ECL Translator Guide
AND8001/D – Odd Number Counters Design
AND8002/D – Marking and Date Codes
AND8020/D – Termination of ECL Logic Devices
AND8066/D – Interfacing with ECLinPS
AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

PUBLICATION ORDERING INFORMATION

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