

# MC100E310

## 5V ECL Low Voltage 2:8 Differential Fanout Buffer

### Description

The MC100E310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The E310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

The lowest TPD delay time results from terminating only one output pair, and the greatest TPD delay time results from terminating all the output pairs. This shift is about 10–20 pS in TPD. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest TPD delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest TPD (delay time) occurs and all outputs display about the same 10 – 20 ps increase in TPD, so the relative skew between any two output pairs remains about 25 ns.

For more information on using PECL, designers should refer to ON Semiconductor Application Note AN1406/D.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also be used as a coupled input. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series Contains Temperature Compensation

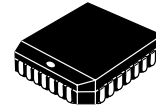
### Features

- Dual Differential Fanout Buffers
- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- 28-lead PLCC Packaging
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- PECL Mode Operating Range:  $V_{CC} = 4.2$  V to 5.7 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -4.2$  V to  $-5.7$  V
- Internal Input 50 k $\Omega$  Pulldown Resistors
- ESD Protection: Human Body Model; >2 kV, Machine Model; >200 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test



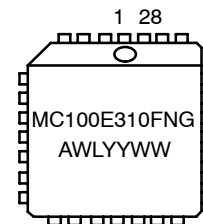
ON Semiconductor®

<http://onsemi.com>



PLCC-28  
FN SUFFIX  
CASE 776

### MARKING DIAGRAM\*



A = Assembly Location  
WJ = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*For additional marking information, refer to Application Note AND8002/D.

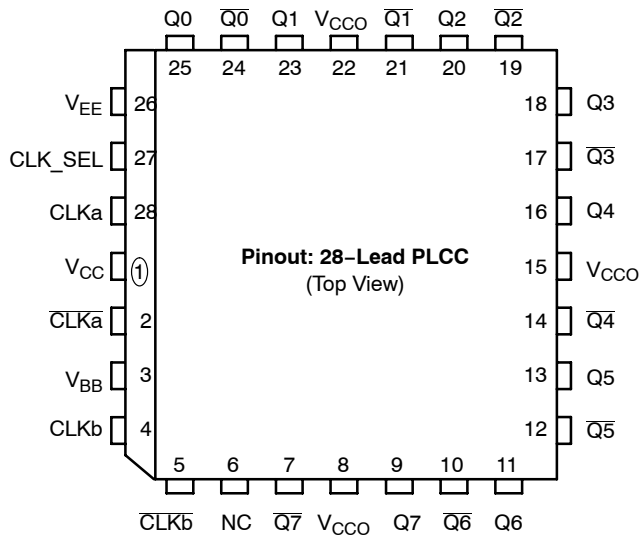
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

- Moisture Sensitivity Level: Pb = 1; Pb-Free = 3  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 212 devices
- Pb-Free Packages are Available\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

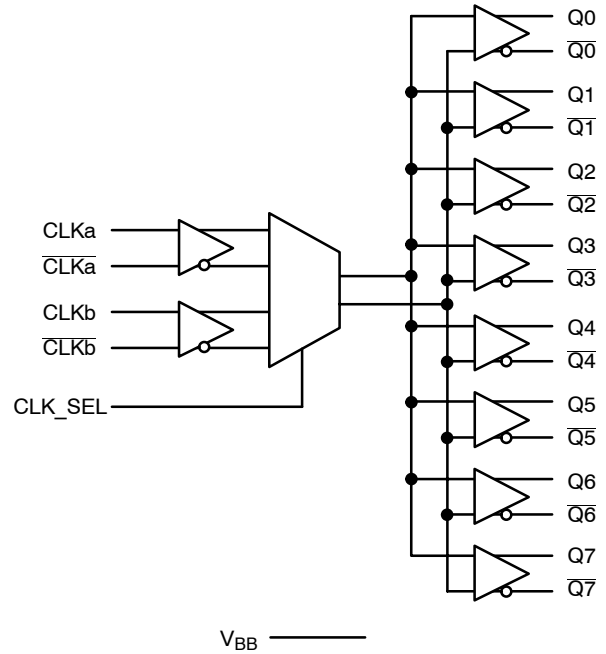
# MC100E310



\* All V<sub>CC</sub> and V<sub>CCO</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub>, V<sub>CCO</sub>, and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout Assignment**



**Figure 2. Logic Symbol**

[www.BDTIC.com/ON](http://www.BDTIC.com/ON)

**Table 1. PIN DESCRIPTION**

| PIN                                | Function                     |
|------------------------------------|------------------------------|
| CLKa, CLKb;<br>CLKa-bar, CLKb-bar  | ECL Differential Input Pairs |
| Q0:7; Q0-bar:7                     | ECL Differential Outputs     |
| CLK_SEL                            | ECL Input Clock Select       |
| V <sub>BB</sub>                    | Reference Voltage Output     |
| V <sub>CC</sub> , V <sub>CCO</sub> | Positive Supply              |
| V <sub>EE</sub>                    | Negative Supply              |
| NC                                 | No Connect                   |

**Table 2. FUNCTION TABLE**

| PIN | Function      |
|-----|---------------|
| 0   | CLKa Selected |
| 1   | CLKb Selected |

# MC100E310

**Table 3. MAXIMUM RATINGS**

| Symbol        | Parameter  | Condition 1                                    | Condition 2                            | Rating       | Unit   |
|---------------|--|--|--|--------------|--|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0\text{ V}$                          |  | 8            | V  |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>-6      | V<br>V   |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100    | mA<br>mA   |
| $I_{BB}$      | $V_{BB}$ Sink/Source                               |  |  | $\pm 0.5$    | mA   |
| $T_A$         | Operating Temperature Range                        |  |  | 0 to +85     | $^{\circ}\text{C}$   |
| $T_{stg}$     | Storage Temperature Range                          |  |  | -65 to +150  | $^{\circ}\text{C}$   |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | PLCC-28<br>PLCC-28                     | 63.5<br>43.5 | $^{\circ}\text{C}/\text{W}$<br>$^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | PLCC-28                                | 22 to 26     | $^{\circ}\text{C}/\text{W}$                                |
| $T_{sol}$     | Wave Solder<br>Pb<br>Pb-Free                       |  |  | 265<br>265   | $^{\circ}\text{C}$   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

[www.BDTIC.com/ON](http://www.BDTIC.com/ON)

# MC100E310

**Table 4. 100E SERIES PECL DC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1)

| Symbol      | Characteristic   | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
|             |  | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current   |       | 55   | 60   |      | 55   | 60   |      | 65   | 70   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)   | 3915  | 3995 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)  | 3170  | 3305 | 3445 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 3835  | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 3190  | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 3.62  |      | 3.74 | 3.62 |      | 3.74 | 3.62 |      | 3.74 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.7   |      | 4.6  | 2.7  |      | 4.6  | 2.7  |      | 4.6  | V             |
| $I_{IH}$    | Input HIGH Current   |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   | 0.3  |      | 0.5  | 0.25 |      | 0.5  | 0.2  |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

**Table 5. 100E SERIES NECL DC CHARACTERISTICS**  $V_{CCx} = 0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 4)

| Symbol      | Characteristic   | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |  | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current   |       | 55    | 60    |       | 55    | 60    |       | 65    | 70    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 5)   | -1185 | -1005 | -880  | -1025 | -950  | -880  | -1025 | -950  | -880  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 5)  | -1830 | -1695 | -1555 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | -1165 | -1025 | -880  | -1165 | -1025 | -880  | -1165 | -1025 | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV            |
| $V_{BB}$    | Output Voltage Reference   | -1.38 |       | -1.26 | -1.38 |       | -1.26 | -1.38 |       | -1.26 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) | -2.3  |       | -0.4  | -2.3  |       | -0.4  | -2.3  |       | -0.4  | V             |
| $I_{IH}$    | Input HIGH Current   |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   | 0.3   |       | 0.5   | 0.25  |       | 0.5   | 0.2   |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .
5. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
6.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

# MC100E310

**Table 6. AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0\text{ V}$  or  $V_{CCx} = 0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 7)

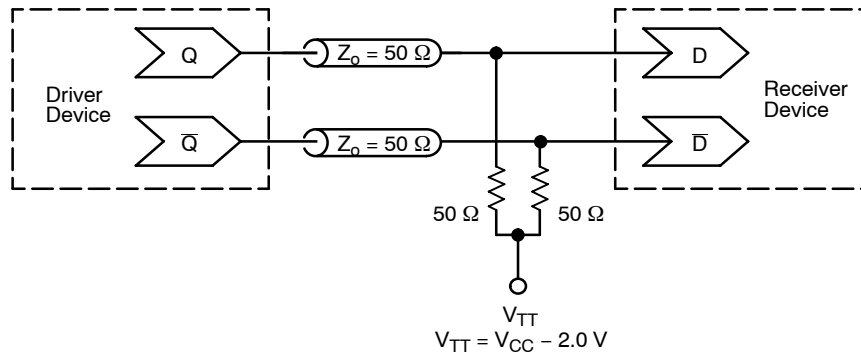
| Symbol                 | Characteristic  | -40°C      |     |            | 25°C       |     |            | 85°C       |     |            | Unit |
|------------------------|---|------------|-----|------------|------------|-----|------------|------------|-----|------------|------|
|                        |   | Min        | Typ | Max        | Min        | Typ | Max        | Min        | Typ | Max        |      |
| $f_{MAX}$              | Maximum Toggle Frequency  | 700        | 900 |            | 700        | 900 |            | 700        | 900 |            | MHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>IN (differential) (Note 8)<br>IN (single-ended) (Note 9) | 525<br>500 |     | 725<br>750 | 550<br>550 |     | 750<br>800 | 575<br>600 |     | 775<br>850 | ps   |
| $t_{skew}$             | Within-Device Skew (Note 10)<br>Part-to-Part Skew (Diff)                                |            |     | 75<br>250  |            |     | 50<br>200  |            |     | 50<br>200  | ps   |
| $t_{JITTER}$           | Random Clock Jitter (RMS)   |            | < 1 |            |            | < 1 |            |            | < 1 |            | ps   |
| $V_{PP}$               | Input Voltage Swing<br>(Differential Configuration)                                     | 500        |     |            | 500        |     |            | 500        |     |            | mV   |
| $t_r/t_f$              | Output Rise/Fall Time<br>(20%–80%)  | 200        |     | 600        | 200        |     | 600        | 200        |     | 600        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7.  $V_{EE}$  can vary  $-0.46\text{ V}$  /  $+0.8\text{ V}$ .
8. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the ON Semiconductor High Performance ECL Data Book (DL140/D).
9. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
10. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

[www.BDTIC.com/ON](http://www.BDTIC.com/ON)

## MC100E310



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device         | Package              | Shipping†         |
|----------------|----------------------|-------------------|
| MC100E310FN    | PLCC-28              | 37 Units / Rail   |
| MC100E310FNG   | PLCC-28<br>(Pb-Free) | 37 Units / Rail   |
| MC100E310FNR2  | PLCC-28              | 500 / Tape & Reel |
| MC100E310FNR2G | PLCC-28<br>(Pb-Free) | 500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

[www.BDTIC.com/ON](http://www.BDTIC.com/ON)

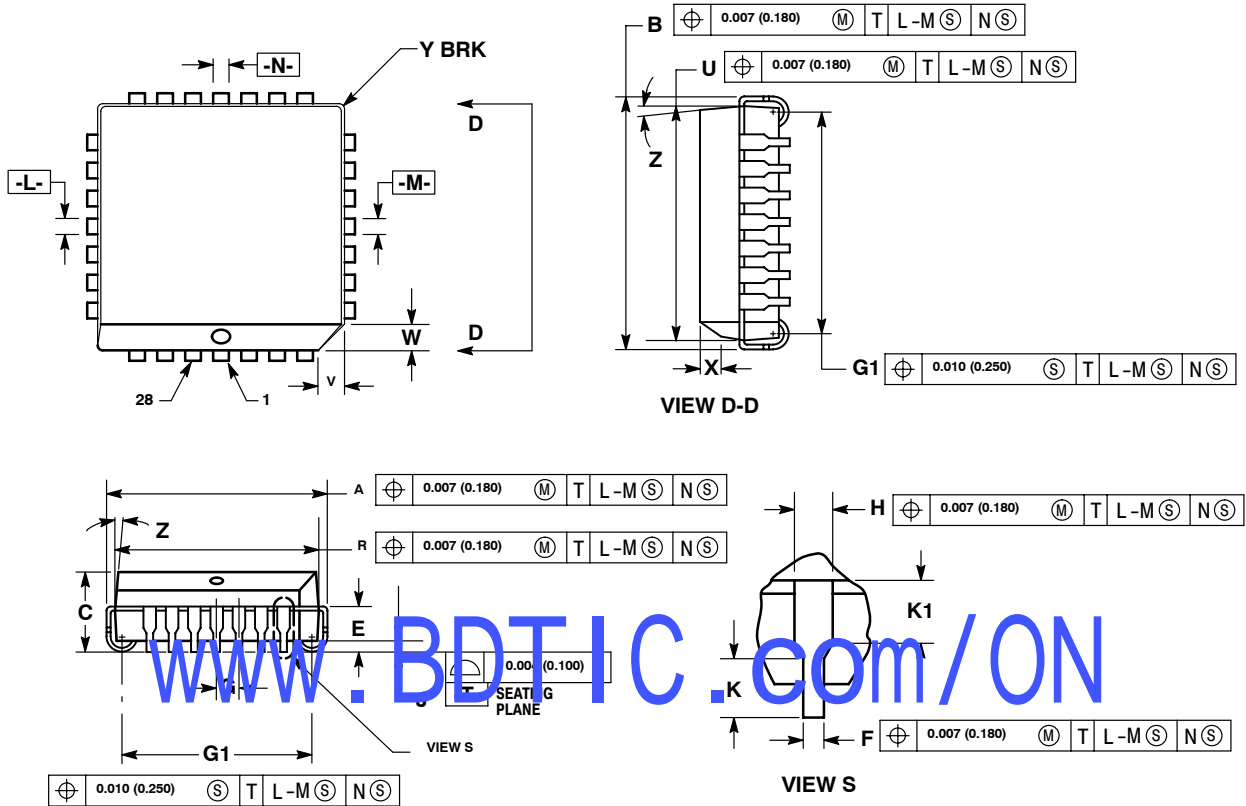
#### Resource Reference of Application Notes

- AN 404/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100E310

## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



**NOTES:**

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.485     | 0.495 | 12.32       | 12.57 |
| B   | 0.485     | 0.495 | 12.32       | 12.57 |
| C   | 0.165     | 0.180 | 4.20        | 4.57  |
| E   | 0.090     | 0.110 | 2.29        | 2.79  |
| F   | 0.013     | 0.019 | 0.33        | 0.48  |
| G   | 0.050 BSC |       | 1.27 BSC    |       |
| H   | 0.026     | 0.032 | 0.66        | 0.81  |
| J   | 0.020     | —     | 0.51        | —     |
| K   | 0.025     | —     | 0.64        | —     |
| R   | 0.450     | 0.456 | 11.43       | 11.58 |
| U   | 0.450     | 0.456 | 11.43       | 11.58 |
| V   | 0.042     | 0.048 | 1.07        | 1.21  |
| W   | 0.042     | 0.048 | 1.07        | 1.21  |
| X   | 0.042     | 0.056 | 1.07        | 1.42  |
| Y   | —         | 0.020 | —           | 0.50  |
| Z   | 2° 10°    |       | 2° 10°      |       |
| G1  | 0.410     | 0.430 | 10.42       | 10.92 |
| K1  | 0.040     | —     | 1.02        | —     |

[www.BDTIC.com/ON](http://www.BDTIC.com/ON)

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

##### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative

[www.BDTIC.com/ON/](http://www.BDTIC.com/ON/) MC100E310/D