

MC100EP809

3.3V 1:9 Differential HSTL/PECL/LVDS to HSTL Clock Driver with LVTTTL Clock Select and Enable

Description

The MC100EP809 is a low skew 1-to-9 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are one differential HSTL and one differential LVPECL. Both input pairs can accept LVDS levels. They are selected by the CLK_SEL pin which is LVTTTL. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable (OE), which is LVTTTL, is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (Figure 9).

The MC100EP809 guarantees low output-to-output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot. The MC100EP809 output structure uses open emitter architecture and will be terminated with 50 Ω to ground instead of a standard HSTL configuration (Figure 7). To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

Designers can take advantage of the EP809's performance to distribute low skew clocks across the backplane of the board. Both clock inputs may be single-end driven by biasing the non-driven pin in an input pair (Figure 8).

Features

- 100 ps Typical Device-to-Device Skew
- 15 ps Typical within Device Skew
- HSTL Compatible Outputs Drive 50 Ω to GND with no Offset Voltage
- Maximum Frequency > 750 MHz
- 850 ps Typical Propagation Delay
- Fully Compatible with Micrel SY9809L
- PECL and HSTL Mode Operating Range: $V_{CCI} = 3\text{ V to }3.6\text{ V}$ with $GND = 0\text{ V}$, $V_{CCO} = 1.6\text{ V to }2.0\text{ V}$
- Open Input Default State
- Pb-Free Packages are Available



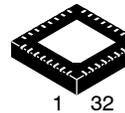
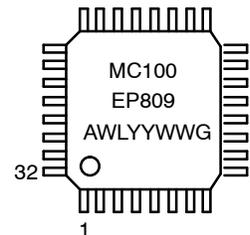
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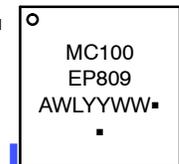
MARKING DIAGRAMS*



32-LEAD LQFP
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM



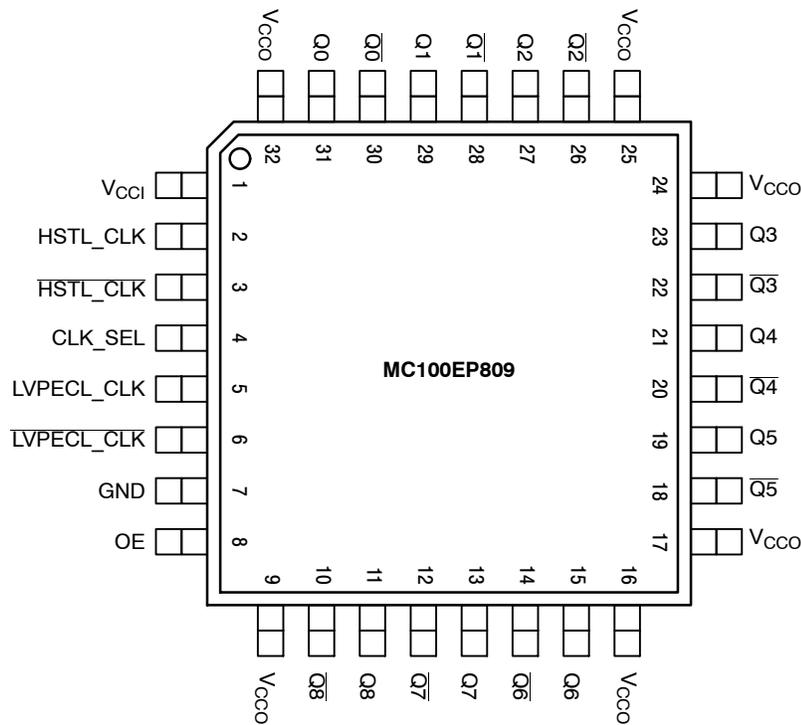
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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All V_{CCI}, V_{CCO}, and GND pins must be externally connected to appropriate Power Supply to guarantee proper operation (V_{CCI} ≠ V_{CCO}).

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Figure 1. 32-Lead QFP Pinout (Top View)

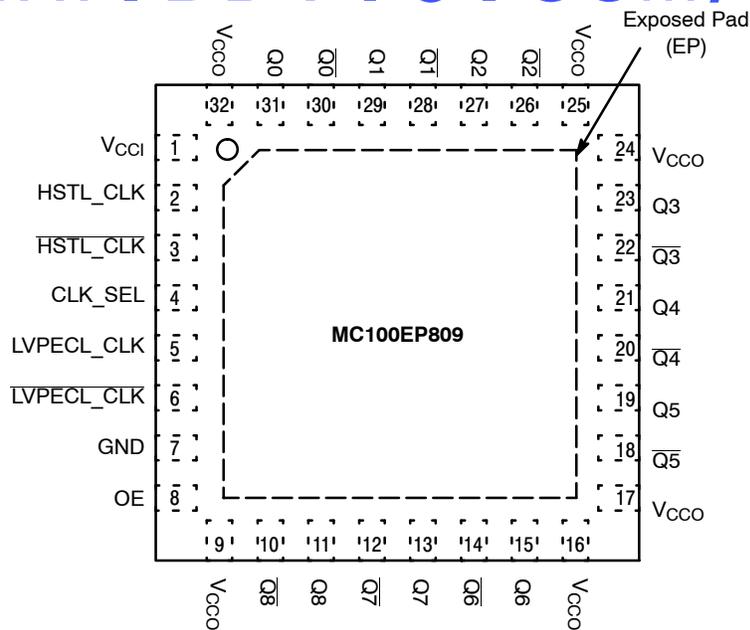


Figure 2. 32-Lead QFN Pinout (Top View)

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Table 1. PIN DESCRIPTION

PIN	FUNCTION
HSTL_CLK*, HSTL_CLK**	HSTL or LVDS Differential Inputs
LVPECL_CLK*, LVPECL_CLK**	LVPECL or LVDS Differential Inputs
CLK_SEL**	LVC MOS/LVTTL Input CLK Select
OE**	LVC MOS/LVTTL Output Enable
Q0 – Q8, Q0 – Q8	HSTL Differential Outputs
V _{CC1}	Positive Supply_Core (3.0 V – 3.6 V)
V _{CC0}	Positive Supply_HSTL Outputs (1.6 V – 2.0 V)
GND	Ground
EP	The exposed pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of the package. THE exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND.

* Pins will default LOW when left open.

** Pins will default HIGH when left open.

Table 2. TRUTH TABLE

OE*	CLK_SEL	Q0 – Q8	$\overline{Q0} - \overline{Q8}$
L	L	L	H
L	H	L	H
H	L	HSTL_CLK	HSTL_CLK
H	H	LVPECL_CLK	LVPECL_CLK

*The OE (Output Enable) signal is synchronized with the rising edge of the HSTL_CLK and LVOCL_CLK signals.

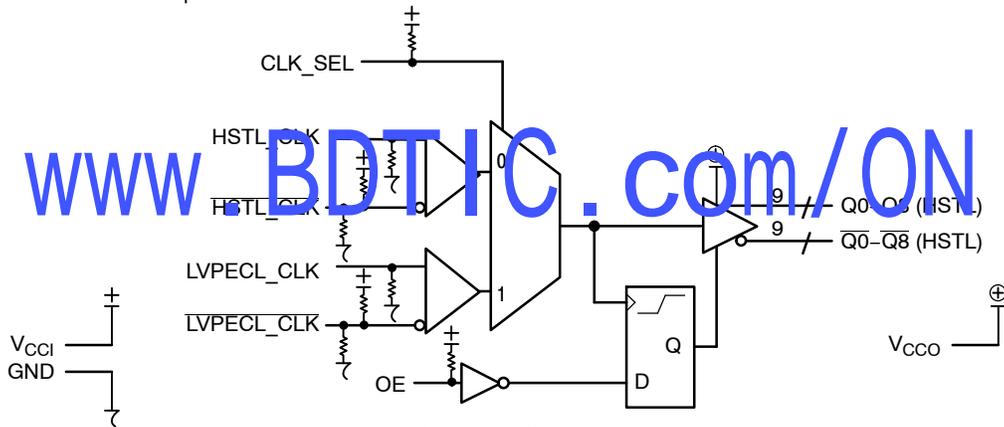


Figure 3. Logic Diagram

Table 3. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model	> 2 kV	
	Machine Model	> 200 V	
	Charged Device Model	> 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb-Free Pkg
		LQFP-32	Level 2
		QFN-32	N/A
Flammability Rating		Oxygen Index: 28 to 34	
		UL 94 V-0 @ 0.125 in	
Transistor Count		478 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC1}	Core Power Supply	GND = 0 V	V _{CC0} = 1.6 to 2.0 V	4	V
V _{CC0}	HSTL Output Power Supply	GND = 0 V	V _{CC1} = 3.0 to 3.6 V	4	V
V _I	Input Voltage	GND = 0 V	V _I ≤ V _{CC1}	4	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	LQFP-32 LQFP-32	80 55	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	LQFP-32	12 to 17	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	2S2P	QFN-32	12	°C/W
T _{sol}	Wave Solder	Pb Pb-Free		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. LVPECL DC CHARACTERISTICS V_{CC1} = 3.0 V to 3.6 V; V_{CC0} = 1.6 V to 2.0 V, GND = 0 V

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CC}	Core Power Supply Current	75	95	115	75	95	115	75	95	115	mA
V _{IH}	Input HIGH Voltage (Single-Ended)	V _{CC1} - 1.165		V _{CC1} - 0.88	V _{CC1} - 1.165		V _{CC1} - 0.88	V _{CC1} - 1.165		V _{CC1} - 0.88	V
V _{IL}	Input LOW Voltage (Single-Ended)	V _{CC1} - 1.945		V _{CC1} - 1.6	V _{CC1} - 1.945		V _{CC1} - 1.6	V _{CC1} - 1.945		V _{CC1} - 1.6	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) (Figure 5) LVPECL_CLK/LVPECL_CLK	1.2		V _{CC1}	1.2		V _{CC1}	1.2		V _{CC1}	V
I _{IH}	Input HIGH Current	-150		150	-150		150	-150		150	μA
I _{IL}	Input LOW Current	-150		150	-150		150	-150		150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. V_{IHCMR} max varies 1:1 with V_{CC1}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 6. LVTTTL/LVC MOS DC CHARACTERISTICS $V_{CCI} = 3.0\text{ V to }3.6\text{ V}$; $V_{CCO} = 1.6\text{ V to }2.0\text{ V}$, $GND = 0\text{ V}$

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V
I_{IH}	Input HIGH Current	-150		150	-150		150	-150		150	μA
I_{IL}	Input LOW Current	-300		300	-300		300	-300		300	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. HSTL DC CHARACTERISTICS $V_{CCI} = 3.0\text{ V to }3.6\text{ V}$; $V_{CCO} = 1.6\text{ V to }2.0\text{ V}$, $GND = 0\text{ V}$

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 3)	1.0		1.2	1.0		1.2	1.0		1.2	V
V_{OL}	Output LOW Voltage (Note 3)	0.1		0.4	0.1		0.4	0.1		0.4	V
V_{IH}	Input HIGH Voltage (Figure 6)	$V_X + 0.1$		1.6	$V_X + 0.1$		1.6	$V_X + 0.1$		1.6	V
V_{IL}	Input LOW Voltage (Figure 6)	-0.3		$V_X - 0.1$	-0.3		$V_X - 0.1$	-0.3		$V_X - 0.1$	V
V_X	HSTL Input Crossover Voltage	0.68	-	0.9	0.68	-	0.9	0.68	-	0.9	V
I_{IH}	Input HIGH Current	-150		150	-150		150	-150		150	μA
I_{IL}	Input LOW Current	-300		300	-300		300	-300		300	μA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) HSTL_CLK/IST_CLK	0.6		$V_{CCI} - 1.2$	0.6		$V_{CCI} - 1.2$	0.6		$V_{CCI} - 1.2$	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. All outputs loaded with 50 Ω to GND (Figure 7).

4. V_{IHCMR} max varies 1:1 with V_{CCI} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 8. AC CHARACTERISTICS $V_{CCI} = 3.0\text{ V to }3.6\text{ V}$; $V_{CCO} = 1.6\text{ V to }2.0\text{ V}$, $GND = 0\text{ V}$ (Note 5)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{Opp}	Differential Output Voltage $f_{out} < 100\text{ MHz}$ (Figure 4) $f_{out} < 500\text{ MHz}$ $f_{out} < 750\text{ MHz}$	600	850		600	850		600	850		mV mV
		600	750		600	750		600	750		
		450	575		450	575		450	575		
t_{PLH} t_{PHL}	Propagation Delay (Differential Configuration) LVPECL_CLK to Q HSTL_CLK to Q	680	800	930	700	820	950	780	920	1070	ps
		690	830	990	700	850	1000	790	950	1110	ps
t_{skew}	Within-Device Skew (Note 6) Device-to-Device Skew (Note 7)		15	50		15	50		15	50	ps
			100	200		100	200		100	200	ps
t_{JITTER}	Random Clock Jitter (Figure 4) (RMS)		1.4	3.0		1.4	3.0		1.4	3.0	ps
V_{PP}	Input Swing (Differential Configuration) (Note 8) (Figure 5) LVPECL HSTL	200			200			200			mV
		200			200			200			mV
t_S	OE Set Up Time (Note 9)	0.5			0.5			0.5			ns
t_H	OE Hold Time	0.5			0.5			0.5			ns
t_r/t_f	Output Rise/Fall Time (20% – 80%)	350		600	350	450	600	350		600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with 750 mV (LVPECL) source or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to GND (Figure 7).
6. Skew is measured between outputs under identical transitions and conditions on any one device.
7. Device-to-Device skew for identical transitions and conditions.
8. V_{PP} is the Differential Input Voltage swing required to maintain AC characteristics listed herein.
9. OE Set Up Time is defined with respect to the rising edge of the clock. OE High-to-Low transition ensures outputs remain disabled during the next clock cycle. OE Low-to-High transition enables normal operation of the next input clock (Figure 9).

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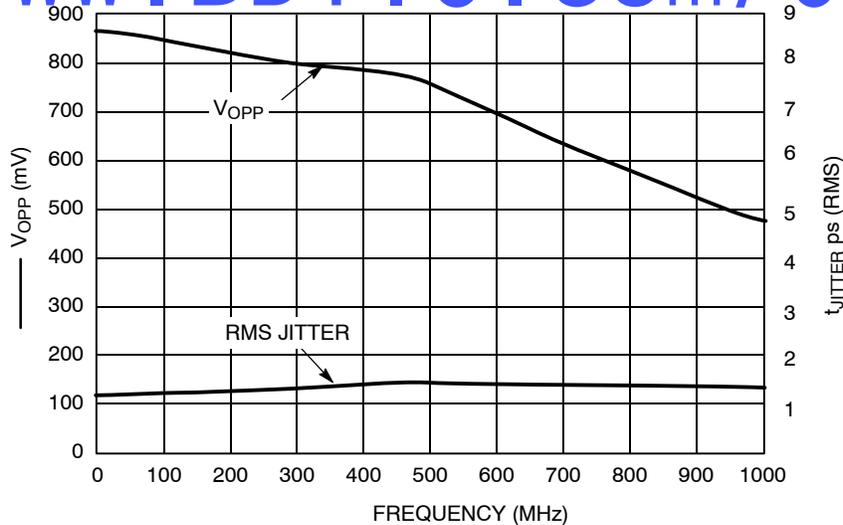


Figure 4. Output Frequency (F_{OUT}) versus Output Voltage (V_{OPP}) and Random Clock Jitter (t_{JITTER})

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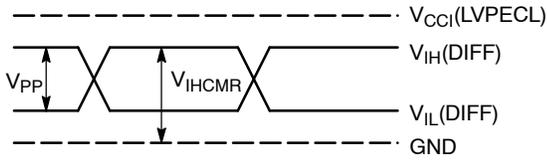


Figure 5. LVPECL Differential Input Levels

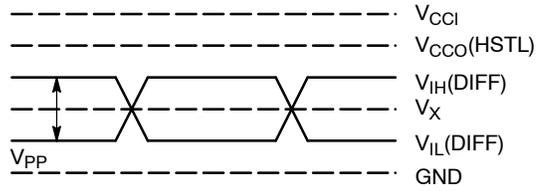


Figure 6. HSTL Differential Input Levels

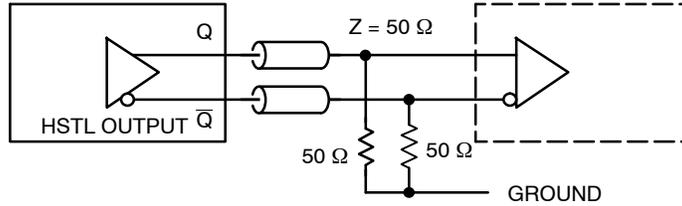
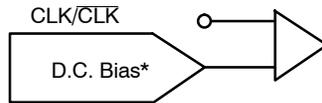


Figure 7. HSTL Output Termination and AC Test Reference



*Must be CLK/CLK common mode voltage: $(V_{IH} + V_{IL})/2$.

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Figure 8. Single-Ended CLK/CLK Input Configuration

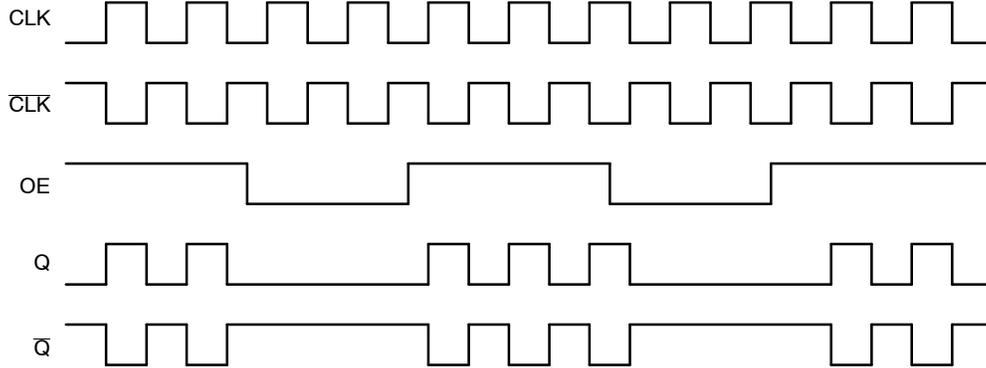


Figure 9. Output Enable (OE) Timing Diagram

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ORDERING INFORMATION

Device	Package	Shipping†
MC100EP809FA	LQFP-32	250 Units / Tray
MC100EP809FAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC100EP809FAR2	LQFP-32	2000 / Tape & Reel
MC100EP809FAR2G	LQFP-32 (Pb-Free)	2000 / Tape & Reel
MC100EP809MNG	QFN32 (Pb-Free)	74 Units / Rail
MC100EP809MNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

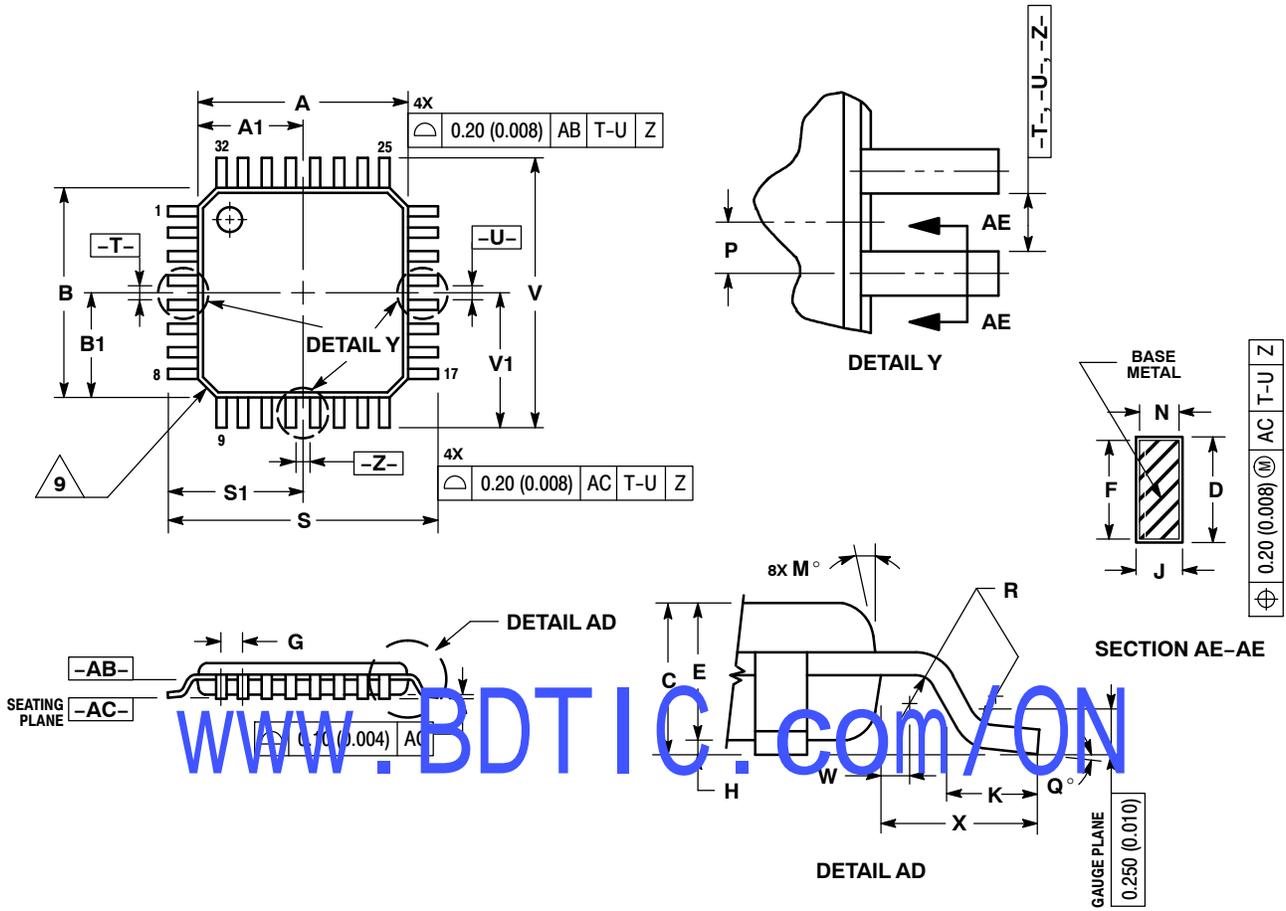
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AN18020/D** – Termination of ECL Logic Devices
- AN18016/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

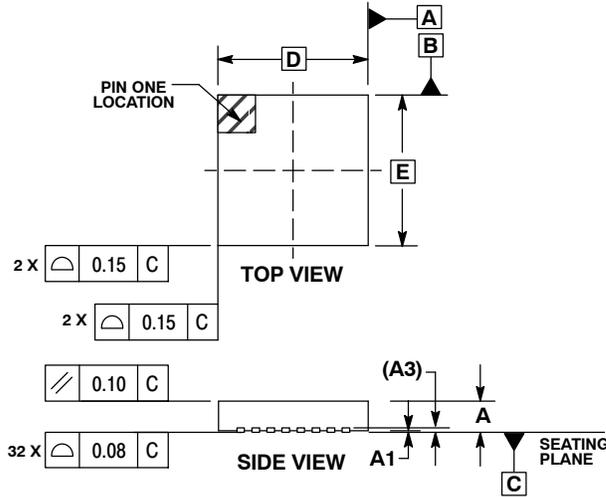
32 LEAD LQFP
CASE 873A-02
ISSUE C



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PACKAGE DIMENSIONS

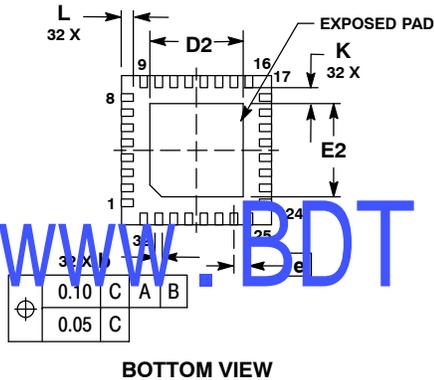
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CASE 488AM-01
ISSUE O



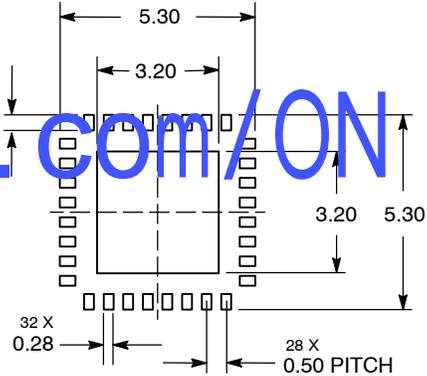
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	---	---
L	0.300	0.400	0.500



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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