

# MC100LVELT20

## Product Preview

# 3.3V LVTTTL/LVCMOS to Differential LVPECL Translator

### Description

The MC100LVELT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only + 3.3 V and ground are required. The small outline SOIC-8 package and the single gate of the MC100LVELT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

### Features

- 390 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 0.8 GHz Typical
- Operating Range  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$  with  $GND = 0\text{ V}$
- PNP TTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- Pb-Free Packages are Available



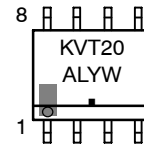
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### MARKING DIAGRAM



SO-8  
D SUFFIX  
CASE 751



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

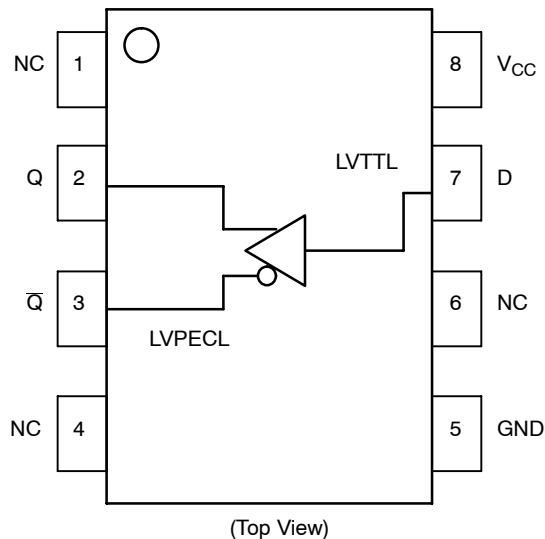
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**Table 1. PIN DESCRIPTION**

Pin	Function
Q, $\bar{Q}$	Differential PECL Outputs
D	LVTTTL Input
V <sub>CC</sub>	Positive Supply
GND	Ground
NC	No Connect

**Figure 1. 8-Lead Pinout and Logic Diagram**

**Table 2. ATTRIBUTES**

Characteristics		Value	
Internal Input Pulldown Resistor		N/A	
Internal Input Pullup Resistor		N/A	
ESD Protection		Human Body Model	> 1.5 kV
		Machine Model	> 200 V
		Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb-Free Pkg
		SOIC-8	Level 1
Flammability Rating		Oxygen Index: 28 to 34	
Transistor Count		150 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	GND = 0 V		6	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
I <sub>out</sub>	Output Current	Continuous		50	mA
		Surge		100	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm	SOIC-8	190	°C/W
		500 lfpm	SOIC-8	130	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
T <sub>sol</sub>	Wave Solder	Pb		265	°C
		Pb-Free		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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**Table 4. LVTTTL INPUT DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current ( $V_{in} = 2.7\text{ V}$ )			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH Current MAX ( $V_{in} = 6.0\text{ V}$ )			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current ( $V_{in} = 0.5\text{ V}$ )			-0.6	$\text{mA}$
$V_{IK}$	Input Clamp Voltage ( $I_{in} = -18\text{ mA}$ )			-1.2	$\text{V}$
$V_{IH}$	Input HIGH Voltage	2.0			$\text{V}$
$V_{IL}$	Input LOW Voltage			0.8	$\text{V}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 5. 100LVELT PECL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$  (Note 2)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{CC}$	Negative Power Supply Current	20	25	30	22	27	32	23	28	33	$\text{mA}$
$V_{OH}$	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	$\text{mV}$
$V_{OL}$	Output LOW Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	$\text{mV}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Output parameters vary 1:1 with  $V_{CC}$ .
3. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

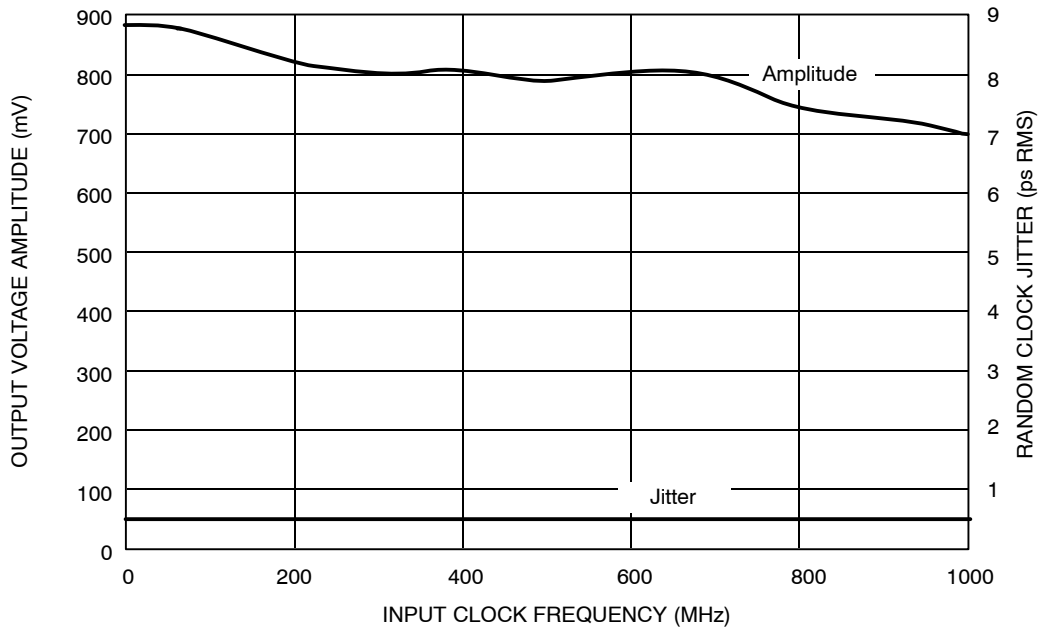
**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $GND = 0\text{ V}$  (Note 4)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Input Clock Frequency (Figure 2)	600	800		600	800		600	800		$\text{MHz}$
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	280	350	430	300	370	450	320	400	490	$\text{ps}$
$t_{SKEW}$	Device-to-Device Skew (Note 5)			250			250			250	$\text{ps}$
$t_{JITTER}$	Random Clock Jitter (RMS) (Figure 2)		< 1	< 2		< 1	< 2		< 1	< 2	$\text{ps}$
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) $Q, \bar{Q}$	70	100	225	80	120	225	90	140	225	$\text{ps}$

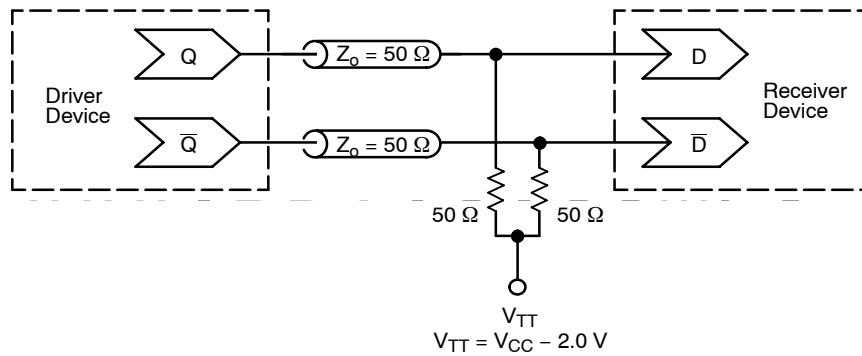
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Measured using a LVTTTL source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
5. Skew is measured between outputs under identical transitions.

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**Figure 2. Output Voltage Amplitude ( $V_{OUTpp}$ )/RMS Jitter vs. Input Clock Frequency at Ambient Temperature**



**Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100LVELT20D	SOIC-8	98 Units / Rail
MC100LVELT20DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100LVELT20DR2	SOIC-8	2500 / Tape & Reel
MC100LVELT20DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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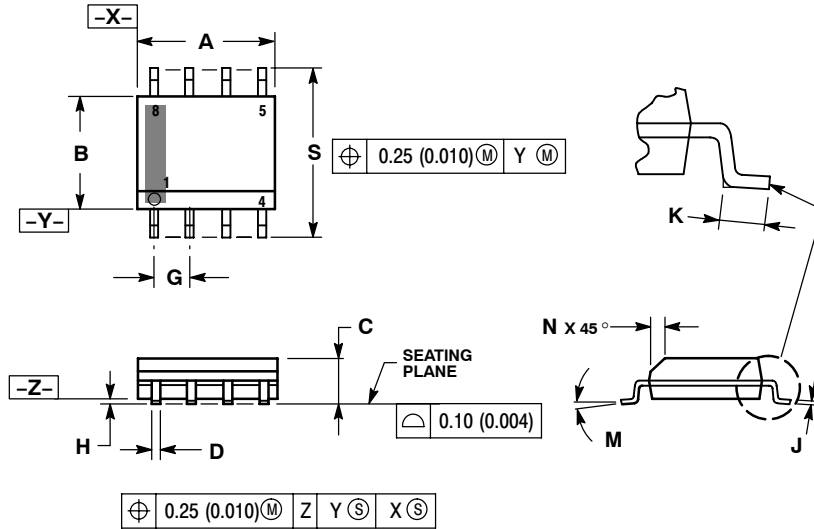
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LVELT20

## PACKAGE DIMENSIONS

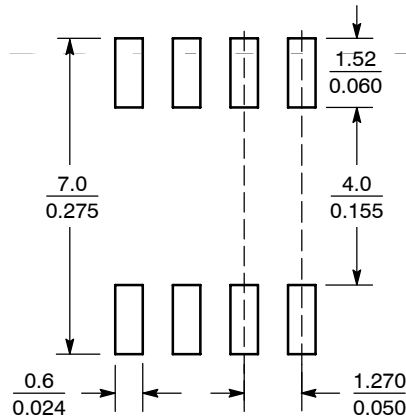
SOIC-8 NB  
CASE 751-07  
ISSUE AH



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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