MC14020B

14-Bit Binary Counter

The MC14020B 14−stage binary counter is constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−dividing circuits.

Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin−for−Pin Replacement for CD4020B
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

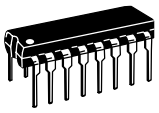
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

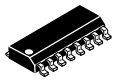
ON Semiconductor®

http://onsemi.com

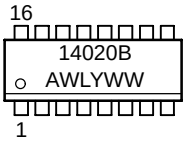
MARKING DIAGRAMS



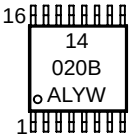
PDIP−16
P SUFFIX
CASE 648

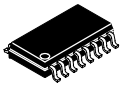


SOIC−16
D SUFFIX
CASE 751B

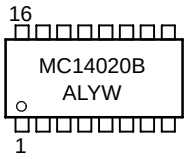


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



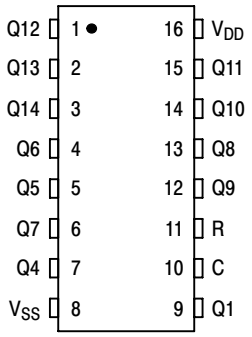
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Publication Order Number:
MC14020B/D

PIN ASSIGNMENT

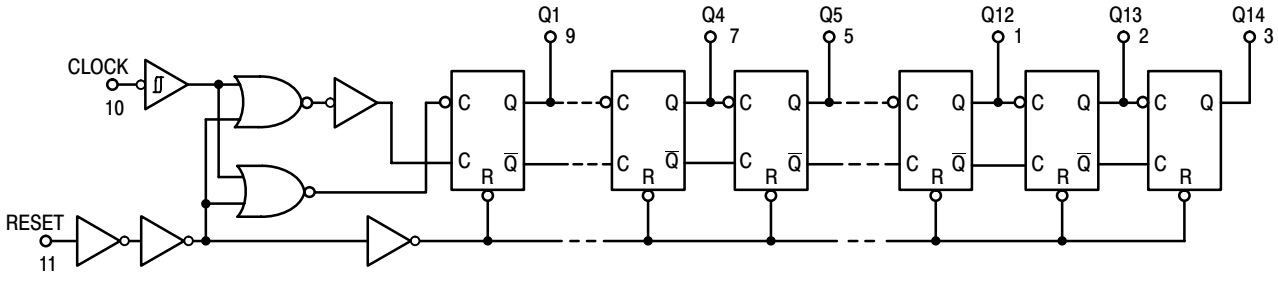


TRUTH TABLE

Clock	Reset	Output State
↗	0	No Change
↘	0	Advance to Next State
X	1	All Outputs are Low

X = Don't Care

LOGIC DIAGRAM



Q6 = PIN 4
Q7 = PIN 6
Q8 = PIN 13
Q9 = PIN 12
Q10 = PIN 14
Q11 = PIN 15
V_{DD} = PIN 16
V_{SS} = PIN 8

ORDERING INFORMATION

Device	Package	Shipping†
MC14020BCP	PDIP−16	500 Units / Rail
MC14020BCPG	PDIP−16 (Pb−Free)	500 Units / Rail
MC14020BD	SOIC−16	48 Units / Rail
MC14020BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14020BDR2	SOIC−16	2500 Units / Tape & Reel
MC14020BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14020BDT	TSSOP−16*	96 Units / Rail
MC14020BFEL	SOEIAJ−16	2000 Units / Tape & Reel
MC14020BFELG	SOEIAJ−16 (Pb−Free)	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	− − − −	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	− − − −	− 1.7 − 0.36 − 0.9 − 2.4	− − − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current	I_{in}	15	−	± 0.1	−	±0.00001	± 0.1	−	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.42 μA/kHz)f + I_{DD} I_T = (0.85 μA/kHz)f + I_{DD} I_T = (1.43 μA/kHz)f + I_{DD}							μAdc

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1	t_{PHL}					
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 175 ns		5.0	–	260	520	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 82 ns		10	–	115	230	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Clock to Q14						ns
t_{PHL}, t_{PLH} – (1.7 ns/pF) C_L + 1735 ns		5.0	–	1820	3900	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 772 ns		10	–	805	1725	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 535 ns		15	–	560	1200	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 285 ns		5.0	–	370	740	
t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Clock Pulse Width	t_{WH}	5.0	500	140	–	ns
		10	165	55	–	
		15	125	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.0	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Reset Pulse Width	t_{WL}	5.0	3000	320	–	ns
		10	550	120	–	
		15	420	80	–	
Reset Removal Time	t_{rem}	5.0	130	65	–	ns
		10	50	25	–	
		15	30	15	–	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

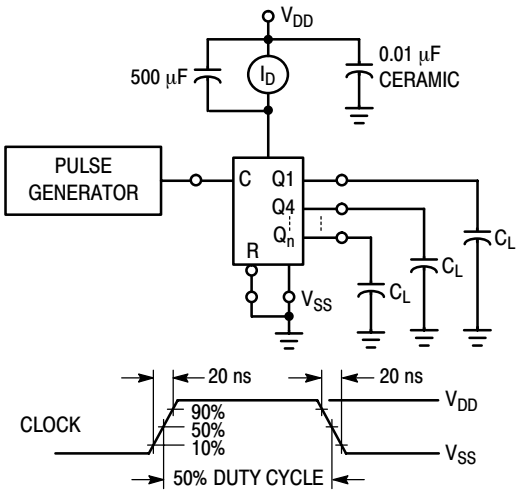


Figure 1. Power Dissipation Test Circuit and Waveform

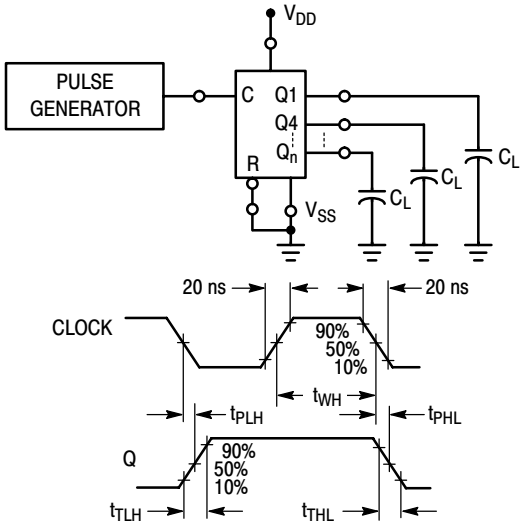


Figure 2. Switching Time Test Circuit and Waveforms

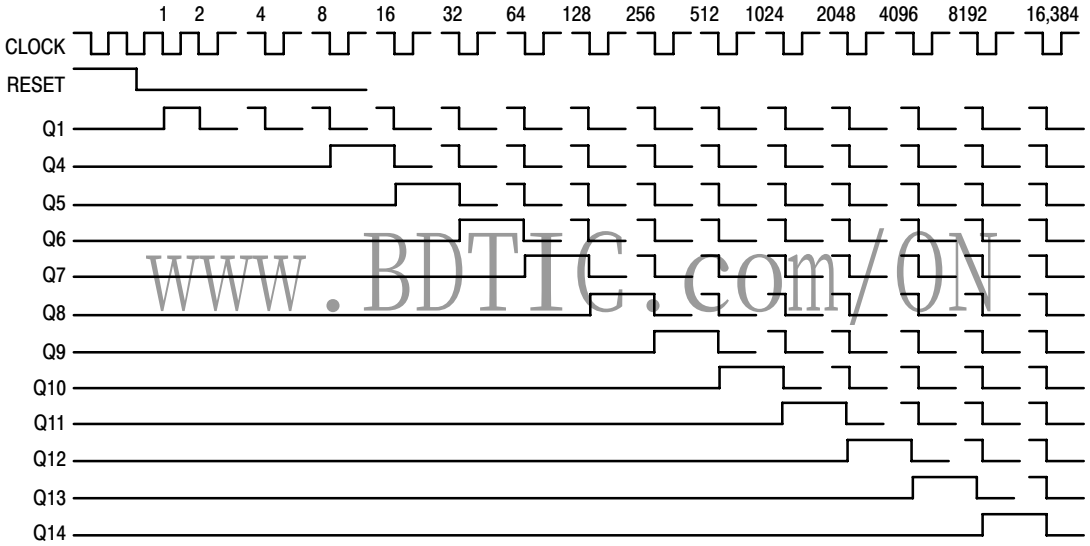
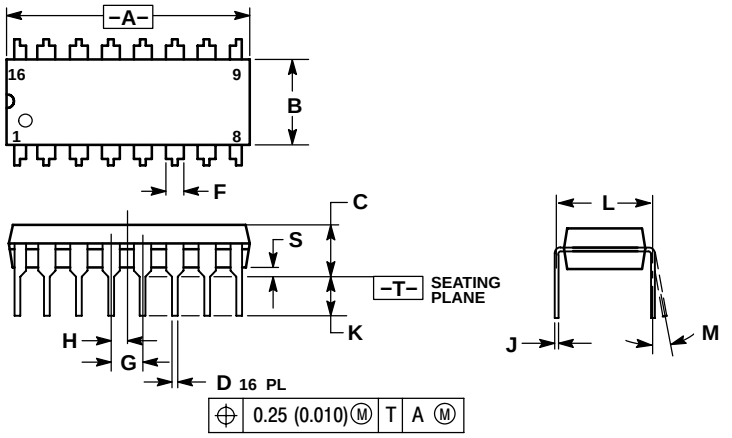


Figure 3. Timing Diagram

PACKAGE DIMENSIONS

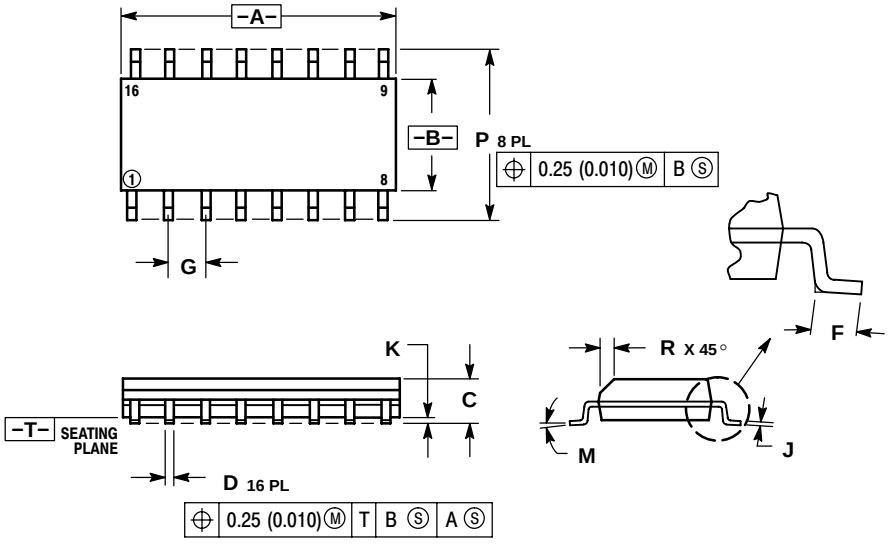
PDIP−16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B−05
ISSUE J

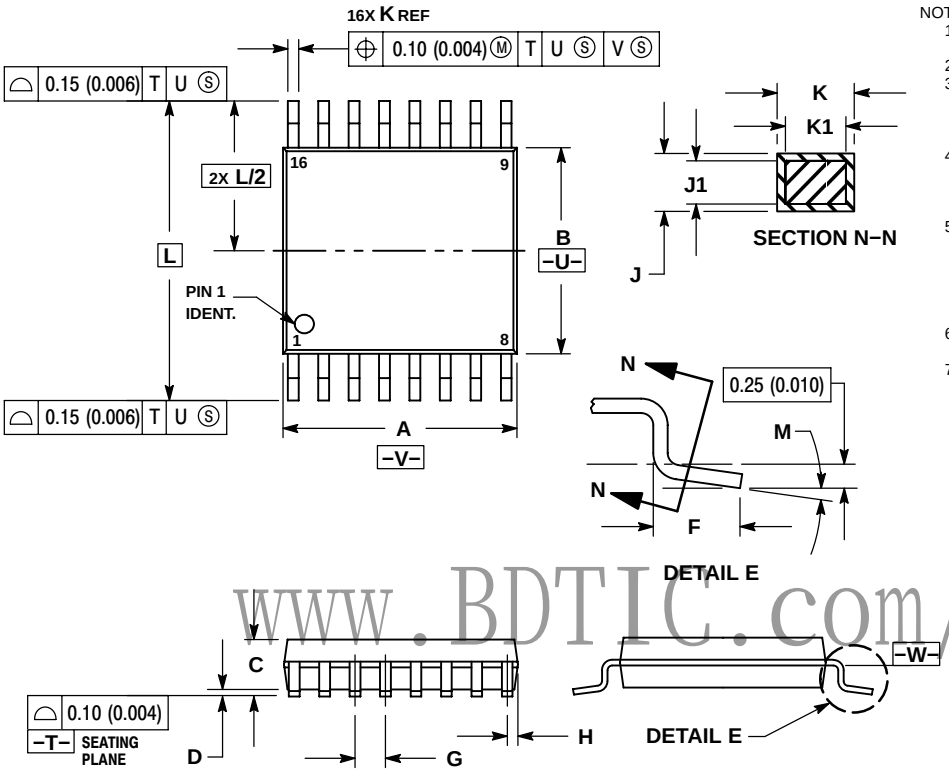


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP−16
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F−01
ISSUE A

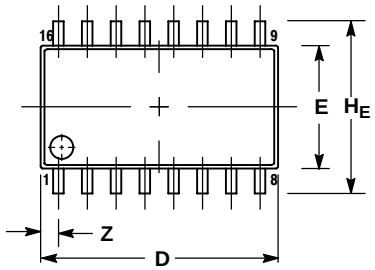


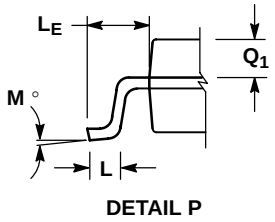
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

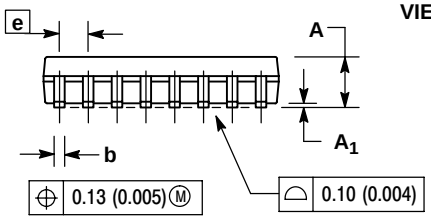
PACKAGE DIMENSIONS

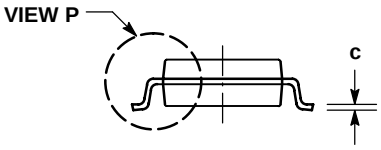
SOEIAJ−16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966−01
ISSUE O





DETAIL P





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.