

# MCR8SD, MCR8SM, MCR8SN

Preferred Device

## Sensitive Gate Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half-wave, silicon gate-controlled devices are needed.

### Features

- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- Blocking Voltage to 800 V
- On-State Current Rating of 8 A RMS at 80°C
- High Surge Current Capability – 80 A
- Rugged, Economical TO-220AB Package
- Glass Passivated Junctions for Reliability and Uniformity
- Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- Immunity to  $dv/dt$  – 5 V/ $\mu$ sec Minimum at 110°C
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ( $T_J = -40$ to $110^\circ\text{C}$ , Sine Wave, 50 to 60 Hz)	$V_{\text{DRM}}$ , $V_{\text{RRM}}$	400 600 800	V
On-State RMS Current ( $180^\circ$ Conduction Angles; $T_C = 80^\circ\text{C}$ )	$I_{\text{T(RMS)}}$	8.0	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 110^\circ\text{C}$ )	$I_{\text{TSM}}$	80	A
Circuit Fusing Consideration ( $t = 8.33$ ms)	$I^2t$	26.5	$\text{A}^2\text{sec}$
Forward Peak Gate Power (Pulse Width $\leq 10$ $\mu\text{s}$ , $T_C = 80^\circ\text{C}$ )	$P_{\text{GM}}$	5.0	W
Forward Average Gate Power ( $t = 8.3$ ms, $T_C = 80^\circ\text{C}$ )	$P_{\text{G(AV)}}$	0.5	W
Forward Peak Gate Current (Pulse Width $\leq 10$ $\mu\text{s}$ , $T_C = 80^\circ\text{C}$ )	$I_{\text{GM}}$	2.0	A
Operating Junction Temperature Range	$T_J$	-40 to 110	$^\circ\text{C}$
Storage Temperature Range	$T_{\text{stg}}$	-40 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $V_{\text{DRM}}$  and  $V_{\text{RRM}}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

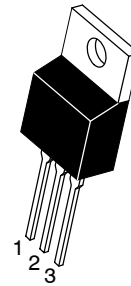
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



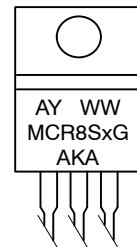
ON Semiconductor®

<http://onsemi.com>

SCRs  
8 AMPERES RMS  
400 thru 800 VOLTS



### MARKING DIAGRAM



TO-220AB  
CASE 221A-09  
STYLE 3

- A = Assembly Location
- Y = Year
- WW = Work Week
- x = D, M, or N
- G = Pb-Free Package
- AKA = Diode Polarity

### PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

### ORDERING INFORMATION

Device	Package	Shipping
MCR8SD	TO-220AB	50 Units / Rail
MCR8SDG	TO-220AB (Pb-Free)	50 Units / Rail
MCR8SM	TO-220AB	50 Units / Rail
MCR8SMG	TO-220AB (Pb-Free)	50 Units / Rail
MCR8SN	TO-220AB	50 Units / Rail
MCR8SNG	TO-220AB (Pb-Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

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## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	$T_L$	260	$^{\circ}\text{C}$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current (Note 3) ( $V_D = \text{Rated } V_{DRM}$ and $V_{RRM}$ ; $R_{GK} = 1 \text{ k}\Omega$ )	$I_{DRM}$ , $I_{RRM}$	-	-	10 500	$\mu\text{A}$
					$T_J = 25^{\circ}\text{C}$ $T_J = 110^{\circ}\text{C}$

### ON CHARACTERISTICS

Peak Forward On-State Voltage (Note 2) ( $I_{TM} = 16 \text{ A}$ )	$V_{TM}$	-	-	1.8	V
Gate Trigger Current (Continuous dc) (Note 4) ( $V_D = 12 \text{ V}$ ; $R_L = 100 \Omega$ )	$I_{GT}$	5.0	25	200	$\mu\text{A}$
Holding Current (Note 3) ( $V_D = 12 \text{ V}$ , Gate Open, Initiating Current = 200 mA)	$I_H$	-	0.5	6.0	mA
Latch Current (Note 4) ( $V_D = 12 \text{ V}$ , $I_G = 200 \mu\text{A}$ )	$I_L$	-	0.6	8.0	mA
Gate Trigger Voltage (Continuous dc) (Note 4) ( $V_D = 12 \text{ V}$ ; $R_L = 100 \Omega$ )	$V_{GT}$	0.3	0.65	1.0 1.5	V
Gate Non-Trigger Voltage ( $V_D = 12 \text{ V}$ , $R_L = 100 \Omega$ )	$V_{GD}$	0.2	-	-	V
					$T_J = 25^{\circ}\text{C}$ $T_J = -40^{\circ}\text{C}$ $T_J = 110^{\circ}\text{C}$

### DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ( $V_D = 67\% V_{DRM}$ , $R_{GK} = 1 \text{ K}\Omega$ , $C_{GK} = 0.1 \mu\text{F}$ , $T_J = 110^{\circ}\text{C}$ )	$dv/dt$	5.0	15	-	$\text{V}/\mu\text{s}$
Critical Rate of Rise of On-State Current $IPK = 50 \text{ A}$ , $Pw = 40 \mu\text{sec}$ , $diG/dt = 1 \text{ A}/\mu\text{sec}$ , $I_{gt} = 10 \text{ mA}$	$di/dt$	-	-	100	$\text{A}/\mu\text{s}$

2. Indicates Pulse Test: Pulse Width  $\leq 2.0 \text{ ms}$ , Duty Cycle  $\leq 2\%$ .

3.  $R_{GK} = 1000 \text{ Ohms}$  included in measurement.

4. Does not include  $R_{GK}$  in measurement.

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## Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
$I_H$	Holding Current

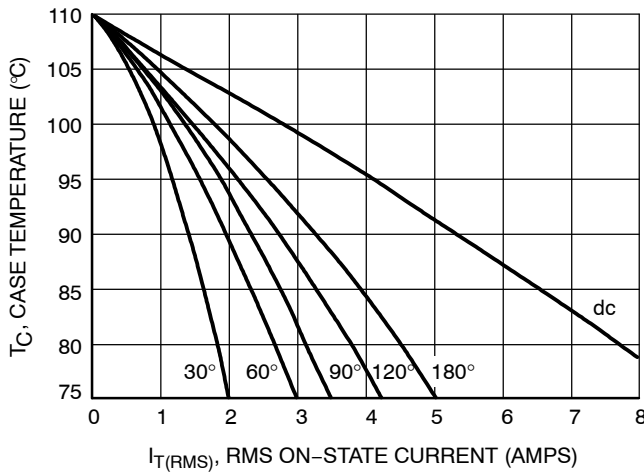
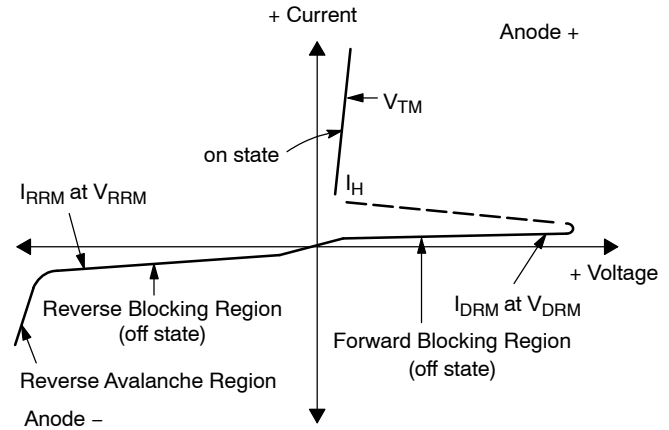


Figure 1. Typical RMS Current Derating

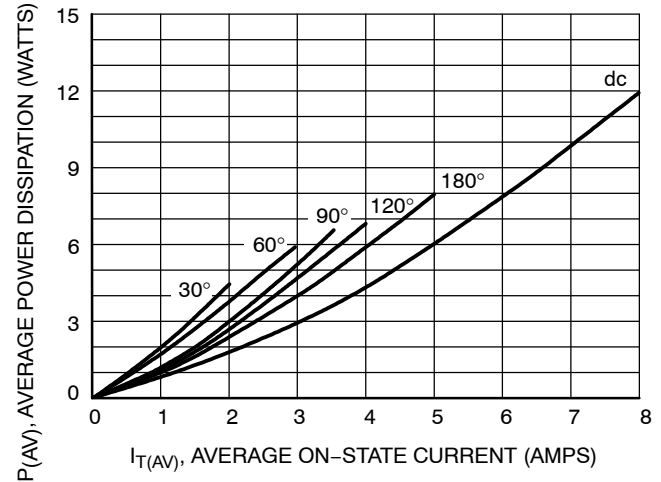


Figure 2. On-State Power Dissipation

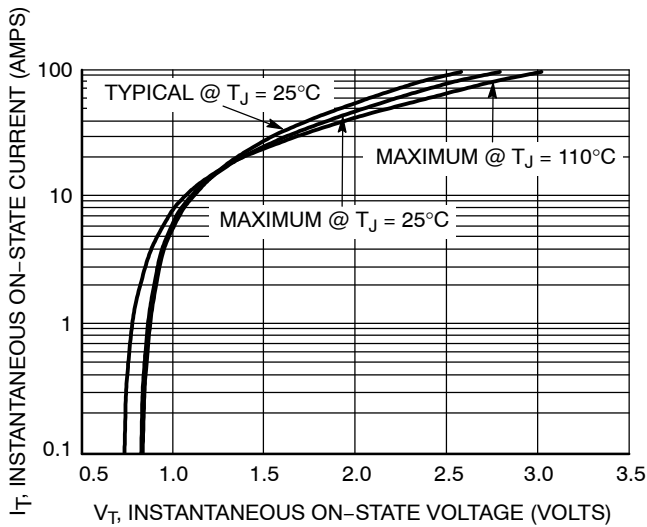


Figure 3. Typical On-State Characteristics

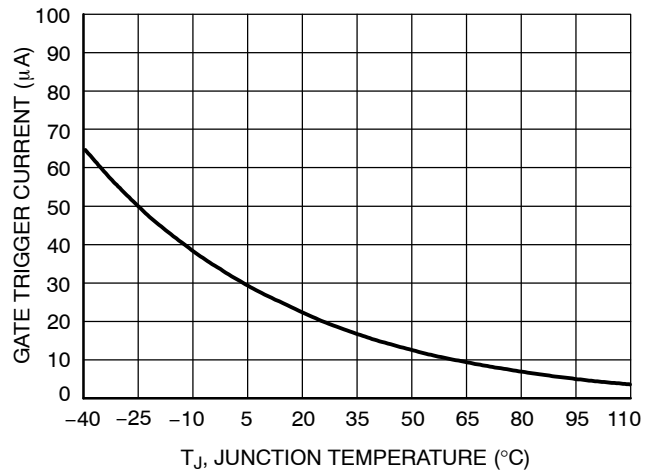


Figure 4. Typical Gate Trigger Current versus Junction Temperature

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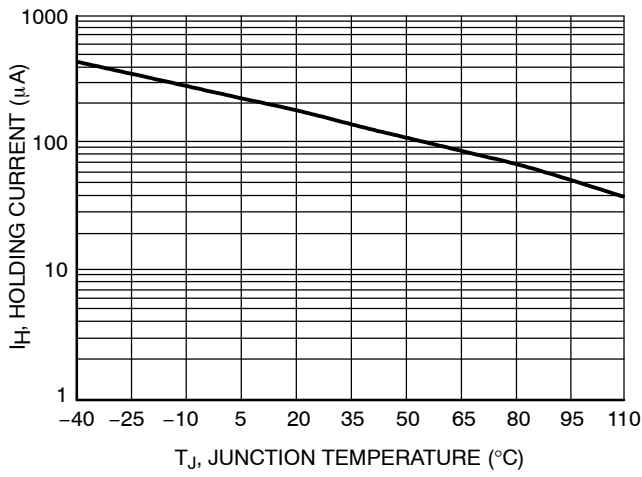


Figure 5. Typical Holding Current versus Junction Temperature

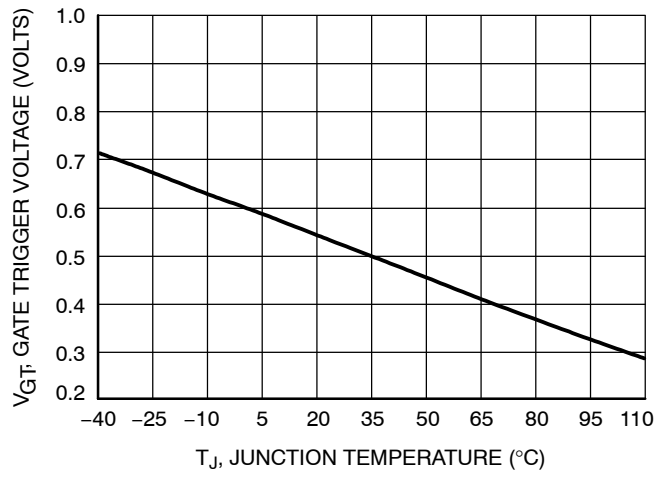


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

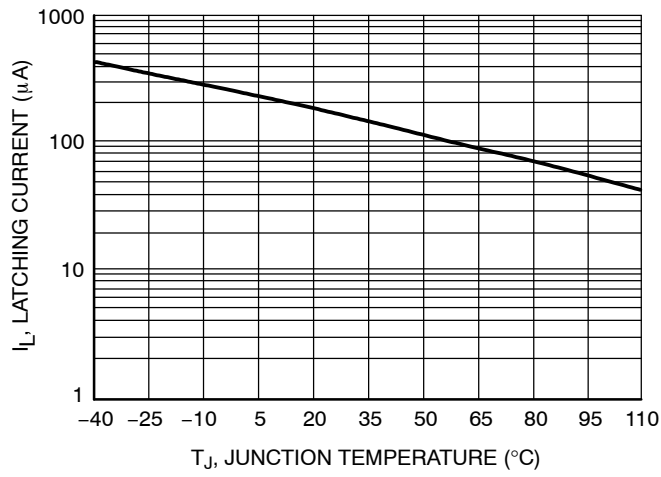
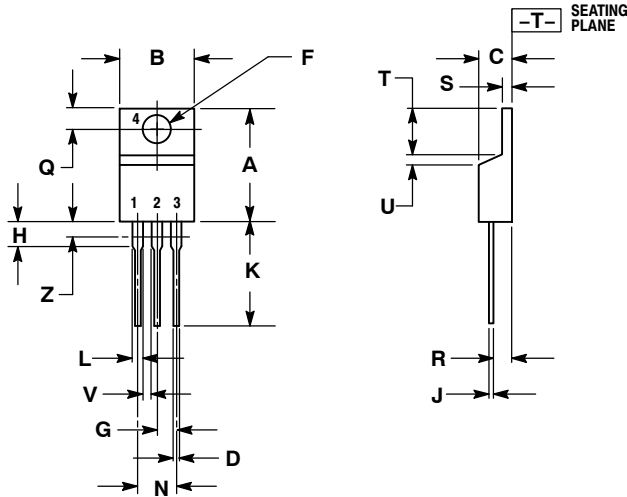


Figure 7. Typical Latching Current versus Junction Temperature

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## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AF



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:

1. CATHODE
2. ANODE
3. GATE
4. ANODE

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