

# MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

## Complementary Silicon Plastic Power Transistor

### DPAK-3 for Surface Mount Applications

Designed for low voltage, low-power, high-gain audio amplifier applications.

#### Features

- Collector-Emitter Sustaining Voltage –  
 $V_{CE(sus)} = 100 \text{ Vdc (Min) @ } I_C$   
 $= 10 \text{ mAdc}$
- High DC Current Gain –  
 $h_{FE} = 40 \text{ (Min) @ } I_C$   
 $= 200 \text{ mAdc}$   
 $= 15 \text{ (Min) @ } I_C = 1.0 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Low Collector-Emitter Saturation Voltage –  
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C$   
 $= 500 \text{ mAdc}$   
 $= 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- High Current-Gain – Bandwidth Product –  
 $f_T = 40 \text{ MHz (Min) @ } I_C$   
 $= 100 \text{ mAdc}$
- Annular Construction for Low Leakage –  
 $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings:
  - ♦ Human Body Model, 3B > 8000 V
  - ♦ Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Packages\*



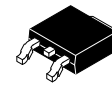
ON Semiconductor®

<http://onsemi.com>

4.0 A, 100 V, 12.5 W  
POWER TRANSISTOR

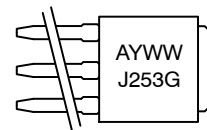


IPAK  
CASE 369D  
STYLE 1

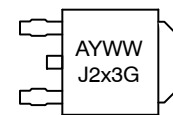


DPAK-3  
CASE 369C  
STYLE 1

#### MARKING DIAGRAMS



IPAK



DPAK

A = Assembly Location  
Y = Year  
WW = Work Week  
x = 4 or 5  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	$V_{CB}$	100	Vdc
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	7.0	Vdc
Collector Current Continuous Peak	$I_C$	4.0 8.0	Adc
Base Current	$I_B$	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	12.5 0.1	W W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2) Derate above $25^\circ\text{C}$	$P_D$	1.4 0.011	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted on minimum pad sizes recommended.

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction–to–Case Junction–to–Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	$^\circ\text{C}/\text{W}$

2. When surface mounted on minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 3) ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ , $T_J = 125^\circ\text{C}$ )	$I_{CBO}$	– –	100 100	nAdc $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	100	nAdc
DC Current Gain (Note 3) ( $I_C = 200\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$h_{FE}$	40 15	180 –	–
Collector–Emitter Saturation Voltage (Note 3) ( $I_C = 500\text{ mAdc}$ , $I_B = 50\text{ mAdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $I_B = 100\text{ mAdc}$ )	$V_{CE(sat)}$	– –	0.3 0.6	Vdc
Base–Emitter Saturation Voltage (Note 3) ( $I_C = 2.0\text{ Adc}$ , $I_B = 200\text{ mAdc}$ )	$V_{BE(sat)}$	–	1.8	Vdc
Base–Emitter On Voltage (Note 3) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 1.0\text{ Vdc}$ )	$V_{BE(on)}$	–	1.5	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 4) ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 10\text{ MHz}$ )	$f_T$	40	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	$C_{ob}$	–	50	pF

3. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\approx 2\%$ .

4.  $f_T = |h_{FE}| \cdot f_{test}$

# MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

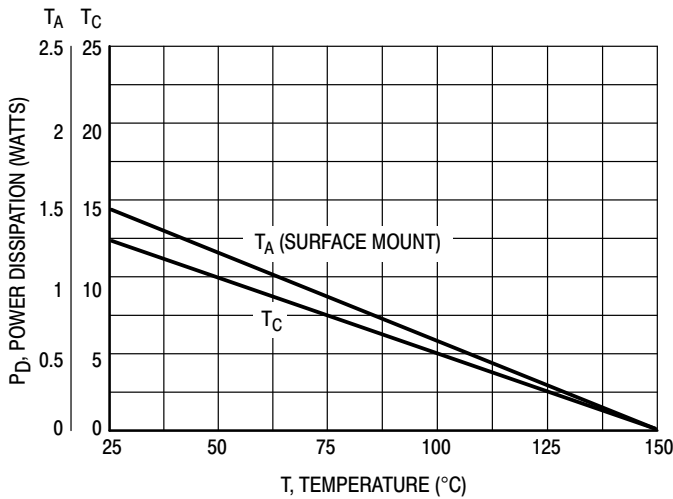


Figure 1. Power Derating

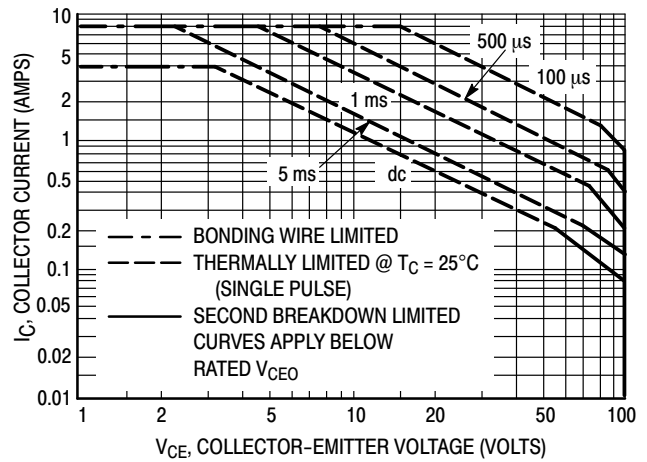


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

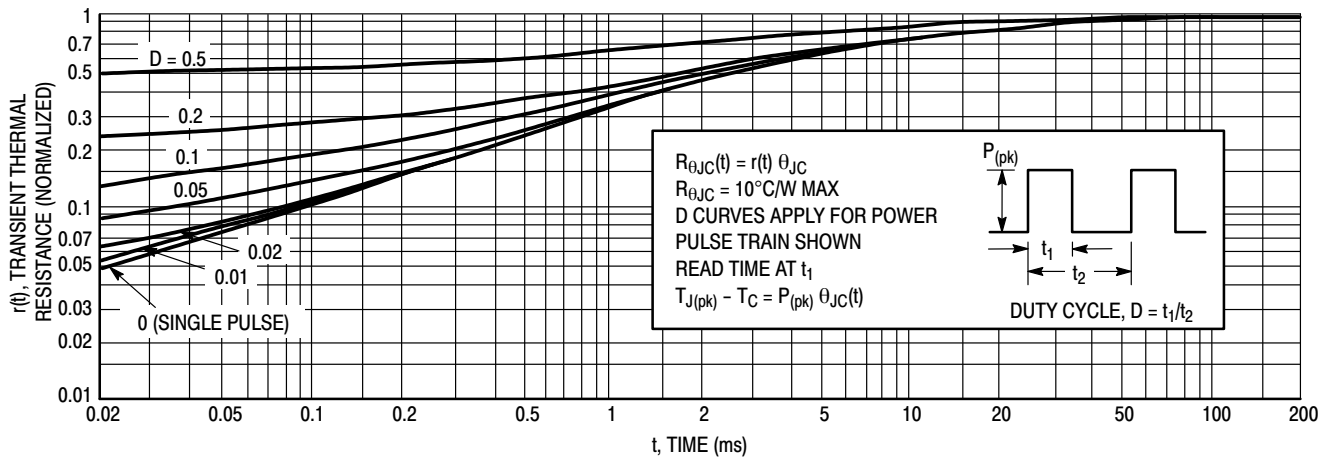
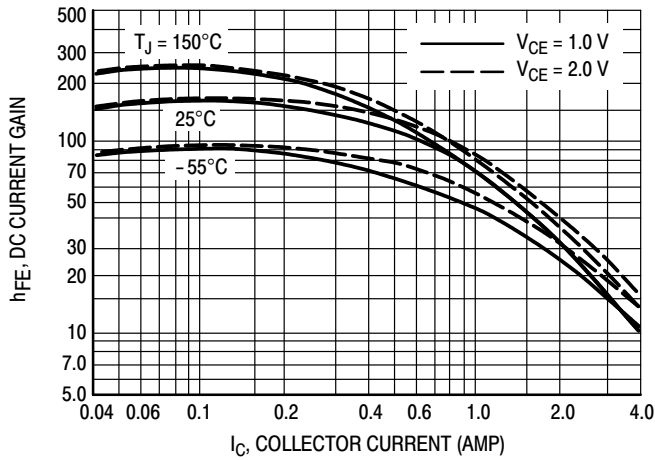


Figure 3. Thermal Response

MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

NPN  
MJD243



PNP  
MJD253

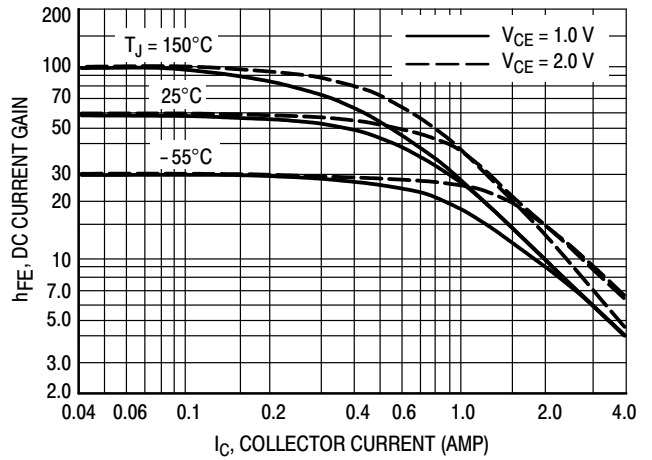


Figure 4. DC Current Gain

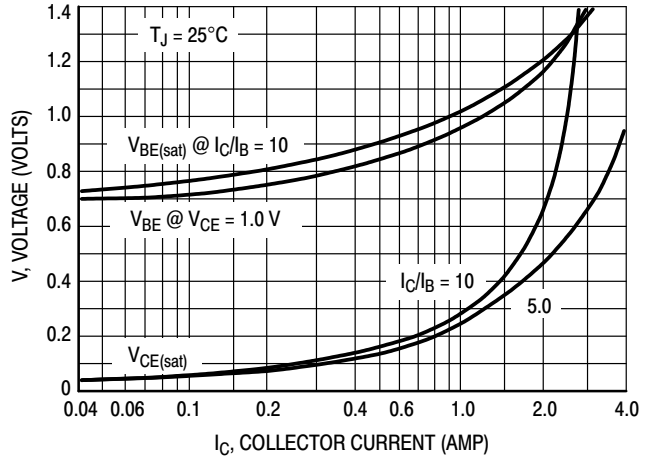
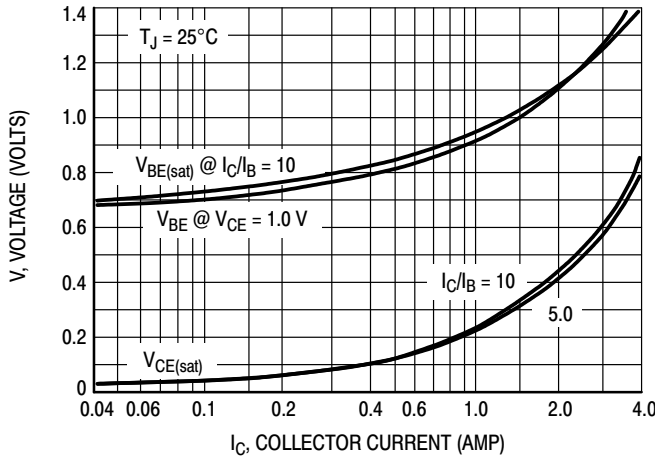


Figure 5. "On" Voltages

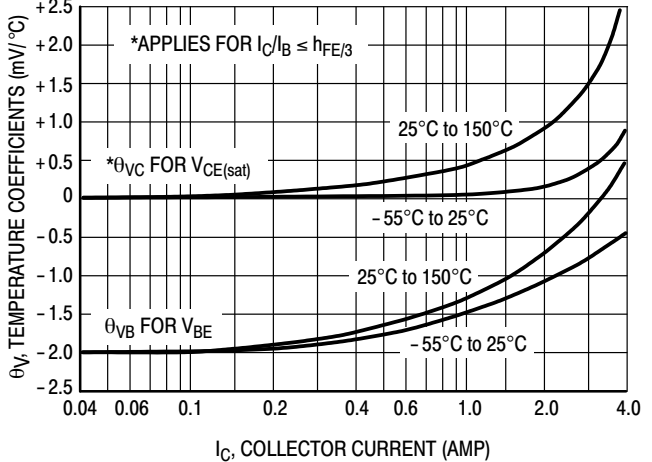
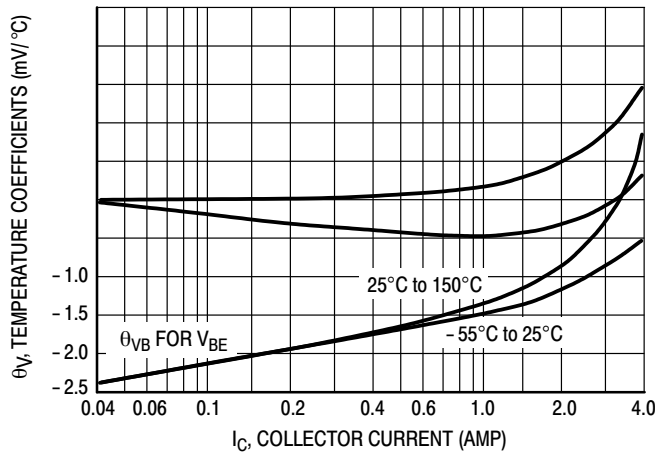


Figure 6. Temperature Coefficients

# MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

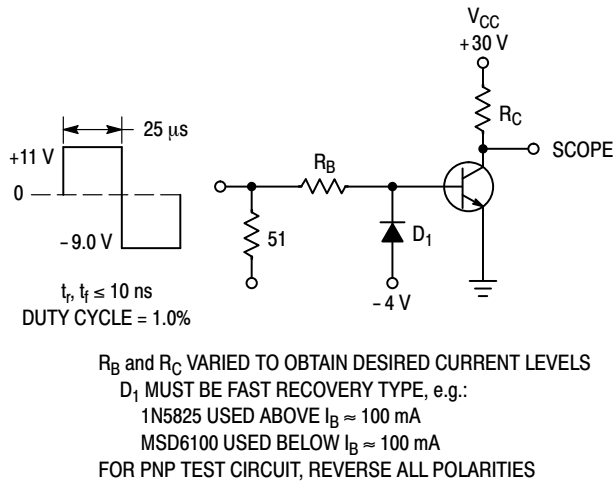


Figure 7. Switching Time Test Circuit

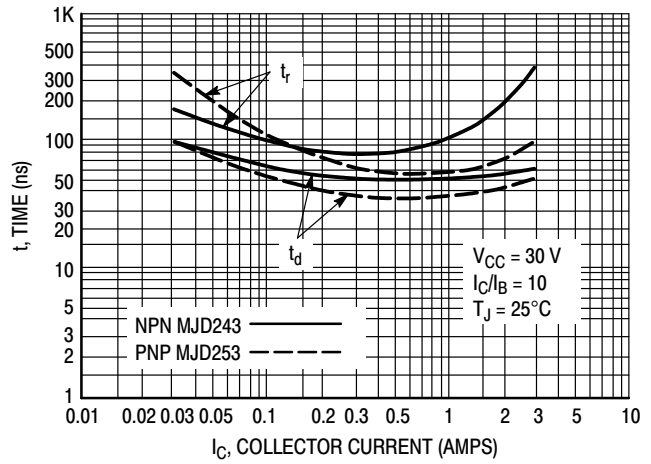


Figure 8. Turn-On Time

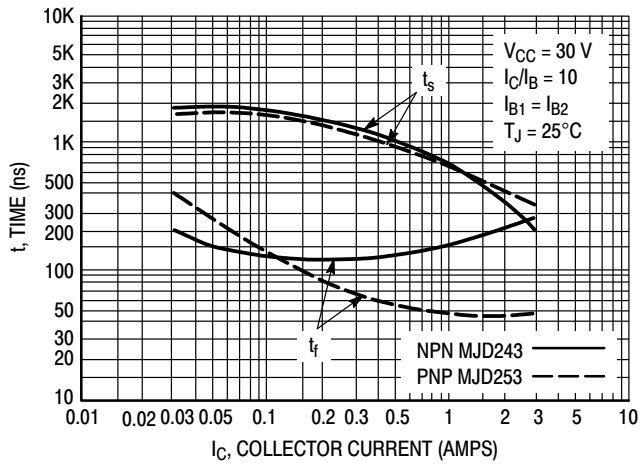


Figure 9. Turn-Off Time

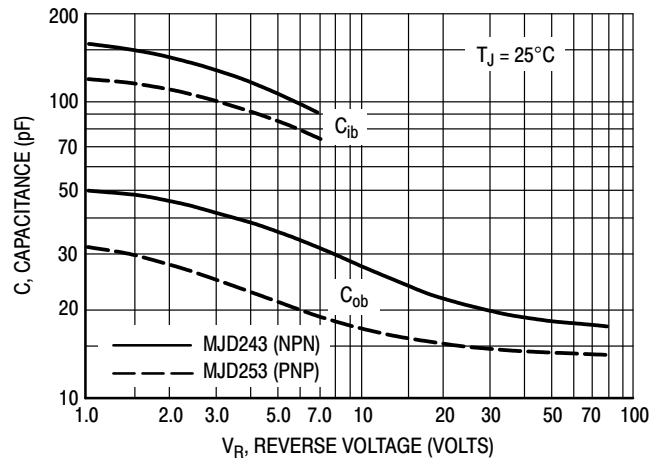


Figure 10. Capacitance

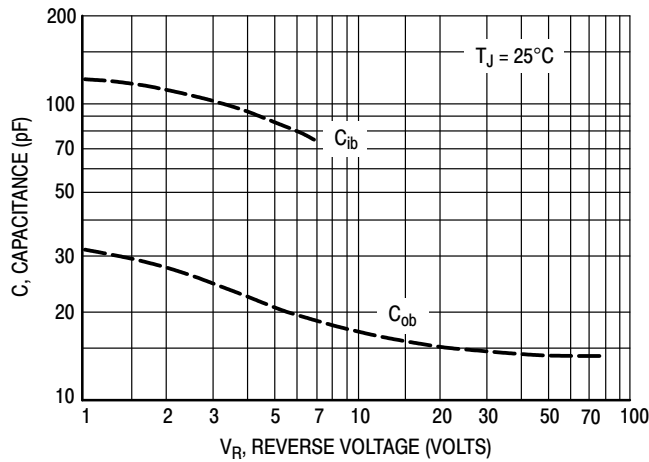


Figure 11. Capacitance

## MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

### ORDERING INFORMATION

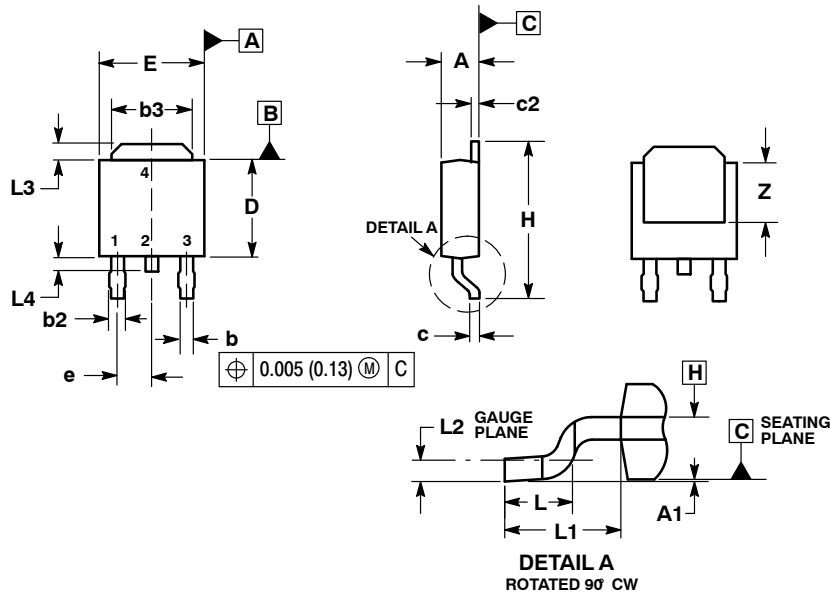
Device	Package Type	Package	Shipping <sup>†</sup>
MJD243G	DPAK-3 (Pb-Free)	369C	75 Units / Rail
MJD243T4G	DPAK-3 (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD243T4G	DPAK-3 (Pb-Free)	369C	2,500 / Tape & Reel
MJD253-1G	IPAK (Pb-Free)	369D	75 Units / Rail
MJD253T4G	DPAK-3 (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD253T4G	DPAK-3 (Pb-Free)	369C	2,500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

## PACKAGE DIMENSIONS

DPAK-3  
CASE 369C-01  
ISSUE D

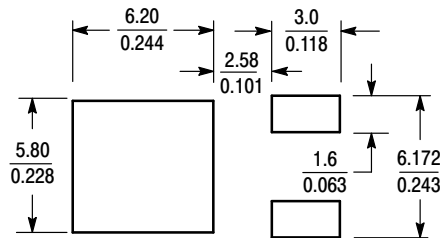


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

STYLE 1:

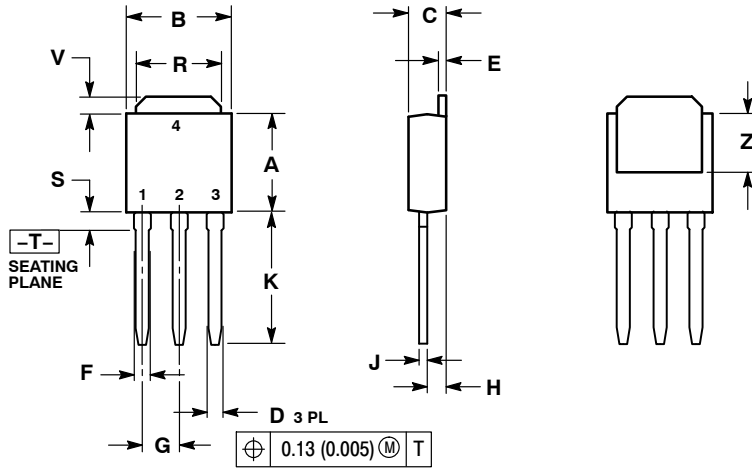
- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJD243, NJVMJD243T4G (NPN), MJD253, NJVMJD253T4G (PNP)

## PACKAGE DIMENSIONS

IPAK  
CASE 369D-01  
ISSUE C



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

[www.BDTIC.com/ON/](http://www.BDTIC.com/ON/)

MJD243/D