NB7V52M

Product Preview

1.8V / 2.5V Differential Data/Clock D Flip-Flop w/ Reset and CML Outputs

Multi-Level Inputs w/ Internal Termination

Description

The NB7V52M is a 10GHz differential Data and Clock D flip-flop with a Differential asynchronous Reset. The differential D/Db, CLK/CLKb and R/Rb inputs incorporate internal 50-Ω termination resistors and will accept LVPECL, CML, LVDS logic levels (see Figure 11).

When Clock transitions from Low to High, Data will be transferred to the differential CML outputs. The differential Clock inputs allow the NB7V52M to also be used as a negative edge triggered device.

The 16mA differential CML outputs provide matching internal 50-Ω terminations and 400 mV output swings when externally terminated with a 50-Ω resistor to VCC (see Figure 13).

The NB7V52M is offered in a low profile 3mm x 3mm 16-pin QFN package.

The NB7V52M is a member of the GigaComm™ family of high performance clock products. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency > 10GHz Typical
- Random Clock Jitter < 0.8ps RMS
- ___ ps Typical Propagation Delay
- 30ps Typical Rise and Fall Times
- Differential CML Outputs, 400mV peak-to-peak, typical
- Operating Range: V_{CC} = 1.71V to 2.625V with V_{EE} = 0V
- Internal 50-Ω Input Termination Resistors
- QFN-16 Package, 3mm x 3mm, Pb-free
- -40ºC to +85ºC Ambient Operating Temperature

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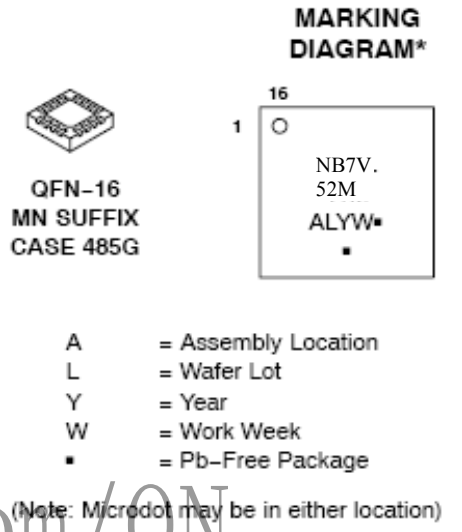


*For additional marking information, refer to Application Note AND8002/D.

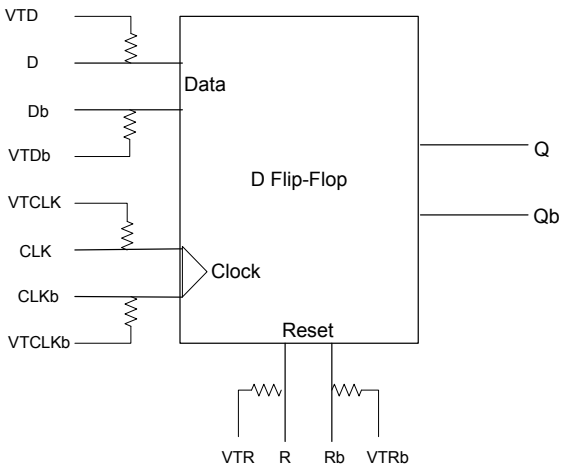


Figure 1.Functional Block Diagram

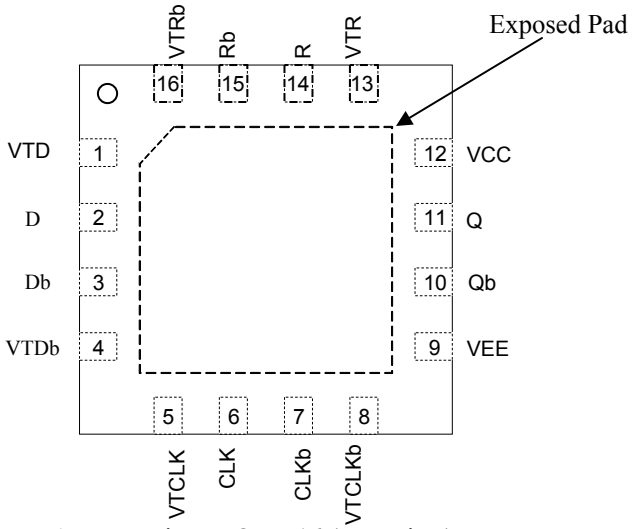


Figure 2. Pinout: QFN-16 (Top View)

Table 1. Truth Table

R	D	CLK	Q
H	x	x	L
L	L	Z	L
L	H	Z	H

Z = LOW to HIGH Transition
x = Don't care

Table 1. Pin Description

Pin	Name	I/O	Description
1	VTD	-	Internal 50-Ω Termination Pin for D
2	D	LVPECL, CML, LVDS Input	Noninverted Differential Data Input. Note 1
3	Db	LVPECL, CML, LVDS Input	Inverted Differential Data Input. Note 1
4	VTDb	-	Internal 50-Ω Termination Pin for Db
5	VTCLK	-	Internal 50-Ω Termination Pin for CLK
6	CLK	LVPECL, CML, LVDS Input	Noninverted Differential Clock Input. Note 1
7	CLKb	LVPECL, CML, LVDS Input	Inverted Differential Clock Input. Note 1
8	VTCLKb	-	Internal 50-Ω Termination Pin for CLKb
9	VEE	-	Negative Supply Voltage. Note 2.
10	Qb	CML Output	Inverted Differential Output
11	Q	CML Output	Noninverted Differential Output
12	VCC	-	Positive Supply Voltage. Note 2.
13	VTR	-	Internal 50-Ω Termination Pin for R
14	R	LVPECL, CML, LVDS Input	Noninverted Differential Reset Input. Note 1
15	Rb	LVPECL, CML, LVDS Input	Inverted Differential Reset Input. Note 1
16	VTRb	-	Internal 50-Ω Termination Pin for Rb
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to VEE on the PC board.

*

1. In the differential configuration, when the input termination pins (VTD, VTDb, VTR, VTRb, VTCLK, VTCLKb) are connected to a common termination voltage or left open, and if no signal is applied on D/Db,CLK/CLKb,R/Rb inputs, then the device will be susceptible to self-oscillation. Q/Qb outputs each have internal 50-ohm source termination resistor.
2. VCC and VEE pins must be externally connected to a power supply for proper operation.

Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity (Note 3)	16-QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		173
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.0	V
V_{IO}	Positive Input/Output Voltage	V_{EE} = 0 V	$-0.5 \le V_{Io} \le V_{CC}+0.5$	-0.5 to V_{CC} +0.5	V
V_{INPP}	Differential Input Voltage |CLK - CLKb|			1.89	V
I_{out}	Output Current	Continuous Surge		34 40	mA mA
I_{IN}	Input Current Through R_T (50-Ω Resistor)			+/-40	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 LFPM 500 LFPM	QFN-16 QFN-16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case) (Note 4)		QFN-16	4	°C/W
T_{sol}	Wave Solder			265	°C

. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS POSITIVE CML OUTPUT V_{CC} = 1.71 V to 2.625 V; V_{EE} = 0 V; TA = -40°C to 85°C (Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
Power Supply Current						
I_{CC}	Power Supply Current (Inputs and Outputs Open)	VCC = 2.5V		90	110	mA
		VCC = 1.8V		70	90	
CML Outputs						
V_{OH}	Output HIGH Voltage (Note 6)		V_{CC} – 40	V_{CC} – 20	V_{CC}	mV
		VCC = 2.5V	2460	2480	2500	
		VCC = 1.8V	1760	1780	1800	
V_{OL}	Output LOW Voltage (Note 6)	VCC = 2.5V	V_{CC} –600	V_{CC} – 500	V_{CC} – 400	mV
		VCC = 2.5V	1900	2000	2100	
		VCC = 1.8V	V_{CC} –550	V_{CC} – 450	V_{CC} – 350	mV
		VCC = 1.8V	1250	1350	1450	
Differential Inputs Driven Single-ended (Figures 5 & 7)						
V_{th}	Input Threshold Reference Voltage Range (Note 7)		1000		VCC - 100	mV
V_{IH}	Single-ended Input HIGH Voltage		Vth +100		VCC	mV
V_{IL}	Single-ended Input LOW Voltage		VEE		Vth - 100	mV
V_{ISE}	Single-ended Input Voltage (V_{IH} - V_{IL})		200		1200	mV
Differential D/Db, CLK/CLKb, R/Rb Inputs Driven Differentially (Figures 6 & 8) (Note 8)						
V_{IHD}	Differential Input HIGH Voltage		1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		V_{EE}		V_{CC} - 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} - V_{ILD})		100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 9) (Figure 9)		1050		V_{CC} - 50	mV
I_{IH}	Input HIGH Current (VTx/VTxb Open)		-150		150	uA
I_{IL}	Input LOW Current (VTx/VTxb Open)		-150		150	uA
Termination Resistors						
R_{TIN}	Internal Input Termination Resistor		40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor		40	50	60	Ω
R_T Coef	Internal Output Termination Resistor Temperature Coefficient			TBD		mΩ/°C

Note: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}.
6. CML outputs loaded with 50-Ω to V_{CC} for proper operation.
7. Vth, V_{IH}, $V_{IL,}$ and V_{ISE} parameters must be complied with simultaneously.
8. Vth is applied to the complementary input when operating in single-ended mode.
9. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS V_{CC} = 1.71 V to 2.625 V; V_{EE} = 0 V; TA = -40°C to 85°C (Note 10)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency		10			GHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 11) (Figures 8 & 10)	$f_{in} \le$ 7GHz $f_{in} \le$ 10GHz	300 200	400 300		mV mV
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs, 1GHz, measured at differential cross-point	CLK/CLKb toQ,Qb R/Rb to Q/Qb		100 150		ps
t_S	Set-Up Time (D to CLK)		TBD			ps
t_H	Hold Time (D to CLK)		TBD			ps
t_{RR}	Reset Recovery		TBD			ps
t_{PW}	Minimum Pulse Width	R/Rb	TBD			ps
t_{PLH} TC	Propagation Delay Temperature Coefficient			50		Δfs/°C
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \le$ 7.0GHz	45	50	55	%
t_{JITTER}	RJ – Output Random Jitter (Note 12)	f_{in} = 10GHz		0.5	0.8	ps RMS
V_{INPP}	Input Voltage Swing (Differential Configuration)(Figure 10) (Note 13)		100		1200	mV
t_r, t_f	Output Rise/Fall Times @ 1 GHz (20% - 80%), Q, Qb			30	50	ps

10. Measured using a V_{INPP}pk-pk min source, 50% duty cycle clock source. All output loading with external 50-Ω to V_{CC}. Input edge rates 40 ps (20% - 80%).
11. Output voltage swing is a single-ended measurement operating in differential mode.
12. Additive RMS jitter with 50% duty cycle clock signal.
13. Input voltage swing is a single-ended measurement operating in differential mode.

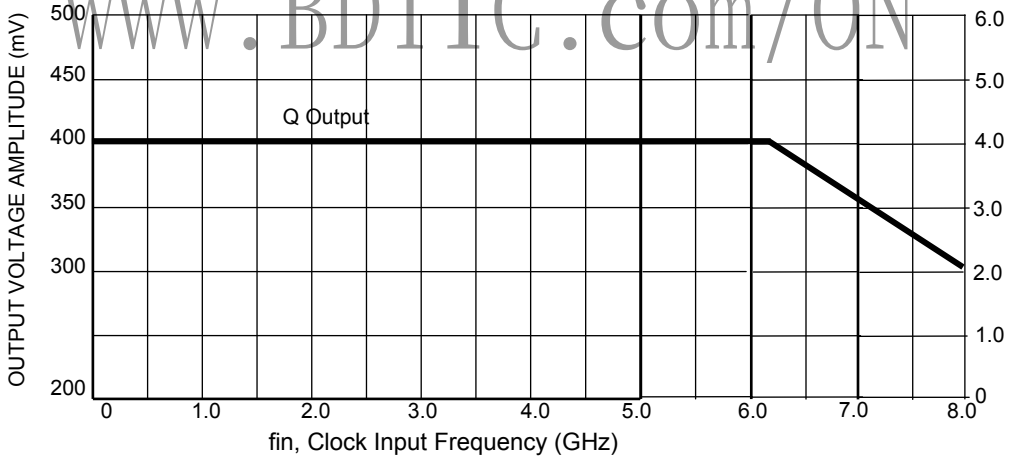


Figure 3. CLOCK Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (typical)

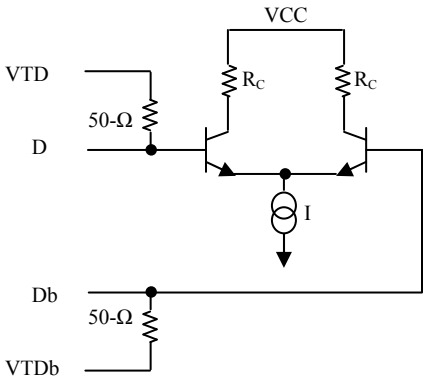


Figure 4. Input Structure

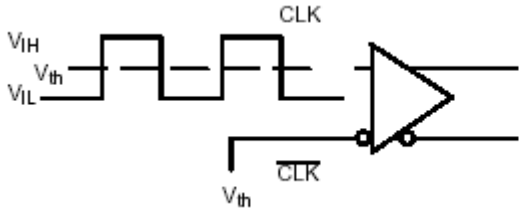


Figure 5. Differential Input Driven Single-Ended

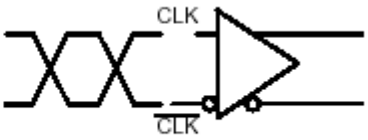


Figure 6. Differential Inputs Driven Differentially

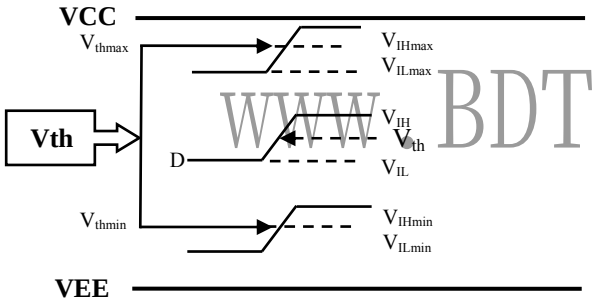


Figure 7. V_{th} Diagram

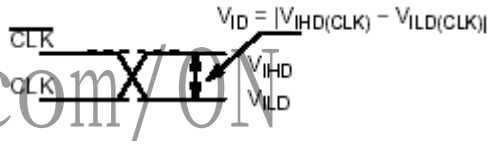


Figure 8. VID - Differential Inputs Driven Differentially

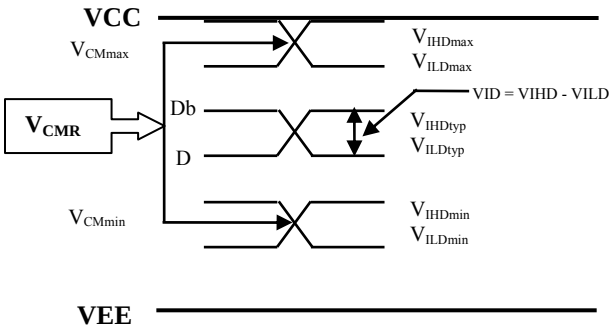


Figure 9. VCMR Diagram

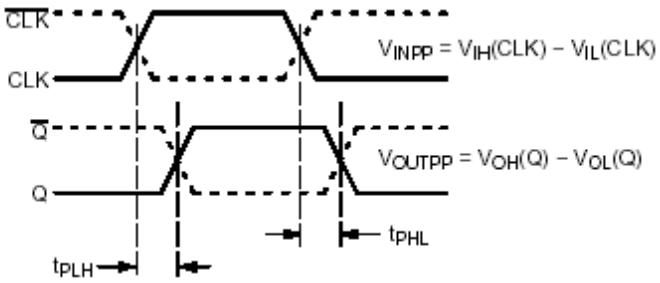


Figure 10. AC Reference Measurement

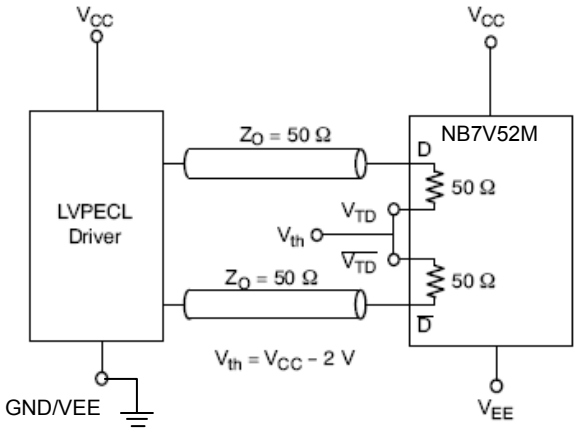


Figure 10. LVPECL Interface

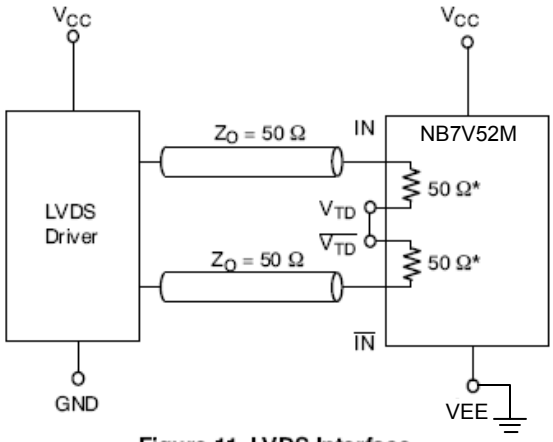


Figure 11. LVDS Interface

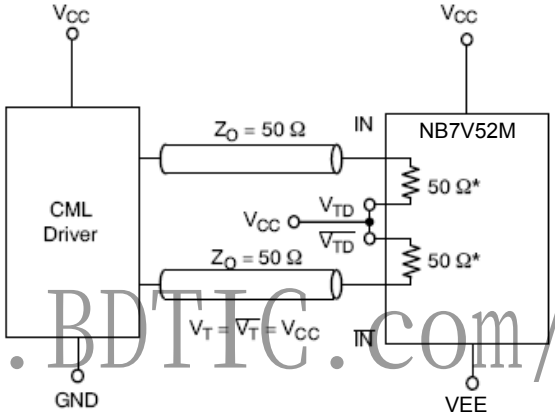


Figure 12. Standard 50 Ω Load CML Interface

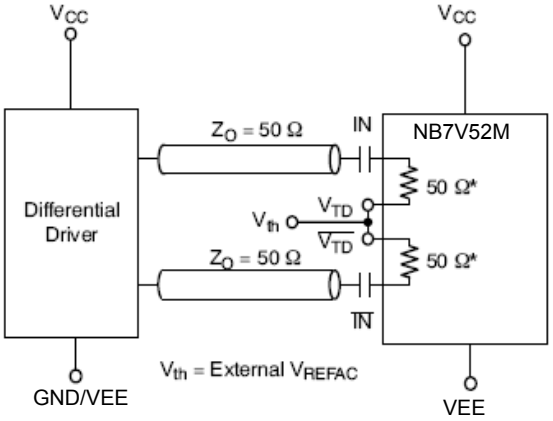


Figure 13. Capacitor−Coupled Differential Interface ($V_{TD}/\overline{V_{TD}}$ Connected to V_{REFAC}; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

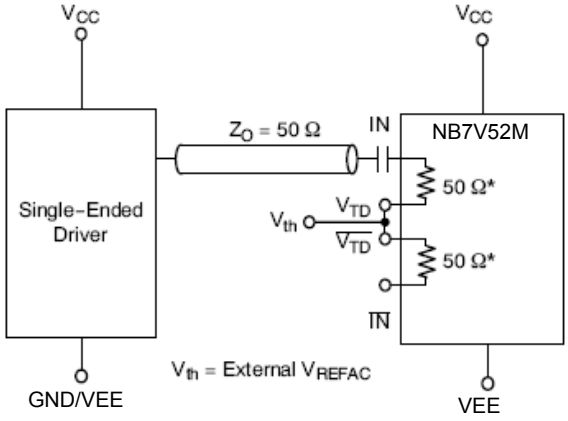


Figure 14. Capacitor−Coupled Single−Ended Interface ($V_T/\overline{V_T}$ Connected to V_{REFAC}; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

Figure 11. Input Interface Options

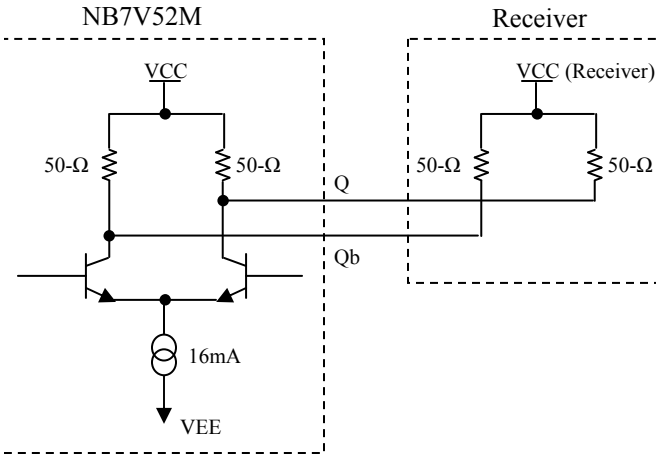


Figure 12. Typical CML Output Structure and Termination

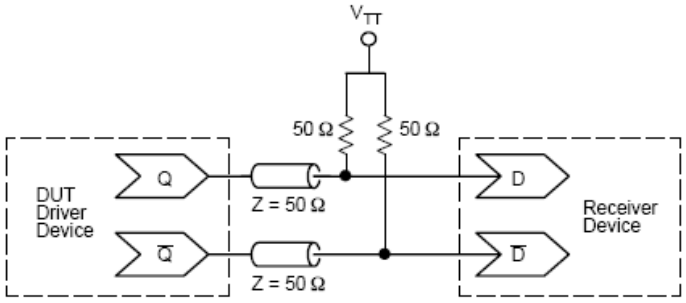
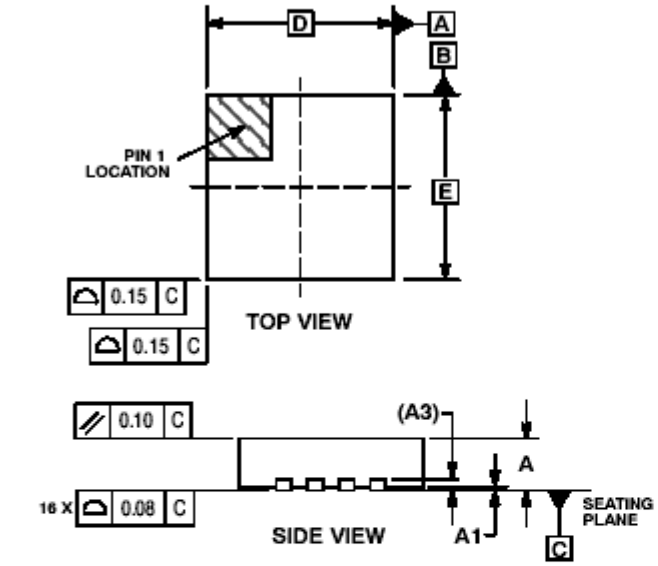


Figure 13. Typical Termination for Output Driver and Device Evaluation
(see Application Note AND8173AND8173)

Device	Package	Shipping
NB7V52MMNG	QFN-16 (Pb-free)	123 Units / Rail
NB7V52MMNR2G	QFN-16 (Pb-free)	3000 / Tape & Reel

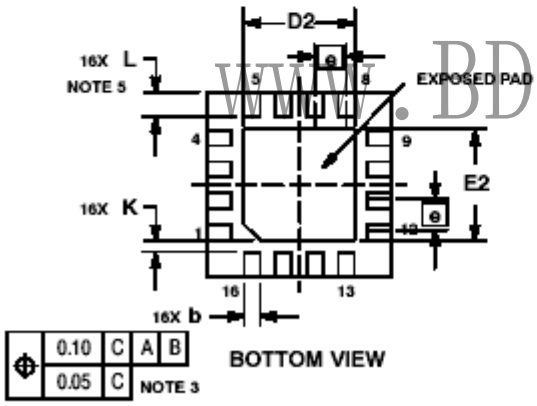
PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G−01
ISSUE B

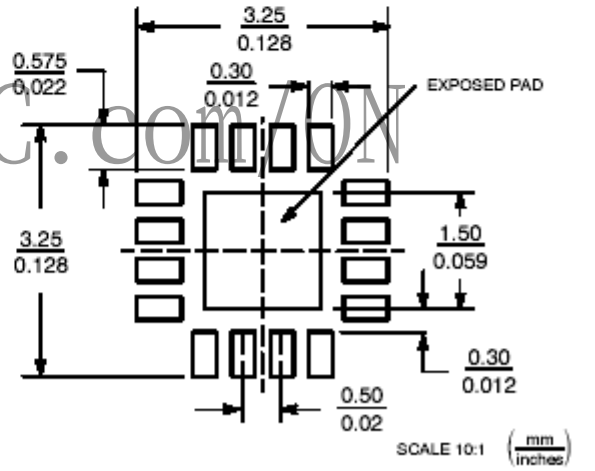


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	---
L	0.30	0.50



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.