NCP367

Battery Charge Front−End Protection, USB and AC/DC Supply Compliant

NCP367 is a charge path protection device which allows disconnecting the systems from its output pin in case wrong charging conditions are detected. The system is positive overvoltage protected up to +30 V. Thanks to a very low current consumption, the USB charge is compatible with this integrated component.

This device uses internal PMOS FET, making external devices unnecessary, which reduces the system cost and PCB area of the application board. First, NCP367 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold. Additional overcurrent protection function allows turning off internal PMOS FET when the charge current exceeds current limit, which is externally selectable.

The current limit value can be modified with control logic pin to divide it by internal gain, allowing USB 100 mA/500 mA charging or USB/Wall adapter charging up to overcurrent threshold. At the same time, Li ion Battery voltage is continuously monitored, providing more safety during the charge. Thermal shutdown protection is also available.

NCP367 provides a negative going flag ($\overline{\text{FLAG}}$) output, which alerts the system that a fault has occurred as overvoltage (power supply or battery voltage), overcurrent or thermal event.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1 μF or larger capacitor.

Features

- Overvoltage Protection Up to + 30 V
- Fast Turn Off Time
- Very Low Current Consumption/USB Compliant
- Li ion Battery Voltage Monitoring
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Overcurrent Protection Externally Adjustable (OCP) up to 2.8 A
- Thermal Shutdown
- Shutdown $\overline{\text{EN}}$ and Gain Input Pins
- Soft−Start to Eliminate Inrush Current
- Alert $\overline{\text{FLAG}}$ Output
- Compliance to IEC61000−4−2 (Level 4)
  8 kV (Contact), 15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 2
- 8 Lead DFN 2.2x2 mm Package
- These are Pb−Free Devices

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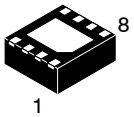
http://onsemi.com



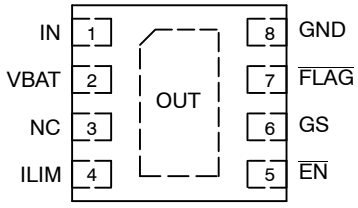
DFN8
MU SUFFIX
CASE 506BP

MARKING DIAGRAM

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(*Note: Microdot may be in either location)

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 10 of this data sheet.

Typical Application

- USB Devices
- Mobile Phones
- Peripheral
- Personal Digital Applications
- MP3 Players

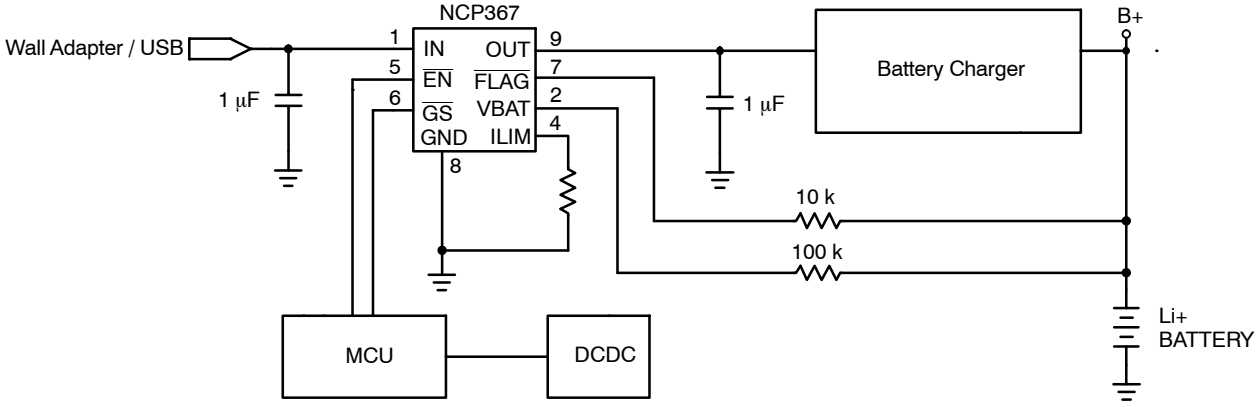


Figure 1. Typical Application Circuit

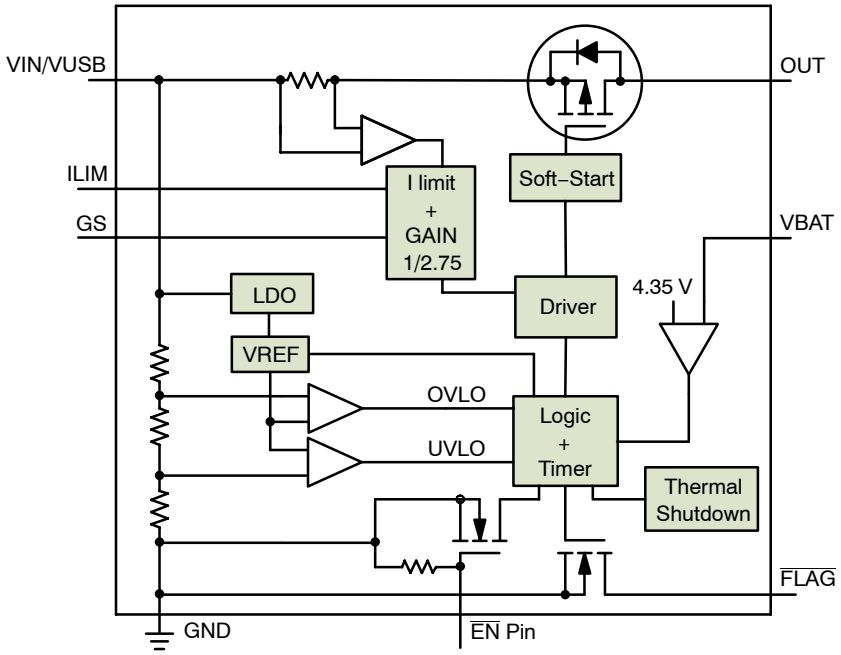


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
1	IN	POWER	Input Voltage Pin. This pin is connected to the power supply: Wall Adapter or USB. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
2	V_{BAT}	INPUT	Li ion Battery voltage sense pin. A serial resistor must be placed between this pin and positive pin of the battery pack.
3	NC	OUTPUT	Not Connected
4	I_{LIM}	OUTPUT	Current Limit Pin. This pin provides the reference, based on the internal band−gap voltage reference, to limit the overcurrent, across internal PMOSFET, from IN to OUT. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the Overcurrent Limit.
5	$\overline{EN}$	INPUT	Enable Mode Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. The state of this pin does not have an impact on the fault detection of the $\overline{FLAG}$ pin.
6	GS	INPUT	Gain Select Pin. When the GS pin is tied to 0 level, the Overcurrent threshold is defined by Ilimit setting. See logic table. When GS pin is tied to high, the Overcurrent threshold is set to Ilimit/GS
7	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect fault condition. The $\overline{FLAG}$ pin goes low when input voltage is below UVLO threshold, exceeds OVLO threshold, charge current from wall adapter to battery exceeds programmed current limit, Li ion Battery voltage (4.3 V) is exceeded or internal temperature exceeds thermal shutdown limit. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull−up resistor to VBattery must be added (10 kΩ minimum value).
8	GND	POWER	Ground.
9	OUT	OUTPUT	Output Voltage Pin. This pin follows IN pin when “no input fault” is detected. The output is disconnected from the Vin power supply when voltage, current or thermal fault events are detected. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.

NOTE: Pin out provided for concept purpose only and might change in the final product

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	$Vmin_{in}$	−0.3	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{in}$	30	V
Maximum Voltage (All others to GND)	Vmax	7.0	V
Maximum DC Current from Vin to Vout (PMOS)	Imax	3.4	A
Thermal Resistance, Junction−to−Air (without PCB area)	$R_{\theta JA}$	190	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Operating Temperature	T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), Model = 2 (Note 1) Machine Model (MM) Model = B (Note 2)	Vesd	15 Air, 8.0 Contact 2000 200	kV V V
Latchup	LU	Class 1	–
Moisture Sensitivity	MSL	Level 1	–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
2. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS

(Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}		1.2		28	V
Undervoltage Lockout Threshold	UVLO	V_{in} falls down UVLO threshold	1.75	1.85	1.9	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$			80	100	mV
Overvoltage Lockout Threshold	OVLO	V_{in} rises up OVLO threshold				V
NCP367OPMUEA			3.65	3.8	3.95	
NCP367DPMUEC			5.64	5.85	6.05	
NCP367DPMUEE			5.85	6.07	6.28	
NCP367DPMUEL			6.60	6.84	7.08	
NCP367OPMUEO			6.90	7.20	7.50	
NCP367DPMUEB			4.38	4.54	4.7	
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$			100	150	mV
Vin versus Vout Resistance	$R_{DS(on)}$	V_{in} = 5 V, Enable Mode, Load Connected to V_{out}		50	100	mΩ
Supply Quiescent Current	Idd	No Load		42	130	μA
Disable Mode	Idd_{dis}	$\overline{EN}$ = 1.2 V		40	110	μA
Overcurrent Threshold	I_{OCP}	V_{in} = 5 V, $\overline{EN}$ = low, Load Connected to V_{out},,				A
NCP367Dx		R_{ilim} = 0 Ω, 1 A/μs, $\overline{GS}$ = 0.4 V	1.25	1.51	1.80	
NCP367Ox			2.30	2.85	3.40	
Overcurrent Response	I_{reg}	1 A/μs, $\overline{GS}$ = low, I_{lim} = 1.51 A		5.0		%
Current Limit Gain NCP367D	GS_{value}	$\overline{GS}$ = 1.2 V		2.70		
NCP367O				2.55		
Battery Overvoltage Threshold	OV_{BAT}	0°C to 85°C	4.3	4.35	4.4	V
Battery Overvoltage Hysteresis	OV_{HYS}	0°C to 85°C	100	150	200	mV
V_{BAT} Pin Leakage	$VBAT_{LEAK}$				20	nA
V_{BAT} Deglitch Time	$VBAT_{DEG}$	V_{BAT} > OV_{BAT}	0.2	2.0	4.0	ms
FLAG Output Low Voltage	Vol_{flag}	V_{in} > OVLO Sink 1 mA on FLAG pin			400	mV
FLAG Leakage Current	$\overline{FLAG}_{leak}$	$\overline{FLAG}$ level = 5 V		10		nA
$\overline{EN}$ Voltage High	V_{ih}	V_{in} from 3.3 V to 5.25 V	1.2			V
$\overline{EN}$ Voltage Low	V_{il}	V_{in} from 3.3 V to 5.25 V			0.4	V
EN Leakage Current	$\overline{EN}_{leak}$	$\overline{EN}$ = 5.5 V or GND		200		nA
$\overline{GS}$ Voltage High	V_{ih}	V_{in} from 3.3 V to 5.25 V	1.2			V
$\overline{GS}$ Voltage Low	V_{il}	V_{in} from 3.3 V to 5.25 V			0.4	V
$\overline{GS}$ Leakage Current	GS_{leak}	$\overline{EN}$ = 5.5 V or GND		200		nA
TIMINGS						
Start Up Delay	t_{on}	From V_{in} > UVLO to V_{out} = 0.8xV_{in}	15	30	45	ms
FLAG going up Delay	t_{start}	From V_{out} > 0.2xV_{in} to $\overline{FLAG}$ = 1.2 V	15	30	45	ms
Rearming Delay	t_{REARM}	OCP Active	15	30	45	ms
Overcurrent Regulation Time	t_{REG}	OCP Active	1.2	1.8	3.0	ms
Output Turn Off Time	t_{off}	From V_{in} > OVLO to V_{out} ≤ 0.3 V, V_{in} increasing from 5 V to 8 V at 3 V/μs.		1.5	5.0	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to $\overline{FLAG}$ ≤ 0.4 V, (see Figure 16) V_{in} increasing from 5 V to 8 V at 3 V/μs		1.5		μs
Disable Time	t_{dis}	From $\overline{EN}$ 0.4 to 1.2 V to V_{out} ≤ 0.3 V		3.0		μs
Thermal Shutdown Temperature	T_{sd}			150		°C
Thermal Shutdown Hysteresis	Tsd_{hyst}			30		°C

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

TYPICAL OPERATING CHARACTERISTICS

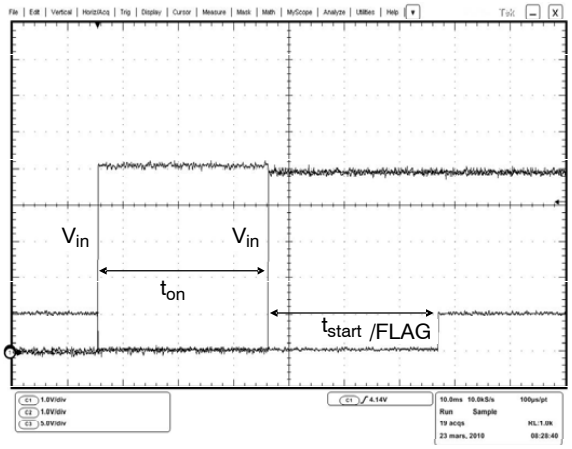


Figure 3. Hot Plug−in from 0 to 5 V, t_{on} and t_{start}

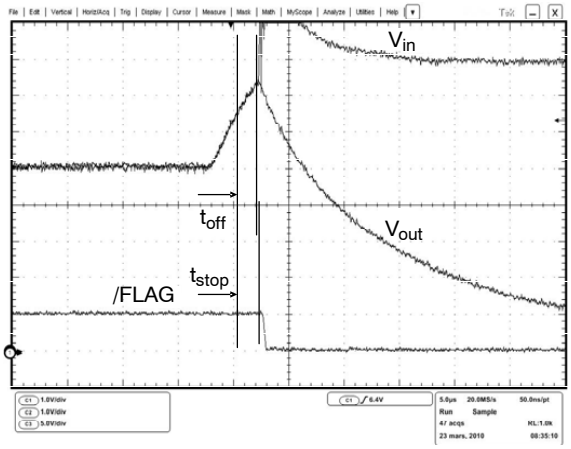


Figure 4. Overvoltage from 5 to 8 V, t_{off} and t_{stop}

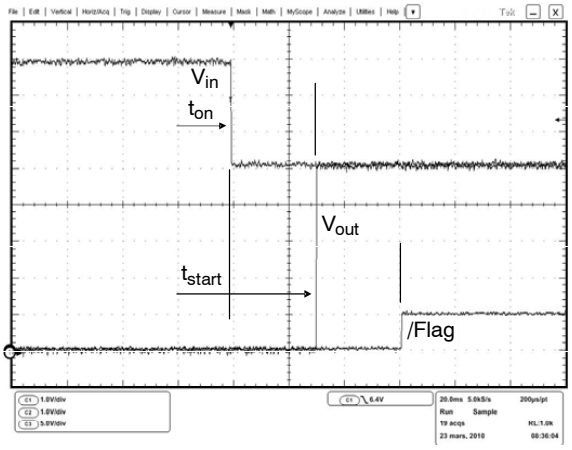


Figure 5. Retrieve Normal Operation, t_{on} and t_{start}

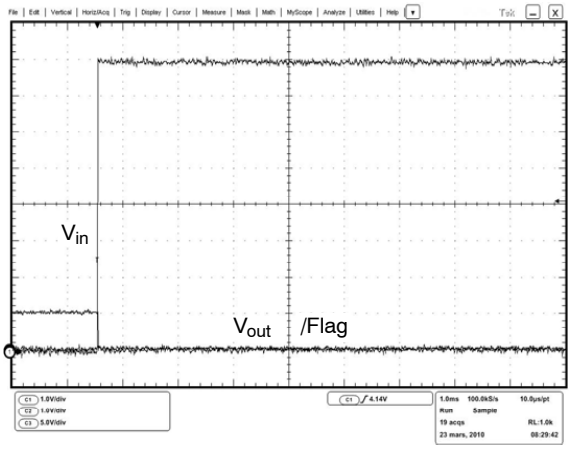


Figure 6. Overvoltage from 0 to 10 V

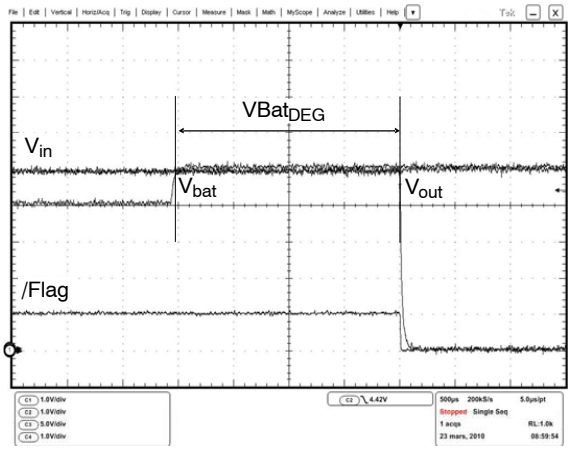


Figure 7. Battery Overvoltage, Deglitch Time

TYPICAL OPERATING CHARACTERISTICS

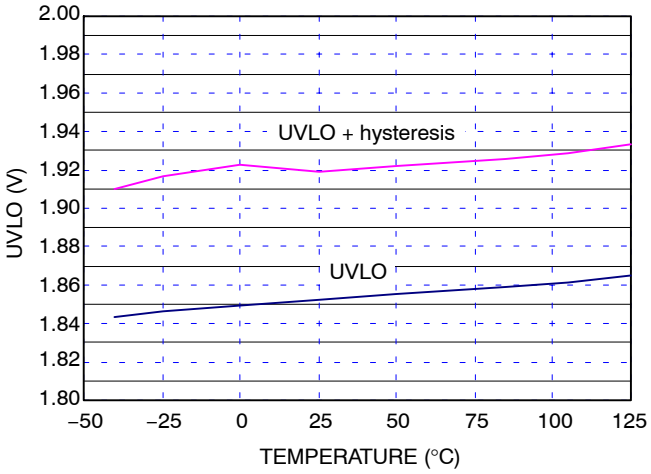


Figure 8. UVLO and Hysteresis

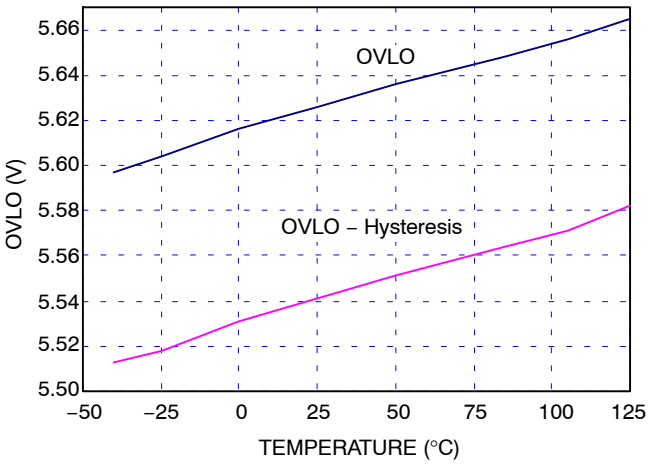


Figure 9. OVLO and Hysteresis vs. Temperature (5.6 V version)

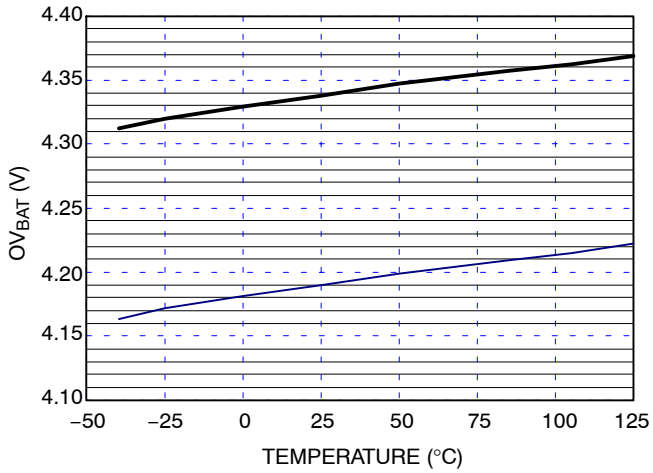


Figure 10. V_{BAT} Threshold and Hysteresis vs. Temperature

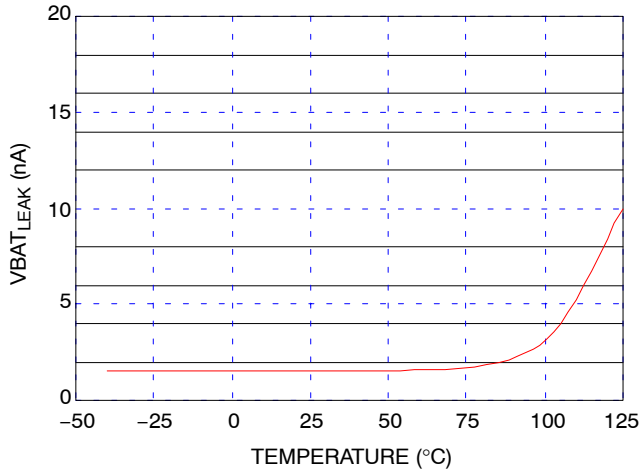


Figure 11. V_{BAT} Pin Leakage vs. Temperature

APPLICATION INFORMATION

Operation

The NCP367 is an integrated IC which offers a complete protection of the portable devices during the Li ion battery charge.

First, the input pin is protected up to +30 V, protecting the down stream system (charger, transceiver, system...) against the power supply transients such as inrush current or defective functionality. Additional protection level is offered with the overcurrent block which eliminates current peak or opens the charge path if an overcurrent default appears.

More of that, the battery voltage is monitored all along the input power supply is connected, allowing to open charge path if Li ion battery voltage exceeds 4.3 V, caused by CCCV charger or battery pack fault.

The integrated pass element (PMOS FET) is sized to support very high charge DC current up to 2.3 A. The overcurrent threshold can be externally adjusted with a pull−down resistor and gain select pin is available to divide current limit threshold with internal fixed gain. Allowing to adjust with logic pin the overcurrent threshold if USB/500 mA or WA/1.5 A is detected, without changing R_{ILIM} resistor, in example.

Undervoltage, Overvoltage, Overcurrent and thermal faults are signalized thanks to the open drain $\overline{FLAG}$ pin, by pulling its down.

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in undervoltage lock out (UVLO) circuit. During Vin positive going slope, the output remains disconnected from input until Vin voltage is above 1.85 V plus hysteresis nominal. This circuit has a 80 mV hysteresis to provide noise immunity to transient condition.

Overvoltage Lockout (OVLO)

To protect connected systems on Vout pin from overvoltage, the device has a built−in overvoltage lock out (OVLO) circuit. During overvoltage condition, the output remains disabled as long as the input voltage exceeds this threshold.

$\overline{FLAG}$ output is tied to low as long as Vin is higher than OVLO. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

$\overline{FLAG}$ Output

NCP367 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon as the OVLO, OV_{BAT}, I_{OCP} or internal temperature thresholds are exceeded and remains low until between minimum driving voltage and UVLO threshold. When Vin level recovers normal condition, $\overline{FLAG}$ is held high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ − Minimum 10 kΩ) must be provided to V_{CC}. $\overline{FLAG}$ pin is an open drain output, which is able to support 1 mA maximum.

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive a UVLO or OVLO fault.

Overcurrent Protection (OCP)

This device integrates the overcurrent protection function, from wall adapter to battery. That means the current across the internal PMOS is regulated and cut when the value, set by external RSEL resistor, exceeds I_{LIM} longer than t_{REG}.

An internal resistor is placed in series with the pin allowing to have a maximum OCP value when I_{LIM} pin is directly connected to GND.

By adding external resistors in series with I_{LIM} and GND, the OCP value is decreased.

An additional logic pin, $\overline{GS}$ (gain select), is very useful in case of different charge rate is necessary (Wall adapter and USB, for example).

By setting $\overline{GS}$ to 0.4 V, overcurrent thresholds are depending on R select resistor, which is connect between pin 4 and GND. When the $\overline{GS}$ pin is tied to 1.2 V (high logic level) the preselected current limit is divided by 2.75. Due

to this option, both fast charge or USB charge are authorized with the same device.

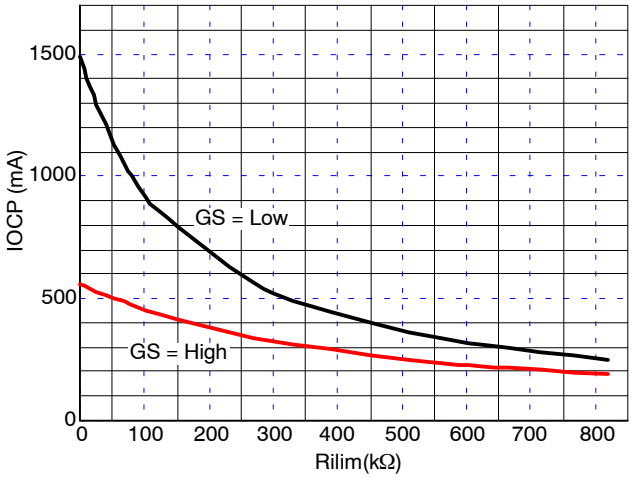


Figure 12. I_{OCP} versus R_{LIM}, GS = low and high, 1.5 A version

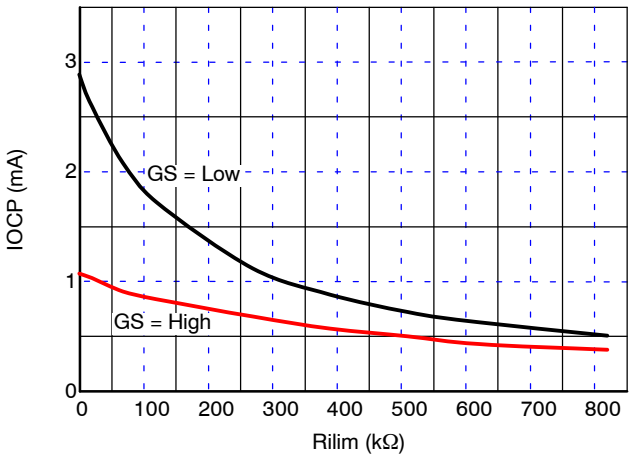


Figure 13. Over Current Threshold versus R_{LIMIT} 2.85 A Version

Typical R_{LIM} calculation is following:
NCP367DxMUxxTBG

$$R_{LIM}\ (k\Omega) = 249 / I_{OCP} - 165$$

NCP367OxMUxxTBG

$$R_{LIM}\ (k\Omega) = 532 / I_{OCP} - 180$$

During overcurrent event, charge area is opened and $\overline{FLAG}$ output is tied to low, allowing the µController to take into account the fault event and then open the charge path.

At power up (accessory is plugged on input pins), the current is limited up to I_{LIM} during 1.8 ms (typical), to allow capacitor charge and limit inrush current. If the I_{LIM} threshold is exceeded over 1.8 ms, the device enter in OCP burst mode until the overcurrent event disappears.

V_{BAT} Sense

The connection of the V_{BAT} pin to the positive connection of the Li ion battery pack allows preventing overvoltage transient, greater than 4.35 V. In case of wrong charger conditions, the PMOS is then opened, eliminating Battery pack over voltage which could create safety issues and temperature increasing.

The 4.35 V comparator has a 150 mV built−in hysteresis.

More of that, deglitch function of 2 ms is integrated to prevent voltage transients on the Battery voltage. If the battery over voltage condition exceeds deglitch time, the charge path is opened and $\overline{FLAG}$ pin is tied to low level until the V_{BAT} is greater than 4.35 V – hysteresis.

At wall adapter insertion, and if the battery is fully charged, V_{bat} comparator stays locked until battery needs to be recharged (4.2 V typ – 4.1 V min).

A serial resistor has to be placed in series with Vbat pin and battery connection, with a 200 kΩ recommended value.

PCB Recommendations

The NCP367 integrates low $R_{DS(on)}$ PMOS FET, nevertheless PCB layout rules must be respected to properly evacuate the heat out of the silicon. The DFN PAD1 corresponds to the PMOS drain so must be connected to OUT plane to increase the heat transfer. Of course, in any case, this pad shall be not connected to any other potential.

Following figure shows package thermal resistance of a DFN 2.2x2 mm.

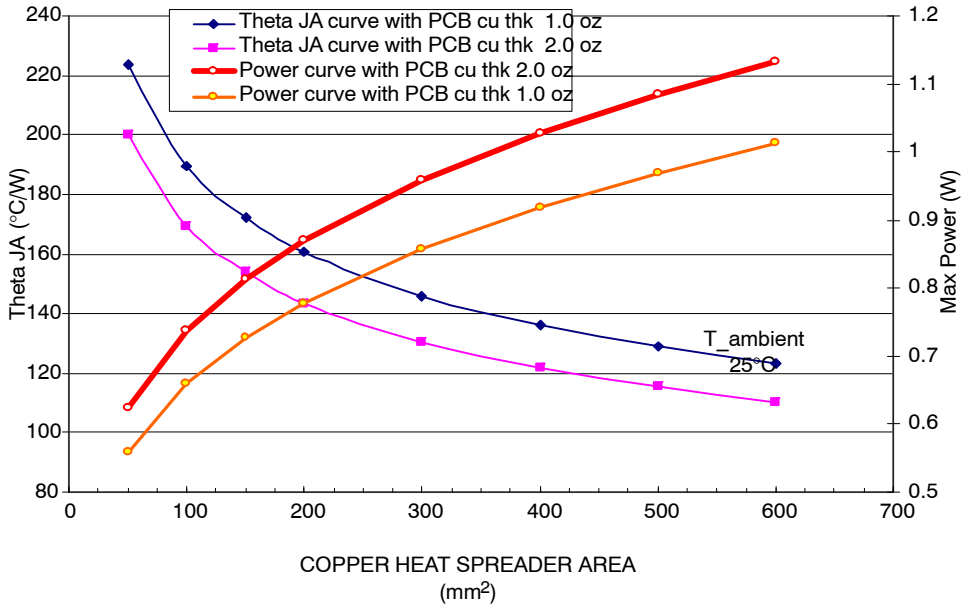


Figure 14.

Internal PMOS FET

NCP367 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive over−voltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin versus V_{in}, due to very low $R_{DS(on)}$.

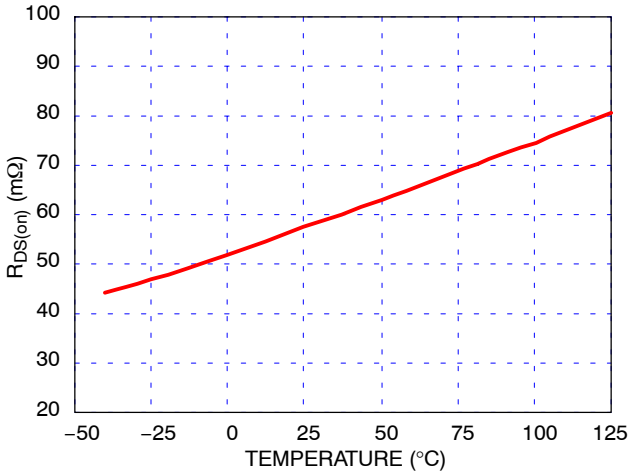


Figure 15. Typical $R_{DS(on)}$ versus Temperature

ESD Tests

NCP367 fully support the IEC61000−4−2, level 4 (Input pin, 1 μF mounted on board). That means, in Air condition, Vin has a ±15 kV ESD protected input. In Contact condition, Vin has ±8 kV ESD protected input. Please refer to Figure 16 to see the IEC 61000−4−2 electrostatic discharge waveform.

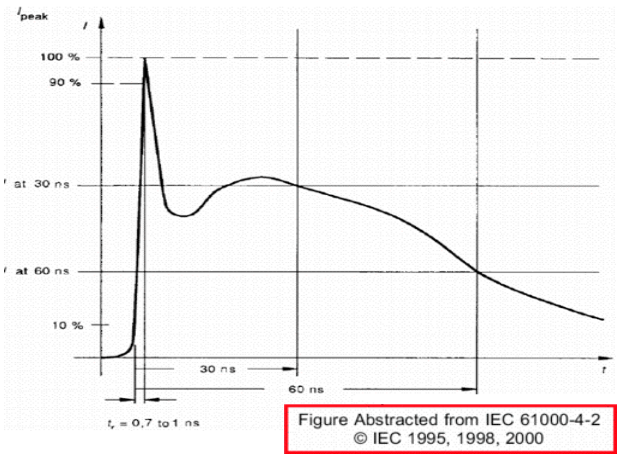


Figure 16. IEC 61000−4−2 Electrostatic Discharge

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP367DPMUECTBG	DC	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP367DPMUEETBG	DE	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP367DPMUELTBG	DL	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP367OPMUEOTBG	P3	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP367OPMUEATBG	EA	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP367DPMEBTBG	PE	DFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SELECTION GUIDE

The NCP367 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:

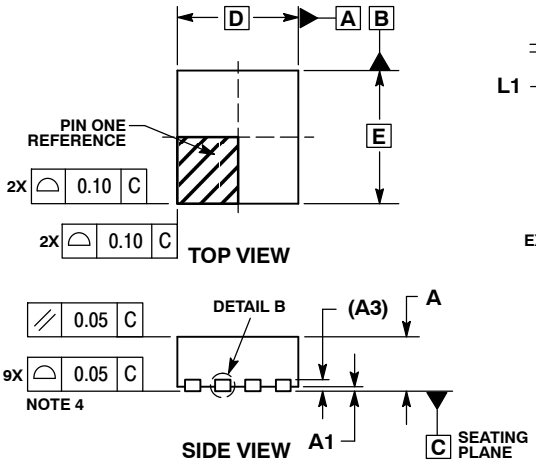
NCP367xxMUxxTBG

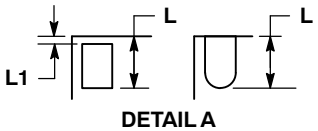
a b c d

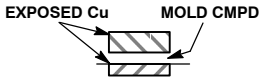
Code	Contents
a	Overcurrent threshold a = D: 1.51 A a = O: 2.85 A
b	V_{BAT} Voltage b: P = 4.36 V (additional thresholds available for a wide Lithium ion material range)
c	UVLO Typical Threshold c: E = 1.85 V
d	OVLO Typical Threshold (Additional thresholds available) d: C = 5.85 V d: E = 6.07 V d: L = 6.85 V d: O = 7.20 V d: A = 3.80 V d: B = 4.54 V

PACKAGE DIMENSIONS

DFN8, 2.0x2.2, 0.5P
CASE 506BP
ISSUE A



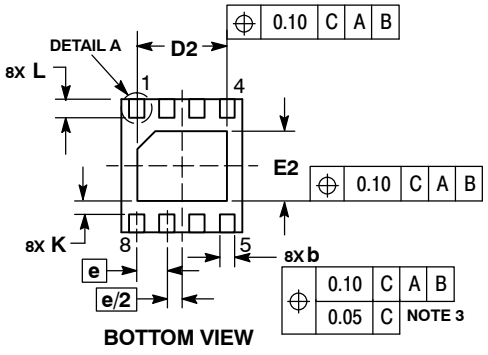




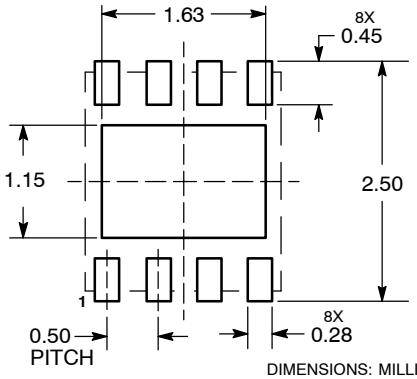
DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	TYP	MAX
A	0.80	---	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.20	---	0.30
D		2.00 BSC	
D2	1.43	---	1.53
E		2.20 BSC	
E2	1.05	---	1.25
e		0.50 BSC	
K	0.20	0.22	0.30
L	0.25	---	0.35
L1	---	---	0.15



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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