

MC33201, MC33202, MC33204, NCV33202, NCV33204

Low Voltage, Rail-to-Rail Operational Amplifiers

The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

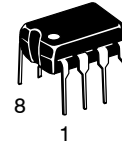
Features

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over-driven Input Signals
- High Output Current ($I_{SC} = 80$ mA, Typ)
- Low Supply Current ($I_D = 0.9$ mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges (-40° to $+105^\circ$ C and -55° to $+125^\circ$ C)
- Typical Gain Bandwidth Product = 2.2 MHz
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- Pb-Free Packages are Available



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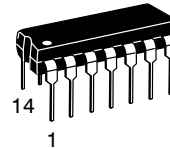
PDIP-8
P, VP SUFFIX
CASE 626



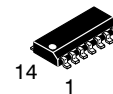
SOIC-8
D, VD SUFFIX
CASE 751



Micro8™
DM SUFFIX
CASE 846A



PDIP-14
P, VP SUFFIX
CASE 646



SOIC-14
D, VD SUFFIX
CASE 751A



TSSOP-14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 12 of this data sheet.

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PIN CONNECTIONS

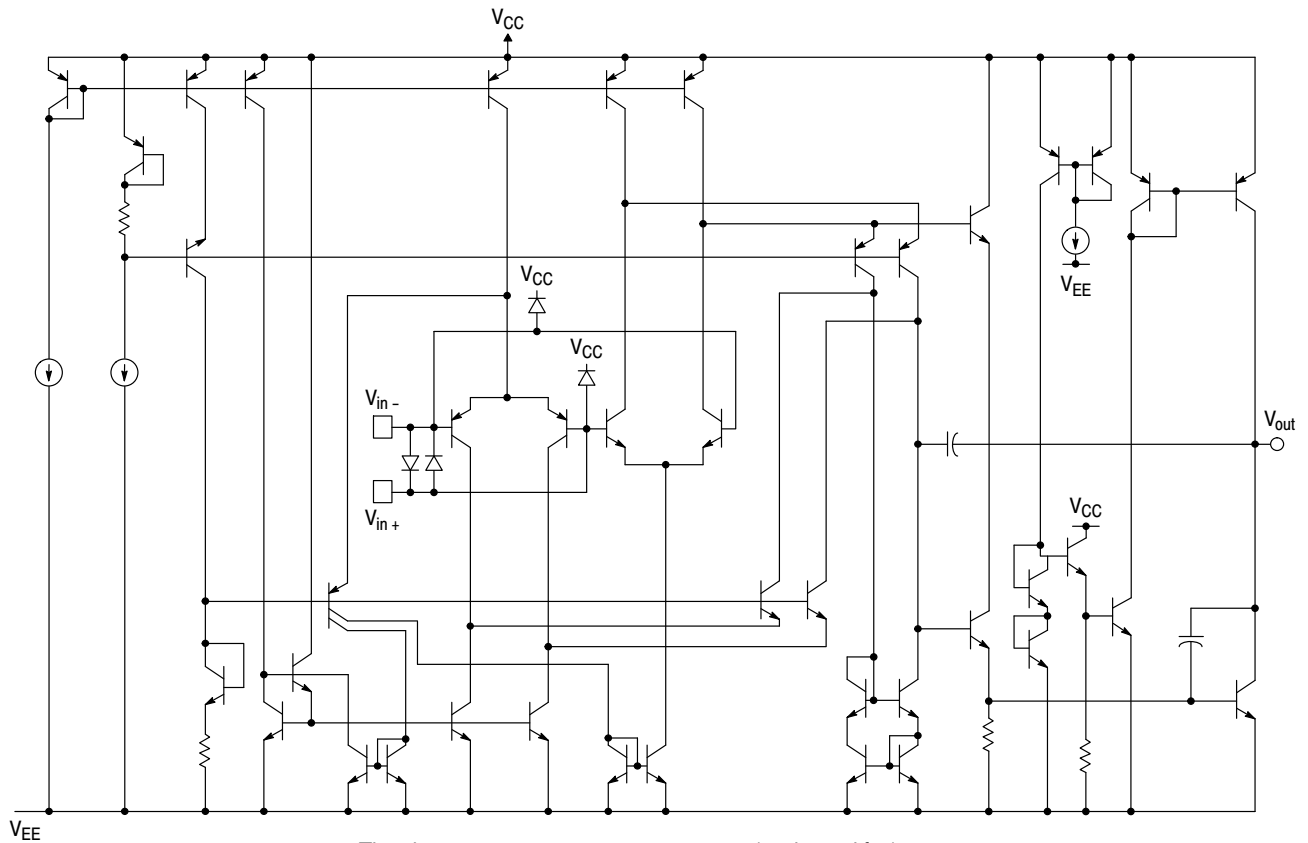
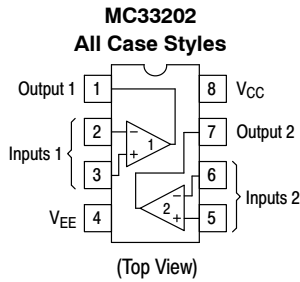
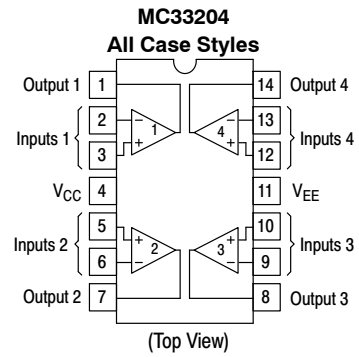
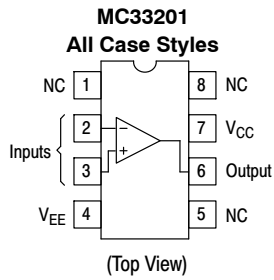


Figure 1. Circuit Schematic
(Each Amplifier)

MC33201, MC33202, MC33204, NCV33202, NCV33204

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------|---|------|
| Supply Voltage (V_{CC} to V_{EE}) | V_S | +13 | V |
| Input Differential Voltage Range | V_{IDR} | Note 1 | V |
| Common Mode Input Voltage Range (Note 2) | V_{CM} | $V_{CC} + 0.5$ V to $V_{EE} - 0.5$ V | V |
| Output Short Circuit Duration | t_s | Note 3 | sec |
| Maximum Junction Temperature | T_J | +150 | °C |
| Storage Temperature | T_{stg} | - 65 to +150 | °C |
| Maximum Power Dissipation | P_D | Note 3 | mW |

DC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

| Characteristic | $V_{CC} = 2.0$ V | $V_{CC} = 3.3$ V | $V_{CC} = 5.0$ V | Unit |
|--|-----------------------------------|-----------------------------------|------------------------------------|------------------------|
| Input Offset Voltage V_{IO} (max) MC33201 MC33202, NCV33202 MC33204, NCV33204 | ± 8.0 ± 10 ± 12 | ± 8.0 ± 10 ± 12 | ± 6.0 ± 8.0 ± 10 | mV |
| Output Voltage Swing V_{OH} ($R_L = 10$ k Ω) V_{OL} ($R_L = 10$ k Ω) | 1.9 0.10 | 3.15 0.15 | 4.85 0.15 | V_{min} V_{max} |
| Power Supply Current per Amplifier (I_D) | 1.125 | 1.125 | 1.125 | mA |

Specifications at $V_{CC} = 3.3$ V are guaranteed by the 2.0 V and 5.0 V tests. $V_{EE} = \text{GND}$.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ V, $V_{EE} = \text{Ground}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|--------------------------|--|--|---|------------------------------|
| Input Offset Voltage ($V_{CM} = 0$ V to 0.5 V, $V_{CM} = 1.0$ V to 5.0 V) MC33201: $T_A = +25^\circ\text{C}$ MC33201: $T_A = -40^\circ$ to $+105^\circ\text{C}$ MC33201V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ MC33202/NCV33202: $T_A = +25^\circ\text{C}$ MC33202/NCV33202: $T_A = -40^\circ$ to $+105^\circ\text{C}$ MC33202V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ NCV33202V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ (Note 4) MC33204: $T_A = +25^\circ\text{C}$ MC33204: $T_A = -40^\circ$ to $+105^\circ\text{C}$ MC33204V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ NCV33204: $T_A = -55^\circ$ to $+125^\circ\text{C}$ | 3 | $ V_{IO} $ | - - - - - - - - - - - - | - - - - - - - - - - - - | 6.0 9.0 13 8.0 11 14 14 10 13 17 17 | mV |
| Input Offset Voltage Temperature Coefficient ($R_S = 50$ Ω) $T_A = -40^\circ$ to $+105^\circ\text{C}$ $T_A = -55^\circ$ to $+125^\circ\text{C}$ | 4 | $\Delta V_{IO}/\Delta T$ | - - | 2.0 2.0 | - - | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current ($V_{CM} = 0$ V to 0.5 V, $V_{CM} = 1.0$ V to 5.0 V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+105^\circ\text{C}$ $T_A = -55^\circ$ to $+125^\circ\text{C}$ | 5, 6 | $ I_{IB} $ | - - - | 80 100 - | 200 250 500 | nA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
- The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
- Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)
- All NCV devices are qualified for Automotive use.

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DC ELECTRICAL CHARACTERISTICS (cont.) ($V_{CC} = +5.0\text{ V}$, $V_{EE} = \text{Ground}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|----------|--|------------------------|------------------------------|------------------------|-----------------|
| Input Offset Current ($V_{CM} = 0\text{ V to } 0.5\text{ V}$, $V_{CM} = 1.0\text{ V to } 5.0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to } +105^\circ\text{C}$ $T_A = -55^\circ\text{ to } +125^\circ\text{C}$ | – | $ I_{IO} $ | – | 5.0 10 – | 50 100 200 | nA |
| Common Mode Input Voltage Range | – | V_{ICR} | V_{EE} | – | V_{CC} | V |
| Large Signal Voltage Gain ($V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 600\ \Omega$ | 7 | A_{VOL} | 50 25 | 300 250 | – – | kV/V |
| Output Voltage Swing ($V_{ID} = \pm 0.2\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 600\ \Omega$ $R_L = 600\ \Omega$ | 8, 9, 10 | V_{OH} V_{OL} V_{OH} V_{OL} | 4.85 – 4.75 – | 4.95 0.05 4.85 0.15 | – 0.15 – 0.25 | V |
| Common Mode Rejection ($V_{in} = 0\text{ V to } 5.0\text{ V}$) | 11 | CMR | 60 | 90 | – | dB |
| Power Supply Rejection Ratio $V_{CC}/V_{EE} = 5.0\text{ V/GND to } 3.0\text{ V/GND}$ | 12 | PSRR | 500 | 25 | – | $\mu\text{V/V}$ |
| Output Short Circuit Current (Source and Sink) | 13, 14 | I_{SC} | 50 | 80 | – | mA |
| Power Supply Current per Amplifier ($V_O = 0\text{ V}$) $T_A = -40^\circ\text{ to } +105^\circ\text{C}$ $T_A = -55^\circ\text{ to } +125^\circ\text{C}$ | 15 | I_D | – – | 0.9 0.9 | 1.125 1.125 | mA |

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V}$, $V_{EE} = \text{Ground}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|--|------------|----------|--------|----------------|--------|---------------------------|
| Slew Rate ($V_S = \pm 2.5\text{ V}$, $V_O = -2.0\text{ V to } +2.0\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $A_V = +1.0$) | 16, 26 | SR | 0.5 | 1.0 | – | V/ μs |
| Gain Bandwidth Product ($f = 100\text{ kHz}$) | 17 | GBW | – | 2.2 | – | MHz |
| Gain Margin ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$) | 20, 21, 22 | A_M | – | 12 | – | dB |
| Phase Margin ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$) | 20, 21, 22 | ϕ_M | – | 65 | – | Deg |
| Channel Separation ($f = 1.0\text{ Hz to } 20\text{ kHz}$, $A_V = 100$) | 23 | CS | – | 90 | – | dB |
| Power Bandwidth ($V_O = 4.0\text{ V}_{pp}$, $R_L = 600\ \Omega$, $\text{THD} \leq 1\%$) | | BW_P | – | 28 | – | kHz |
| Total Harmonic Distortion ($R_L = 600\ \Omega$, $V_O = 1.0\text{ V}_{pp}$, $A_V = 1.0$) $f = 1.0\text{ kHz}$ $f = 10\text{ kHz}$ | 24 | THD | – – | 0.002 0.008 | – – | % |
| Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 2.0\text{ MHz}$, $A_V = 10$) | | $ Z_O $ | – | 100 | – | Ω |
| Differential Input Resistance ($V_{CM} = 0\text{ V}$) | | R_{in} | – | 200 | – | k Ω |
| Differential Input Capacitance ($V_{CM} = 0\text{ V}$) | | C_{in} | – | 8.0 | – | pF |
| Equivalent Input Noise Voltage ($R_S = 100\ \Omega$) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$ | 25 | e_n | – – | 25 20 | – – | nV/ $\sqrt{\text{Hz}}$ |
| Equivalent Input Noise Current $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$ | 25 | i_n | – – | 0.8 0.2 | – – | pA/ $\sqrt{\text{Hz}}$ |

MC33201, MC33202, MC33204, NCV33202, NCV33204

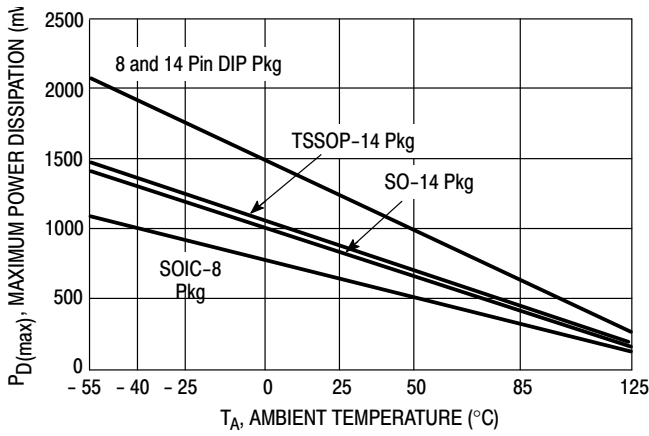


Figure 2. Maximum Power Dissipation versus Temperature

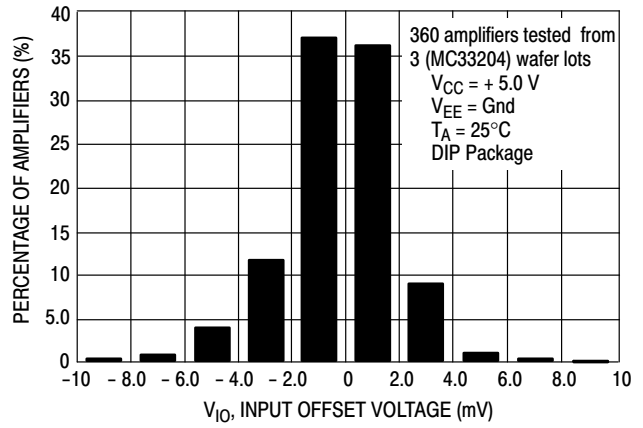


Figure 3. Input Offset Voltage Distribution

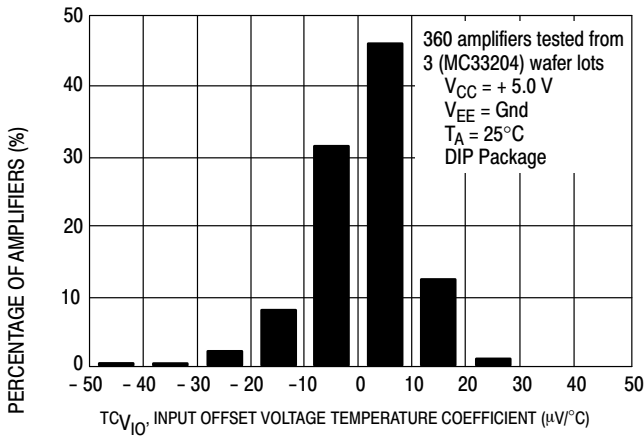


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

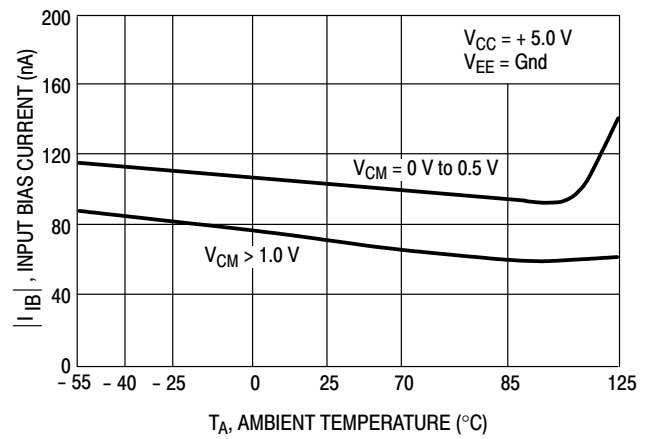


Figure 5. Input Bias Current versus Temperature

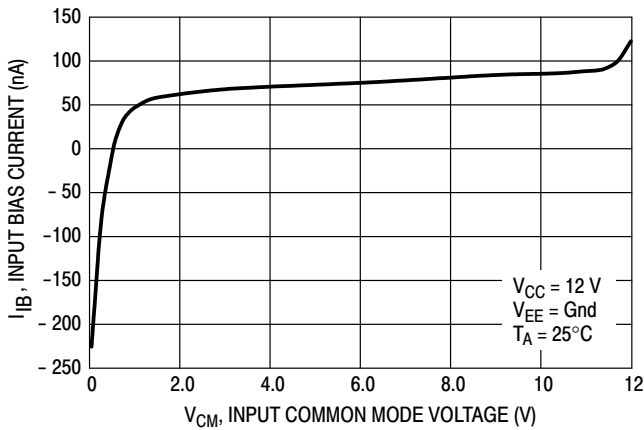


Figure 6. Input Bias Current versus Common Mode Voltage

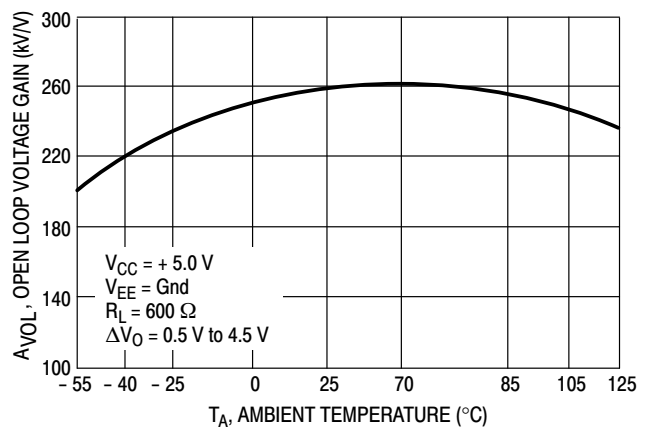


Figure 7. Open Loop Voltage Gain versus Temperature

MC33201, MC33202, MC33204, NCV33202, NCV33204

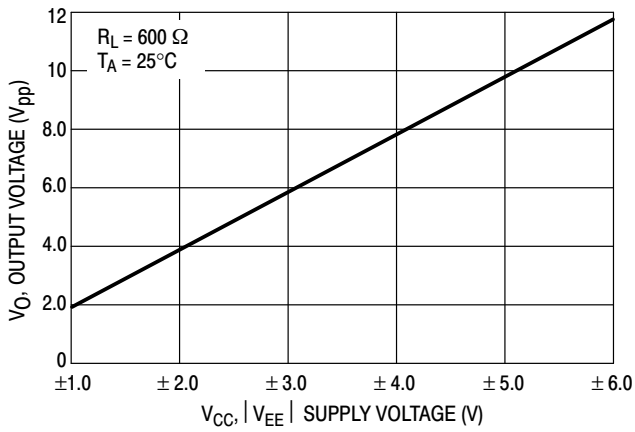


Figure 8. Output Voltage Swing versus Supply Voltage

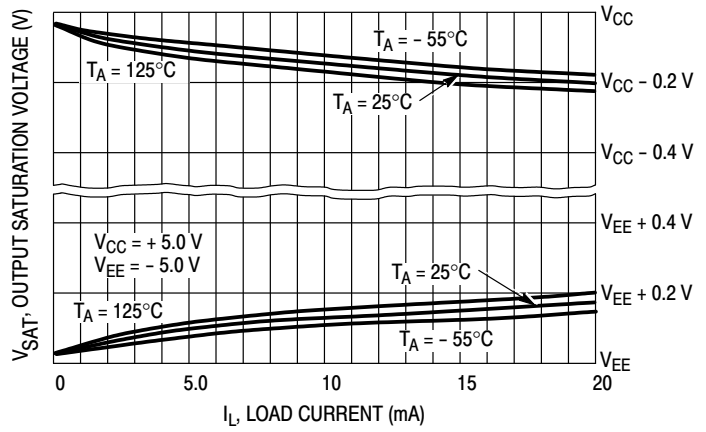


Figure 9. Output Saturation Voltage versus Load Current

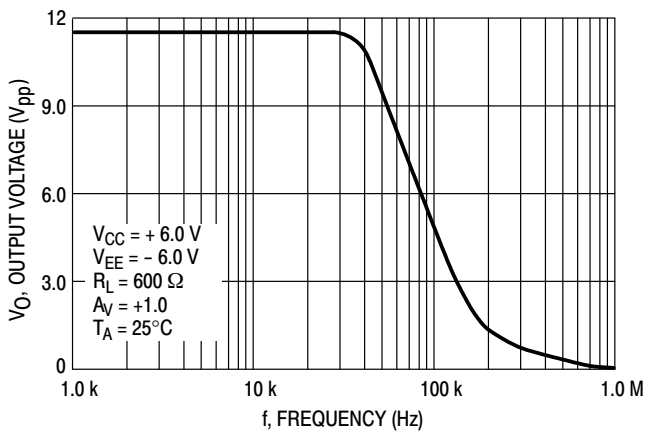


Figure 10. Output Voltage versus Frequency

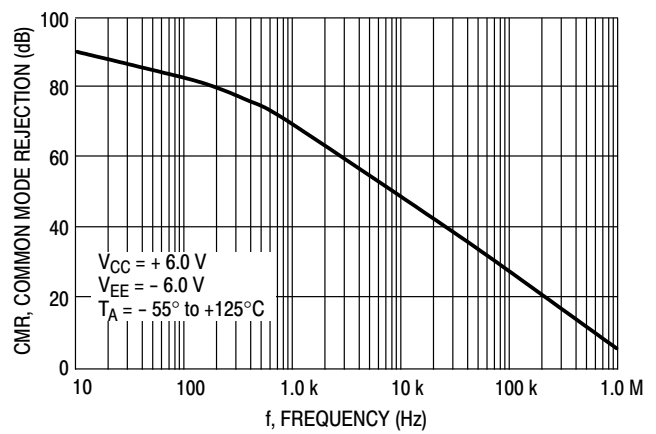


Figure 11. Common Mode Rejection versus Frequency

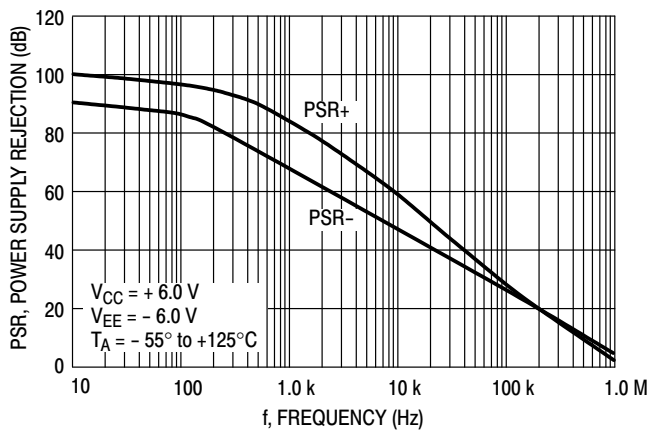


Figure 12. Power Supply Rejection versus Frequency

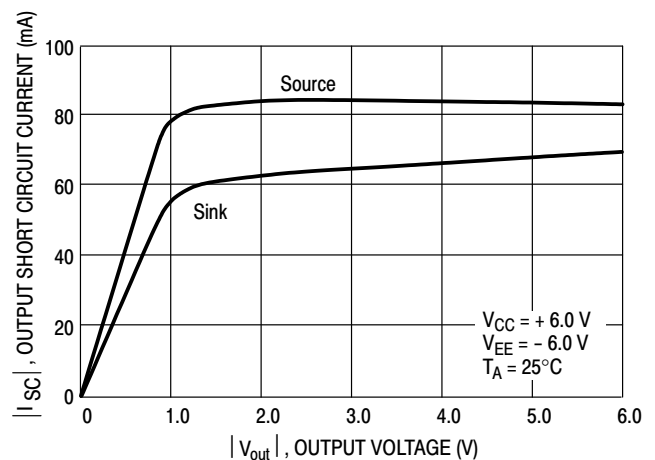


Figure 13. Output Short Circuit Current versus Output Voltage

MC33201, MC33202, MC33204, NCV33202, NCV33204

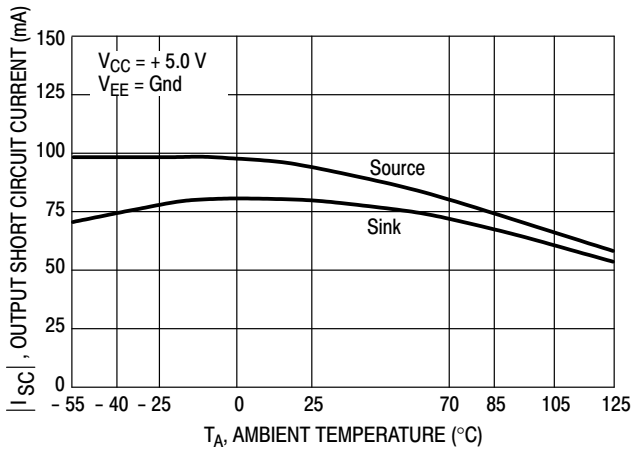


Figure 14. Output Short Circuit Current versus Temperature

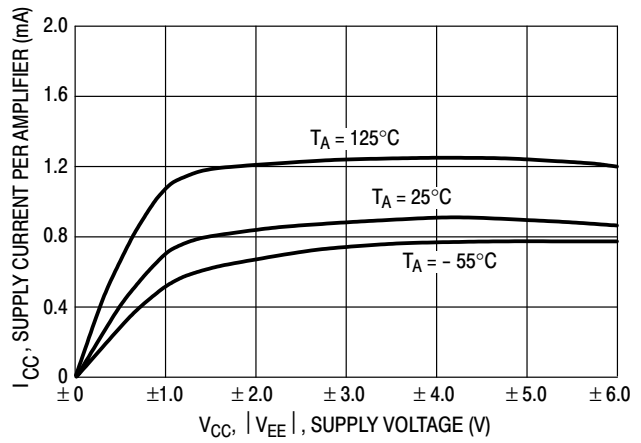


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

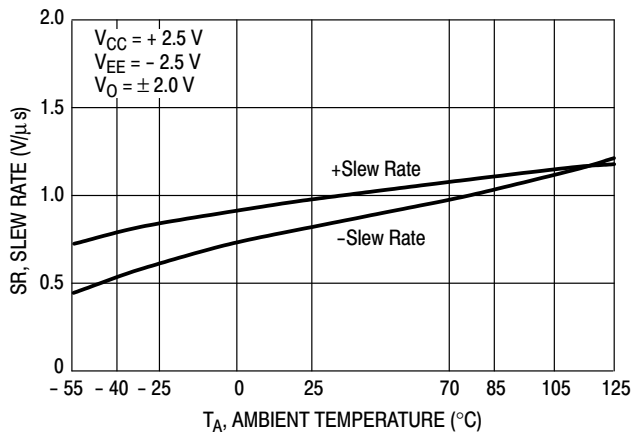


Figure 16. Slew Rate versus Temperature

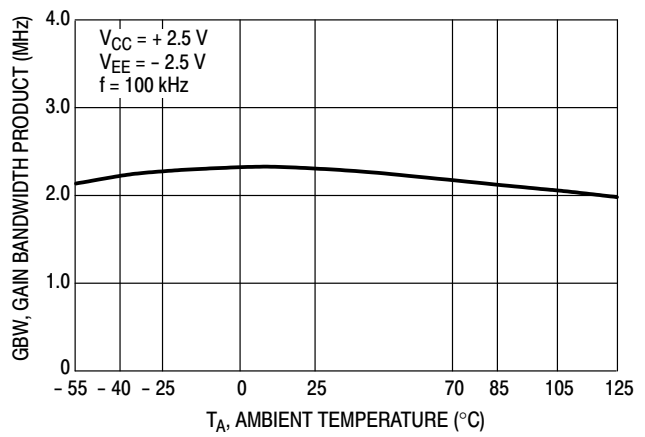


Figure 17. Gain Bandwidth Product versus Temperature

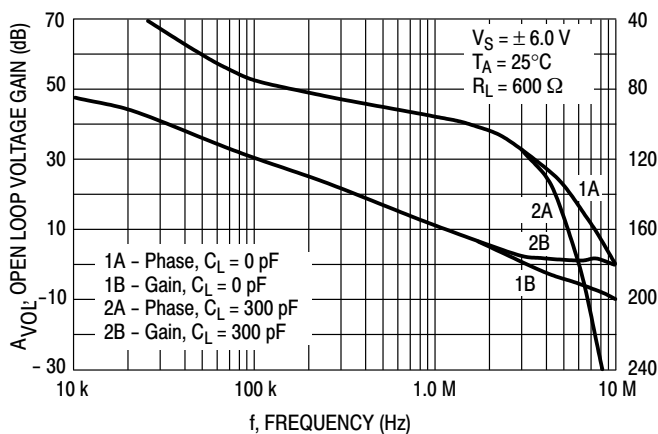


Figure 18. Voltage Gain and Phase versus Frequency

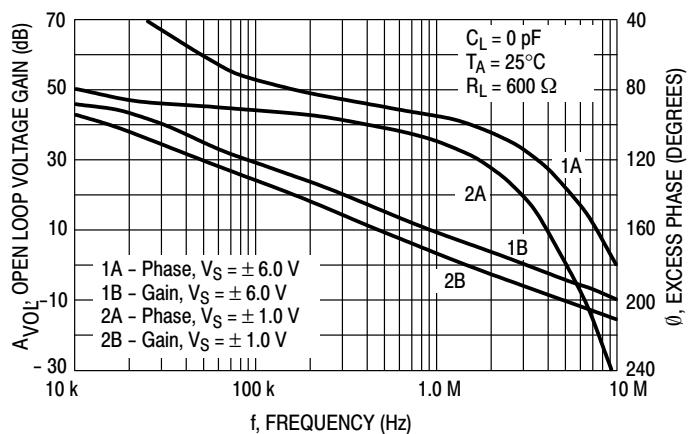


Figure 19. Voltage Gain and Phase versus Frequency

MC33201, MC33202, MC33204, NCV33202, NCV33204

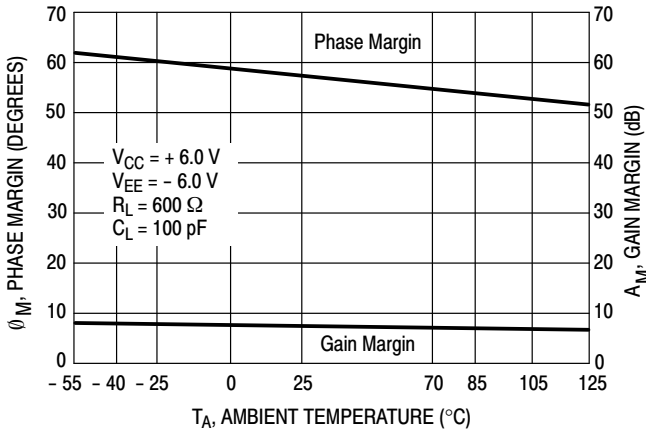


Figure 20. Gain and Phase Margin versus Temperature

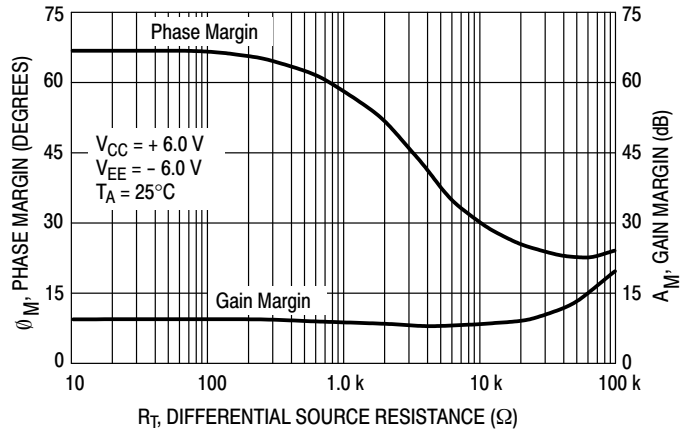


Figure 21. Gain and Phase Margin versus Differential Source Resistance

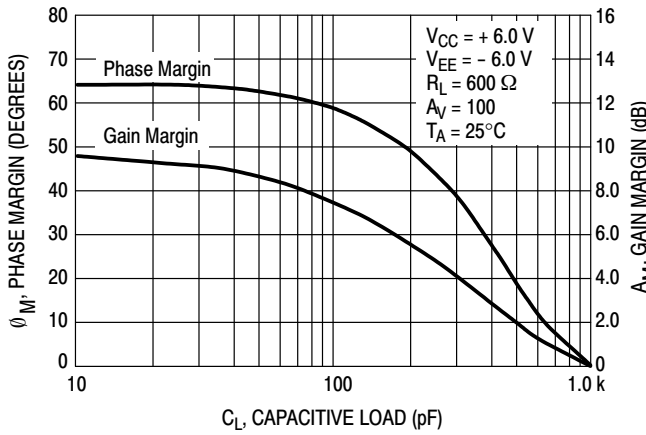


Figure 22. Gain and Phase Margin versus Capacitive Load

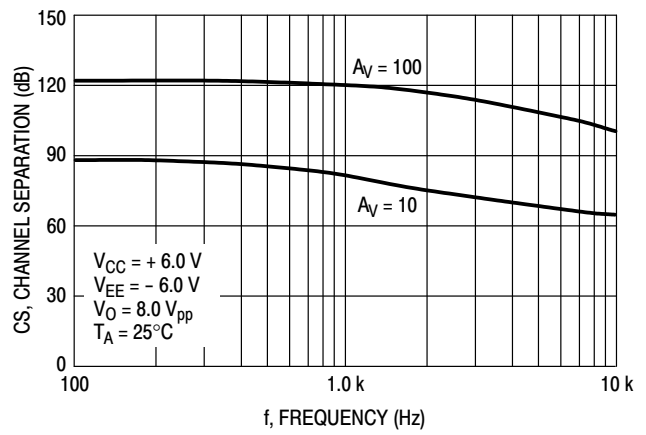


Figure 23. Channel Separation versus Frequency

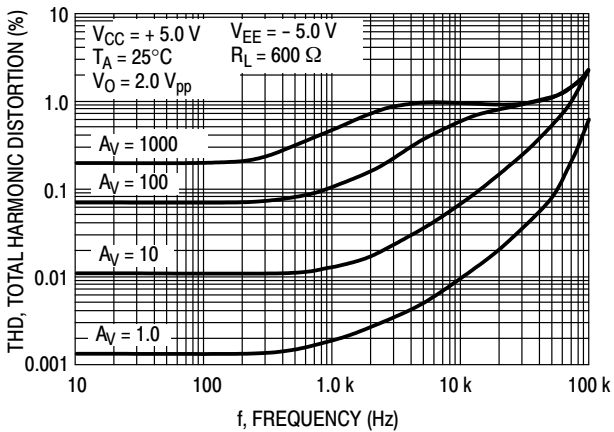


Figure 24. Total Harmonic Distortion versus Frequency

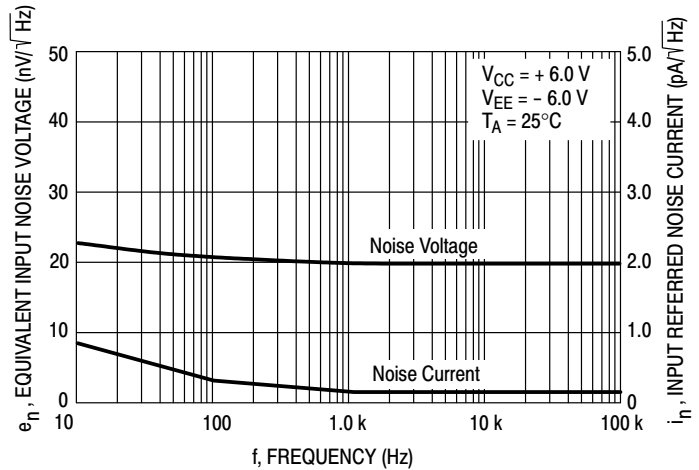


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency

DETAILED OPERATING DESCRIPTION

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE} , it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE} , the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

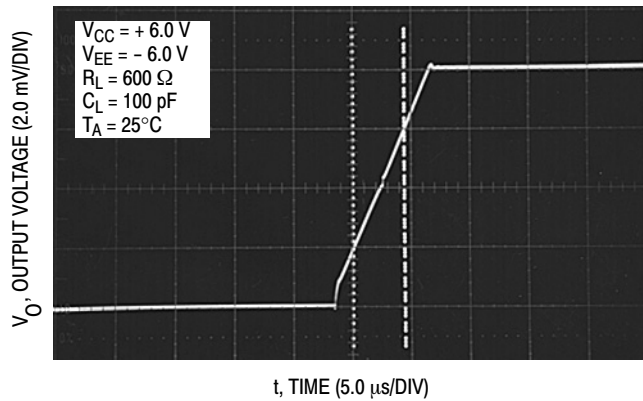


Figure 26. Noninverting Amplifier Slew Rate

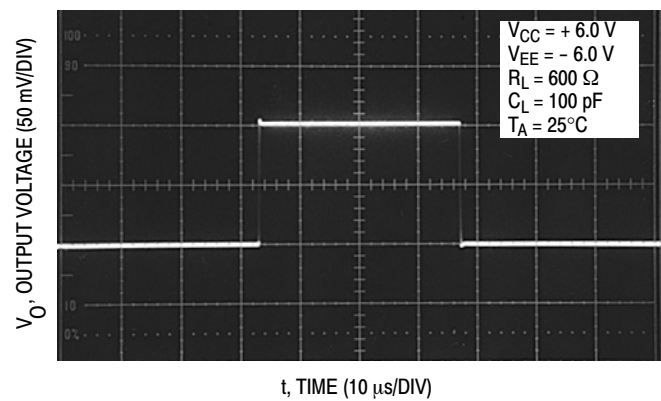


Figure 27. Small Signal Transient Response

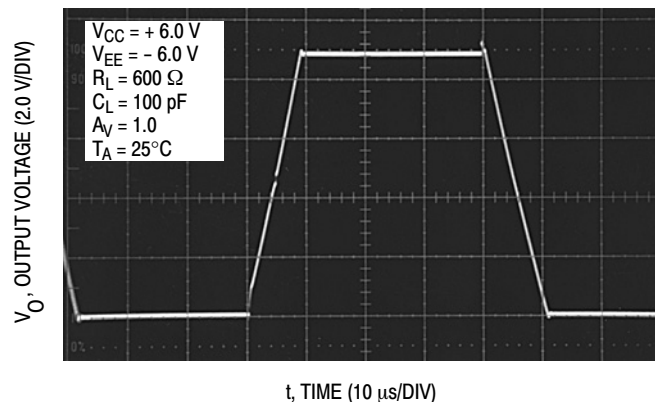


Figure 28. Large Signal Transient Response

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface

between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.

MC33201, MC33202, MC33204, NCV33202, NCV33204

ORDERING INFORMATION

| Operational Amplifier Function | Device | Operating Temperature Range | Package | Shipping† |
|--------------------------------|---------------------|---|----------------------|--------------------|
| Single | MC33201DG | $T_A = -40^\circ \text{ to } +105^\circ \text{C}$ | SOIC-8 (Pb-Free) | 98 Units / Rail |
| | MC33201DR2G | | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| | MC33201P | | PDIP-8 | 50 Units / Rail |
| | MC33201PG | | PDIP-8 (Pb-Free) | |
| | MC33201VDR2G | | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| | MC33201VDG | $T_A = -55^\circ \text{ to } 125^\circ \text{C}$ | SOIC-8 (Pb-Free) | 98 Units / Rail |
| Dual | MC33202DG | $T_A = -40^\circ \text{ to } +105^\circ \text{C}$ | SOIC-8 (Pb-Free) | |
| | MC33202DR2G | | SOIC-8 (Pb-Free) | |
| | MC33202DMR2G | | Micro-8 (Pb-Free) | 4000 / Tape & Reel |
| | NCV33202DMR2G* | | | |
| | MC33202P | | PDIP-8 | 50 Units / Rail |
| | MC33202PG | PDIP-8 (Pb-Free) | | |
| | MC33202VDG | $T_A = -55^\circ \text{ to } 125^\circ \text{C}$ | SOIC-8 (Pb-Free) | 98 Units / Rail |
| | MC33202VDR2G | | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| | NCV33202VDR2G* | | SOIC-8 (Pb-Free) | |
| | MC33202VP | | PDIP-8 | 50 Units / Rail |
| MC33202VPG | PDIP-8 (Pb-Free) | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*All NCV devices are qualified for automotive use.

MC33201, MC33202, MC33204, NCV33202, NCV33204

ORDERING INFORMATION (continued)

| Operational Amplifier Function | Device | Operating Temperature Range | Package | Shipping† |
|--------------------------------|------------------|---|----------------------|--------------------------|
| Quad | MC33204DG | $T_A = -40^\circ$ to $+105^\circ\text{C}$ | SO-14 (Pb-Free) | 55 Units / Rail |
| | MC33204DR2G | | SO-14 (Pb-Free) | 2500 Units / Tape & Reel |
| | MC33204DTBG | | TSSOP-14* | 96 Units / Rail |
| | MC33204DTBR2G | | TSSOP-14* | 2500 Units / Tape & Reel |
| | MC33204PG | | PDIP-14 (Pb-Free) | 25 Units / Rail |
| | MC33204VDG | $T_A = -55^\circ$ to 125°C | SO-14 (Pb-Free) | 55 Units / Rail |
| | MC33204VDR2G | | SO-14 (Pb-Free) | 2500 Units / Tape & Reel |
| | NCV33204DR2G** | | SO-14 (Pb-Free) | |
| | NCV33204DTBR2G** | | TSSOP-14* | |
| | MC33204VPG | | PDIP-14 (Pb-Free) | 25 Units / Rail |

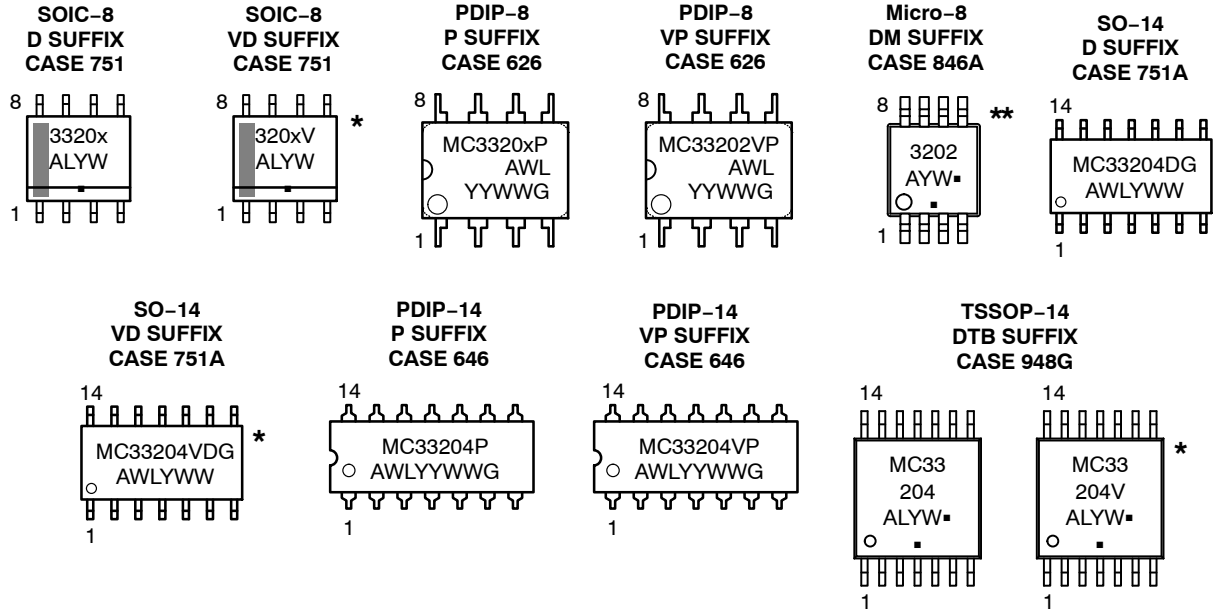
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

**NCV33202 and NCV33204 are qualified for automotive use.

MC33201, MC33202, MC33204, NCV33202, NCV33204

MARKING DIAGRAMS



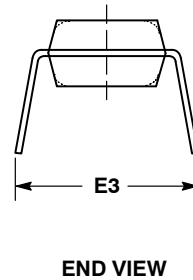
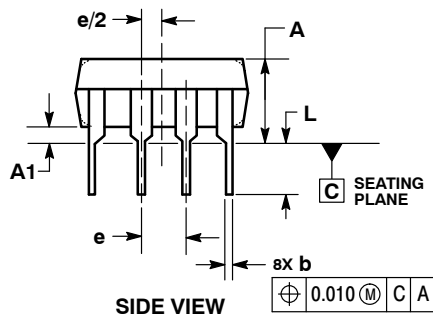
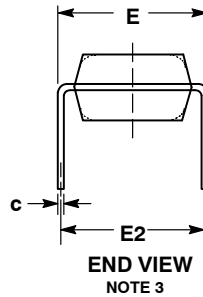
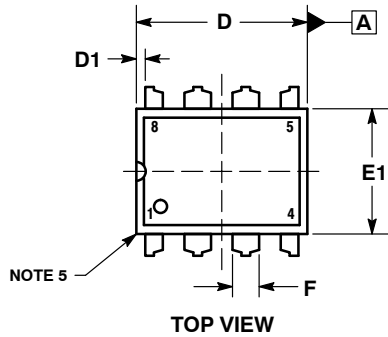
x = 1 or 2
 A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package
 • = Pb-Free Package
 (Note: Microdot may be in either location)

*This marking diagram applies to NCV3320xV

**This marking diagram applies to NCV33202DMR2G

PACKAGE DIMENSIONS

PDIP-8
P, VP SUFFIX
CASE 626-05
ISSUE M



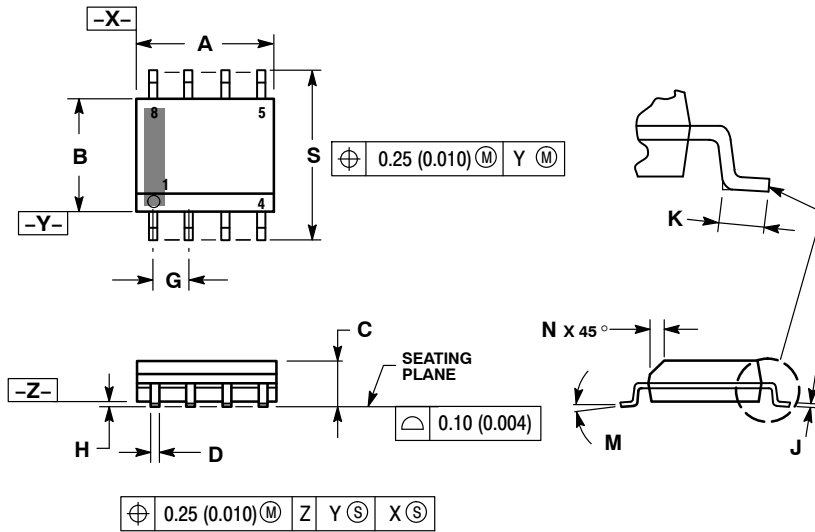
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION E IS MEASURED WITH THE LEADS RESTRAINED PARALLEL AT WIDTH E2.
4. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | | MILLIMETERS | | |
|-----|-----------|-------|-------|-------------|------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | ---- | ---- | 0.210 | ---- | ---- | 5.33 |
| A1 | 0.015 | ---- | ---- | 0.38 | ---- | ---- |
| b | 0.014 | 0.018 | 0.022 | 0.35 | 0.46 | 0.56 |
| C | 0.008 | 0.010 | 0.014 | 0.20 | 0.25 | 0.36 |
| D | 0.355 | 0.365 | 0.400 | 9.02 | 9.27 | 10.02 |
| D1 | 0.005 | ---- | ---- | 0.13 | ---- | ---- |
| E | 0.300 | 0.310 | 0.325 | 7.62 | 7.87 | 8.26 |
| E1 | 0.240 | 0.250 | 0.280 | 6.10 | 6.35 | 7.11 |
| E2 | 0.300 BSC | | | 7.62 BSC | | |
| E3 | ---- | ---- | 0.430 | ---- | ---- | 10.92 |
| e | 0.100 BSC | | | 2.54 BSC | | |
| L | 0.115 | 0.130 | 0.150 | 2.92 | 3.30 | 3.81 |

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

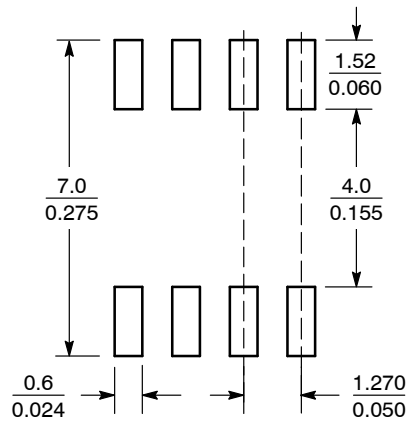


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*

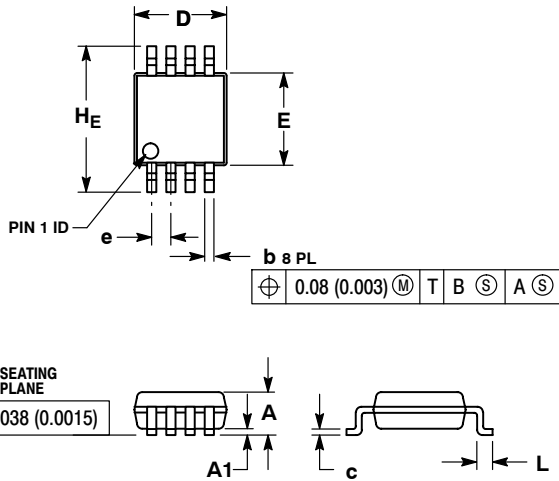


SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

Micro8
DM SUFFIX
CASE 846A-02
ISSUE H

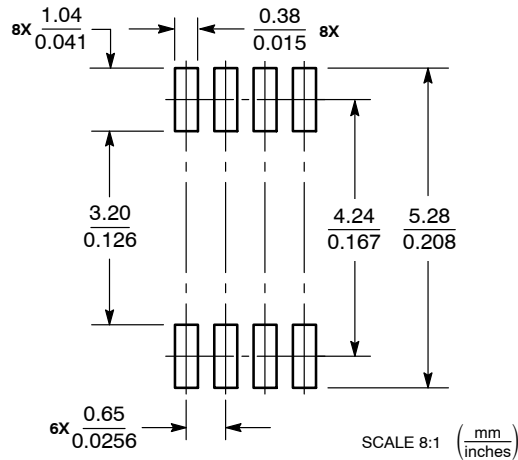


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.10 | --- | --- | 0.043 |
| A1 | 0.05 | 0.08 | 0.15 | 0.002 | 0.003 | 0.006 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.013 | 0.016 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.021 | 0.028 |
| HE | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |

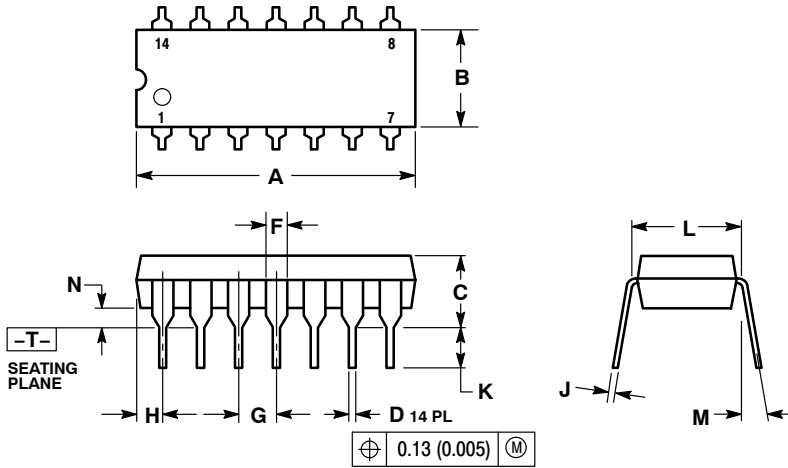
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



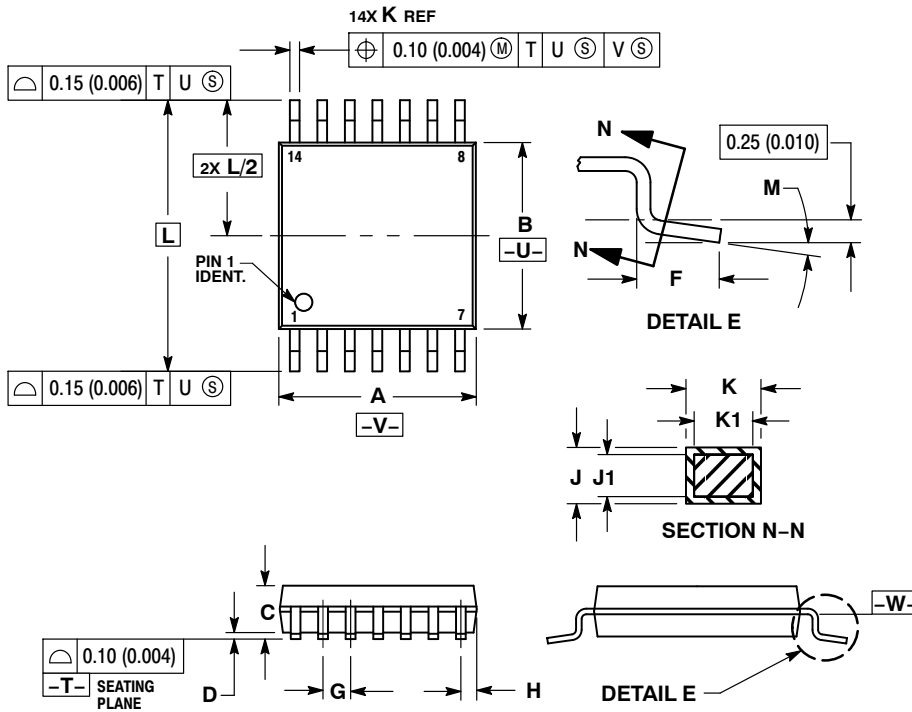
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

PACKAGE DIMENSIONS

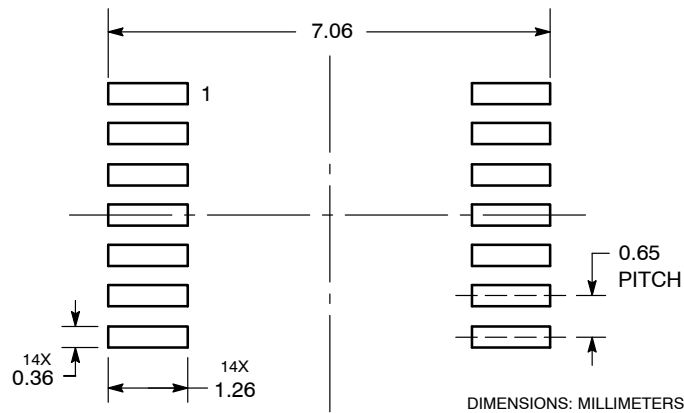
TSSOP-14
CASE 948G-01
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

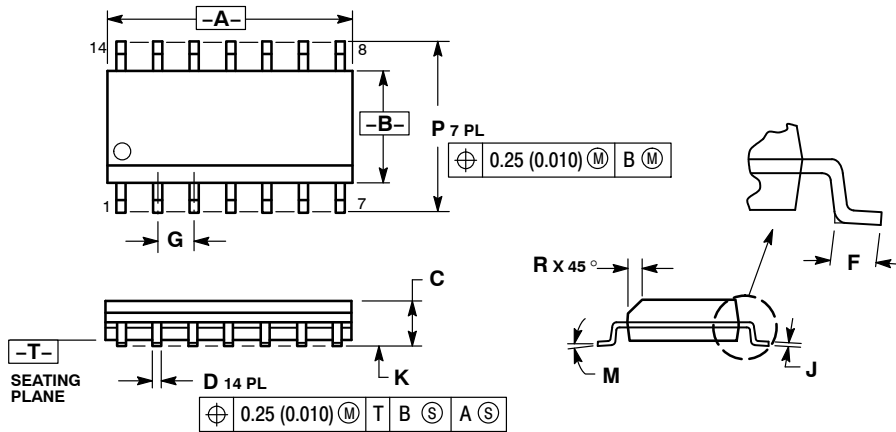


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC33201, MC33202, MC33204, NCV33202, NCV33204

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE J

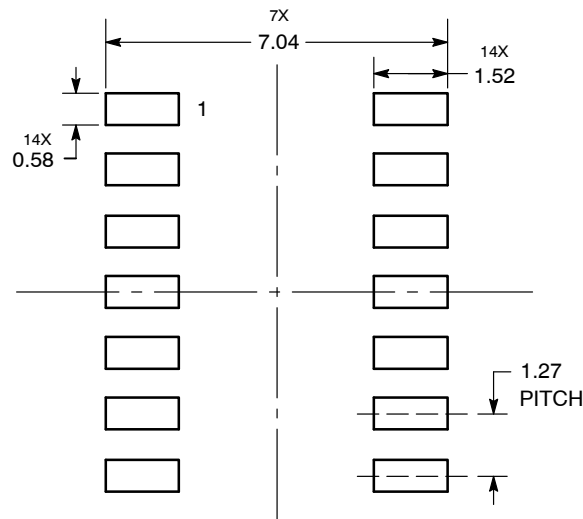


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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