

NLAS1053

2:1 Mux/Demux Analog Switches

The NLAS1053 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. The device consists of a single 2:1 Mux/Demux (SPDT), similar to ON Semiconductor's NLAS4053 analog and digital voltages that may vary across the full power supply range (from V_{CC} to GND).

The inhibit and select input pins have over voltage protection that allows voltages above V_{CC} up to 7.0 V to be present without damage or disruption of operation of the part, regardless of the operating voltage.

Features

- High Speed: $t_{PD} = 1$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- High Bandwidth, Improved Linearity, and Low $R_{DS(ON)}$
- INH Pin Allows a Both Channels 'OFF' Condition (With a High)
- $R_{DS(ON)} \cong 25 \Omega$, Performance Very Similar to the NLAS4053
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Useful For Switching Video Frequencies Beyond 70 MHz
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V
- Tiny US8 Package, Only 2.1 X 3.0 mm
- Pb-Free Package is Available

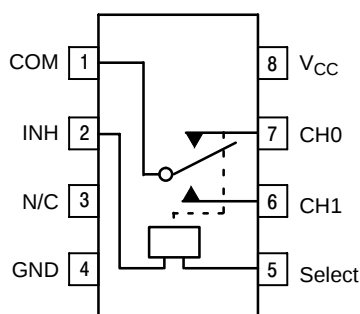


Figure 1. Pin Assignment



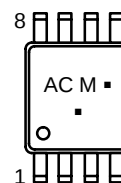
ON Semiconductor®

<http://onsemi.com>



US8
US SUFFIX
CASE 493-01

MARKING DIAGRAMS



AC = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NLAS1053US	US8	3000 / Tape & Reel
NLAS1053USG	US8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FUNCTION TABLE

INH	Select	Ch 0	Ch 1
H	X	OFF	OFF
L	L	ON	OFF
L	H	OFF	ON

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Positive DC Supply Voltage	V_{CC}	-0.5 to +7.0	V
Digital Input Voltage (Select and Inhibit)	V_{IN}	$-0.5 \leq V \leq +7.0$	V
Analog Output Voltage (V_{CH} or V_{COM})	V_{IS}	$-0.5 \leq V \leq V_{CC} + 0.5$	V
DC Current, Into or Out of Any Pin	I_{IK}	50	mA
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds	T_L	260	°C
Junction Temperature under Bias	T_J	+150	°C
Thermal Resistance	θ_{JA}	250	°C/W
Power Dissipation in Still Air at 85°C	P_D	250	mW
Moisture Sensitivity	MSL	Level 1	
Flammability Rating	Oxygen Index: 30% – 35% F_R	UL 94 V-0 @ 0.125 in	
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) V_{ESD}	> 2000 200 N/A	V
Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5) $I_{Latchup}$	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Positive DC Supply Voltage	V_{CC}	2.0	5.5	V
Digital Input Voltage (Select and Inhibit)	V_{IN}	GND	5.5	V
Static or Dynamic Voltage Across an Off Switch	V_{IO}	GND	V_{CC}	V
Analog Input Voltage (CH, COM)	V_{IS}	GND	V_{CC}	V
Operating Temperature Range, All Package Types	T_A	-55	+125	°C
Input Rise or Fall Time (Enable Input)	t_r, t_f	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		ns/V
		0	100	
		0	20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

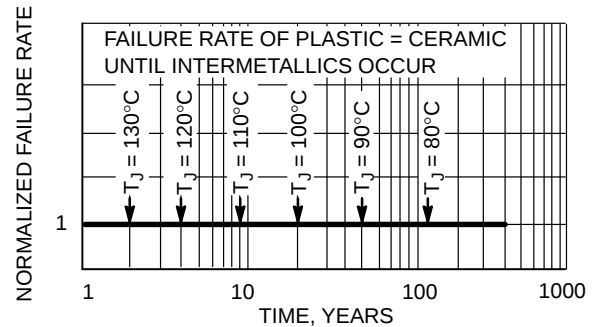


Figure 2. Failure Rate versus Time Junction Temperature

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V _{CC}	Guaranteed Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
Minimum High-Level Input Voltage, Select and Inhibit Inputs		V _{IH}	2.0	1.5	1.5	1.5	V
			2.5	1.9	1.9	1.9	
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
Maximum Low-Level Input Voltage, Select and Inhibit Inputs		V _{IL}	2.0	0.5	0.5	0.5	V
			2.5	0.6	0.6	0.6	
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
Maximum Input Leakage Current, Select and Inhibit Inputs	V _{IN} = 5.5 V or GND	I _{IN}	0 V to 5.5 V	± 0.1	± 1.0	± 1.0	μA
Maximum Quiescent Supply Current	Select and Inhibit = V _{CC} or GND	I _{CC}	5.5	1.0	1.0	2.0	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Parameter	Condition	Symbol	V _{CC}	Guaranteed Limit			Unit
				–55 to 25°C	< 85°C	< 125°C	
Maximum "ON" Resistance (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 10.0 mA	R _{ON}	2.5	70	85	105	Ω
			3.0	40	46	52	
			4.5	20	28	34	
			5.5	16	22	28	
ON Resistance Flatness (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{IS} = 1V, 2V, 3.5V	R _{FLAT} (ON)	4.5	4	4	5	Ω
ON Resistance Match Between Channels	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{CH1} or V _{CH0} = 3.5 V	ΔR _{ON} (ON)	4.5	2	2	3	Ω
CH1 or CH0 Off Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{CH1} or V _{CH0} = 1.0 V _{COM} 4.5 V	I _{CH0} I _{CH1}	5.5	1	10	100	nA
COM ON Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{CH1} 1.0 V or 4.5 V with V _{CH0} floating or V _{CH1} 1.0 V or 4.5 V with V _{CH1} floating V _{COM} = 1.0 V or 4.5 V	I _{COM(ON)}	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Parameter	Test Conditions	Symbol	V _{CC} (V)	Guaranteed Max Limit						Unit	
				-55 to 25°C			< 85°C		< 125°C		
				Min	Typ*	Max	Min	Max	Min		Max
Turn-On Time (Figures 12 and 13) INH to Output	R _L = 300 Ω, C _L = 35 pF (Figures 4 and 5)	t _{ON}	2.5	2	7	12	2	15	2	15	ns
			3.0	2	5	10	2	15	2	15	
			4.5	1	4	9	1	12	1	12	
			5.5	1	3	8	1	12	1	12	
Turn-Off Time (Figures 12 and 13) INH to Output	R _L = 300 Ω, C _L = 35 pF (Figures 4 and 5)	t _{OFF}	2.5	2	7	12	2	15	2	15	ns
			3.0	2	5	10	2	15	2	15	
			4.5	1	4	9	1	12	1	12	
			5.5	1	3	8	1	12	1	12	
Transition Time (Channel Selec- tion Time) (Figure) Select to Output	R _L = 300 Ω, C _L = 35 pF (Figures and)	t _{trans}	2.5	5	18	28	5	30	5	30	ns
			3.0	5	13	21	5	25	5	25	
			4.5	2	12	16	2	20	2	20	
			5.5	2	9	14	2	20	2	20	
Minimum Break-Before-Make Time	V _{IS} = 3.0 V (Figure 3) R _L = 300 Ω, C _L = 35 pF	t _{BBM}	2.5	1	12		1		1		ns
			3.0	1	11		1		1		
			4.5	1	6		1		1		
			5.5	1	5		1		1		
			Typical @ 25, V _{CC} = 5.0 V								
Maximum Input Capacitance, Select/INH Input		C _{IN} C _{NO} or C _{NC} C _{COM} C _(ON)	8								pF
Analog I/O (switch off)			10								
Common I/O (switch off)			10								
Feedthrough (switch on)			20								

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Parameter	Condition	Symbol	V _{CC} (V)	Typical	Unit
				25°C	
Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 10)	V _{IN} = 0 dBm V _{IN} centered between V _{CC} and GND (Figure 7)	BW	3.0 4.5 5.5	170 200 200	MHz
Maximum Feedthrough On Loss	V _{IN} = 0 dBm @ 100 kHz to 50 MHz V _{IN} centered between V _{CC} and GND (Figure 7)	V _{ONL}	3.0 4.5 5.5	-3 -3 -3	dB
Off-Channel Isolation (Figure 10)	f = 100 kHz; V _{IS} = 1 V RMS V _{IN} centered between V _{CC} and GND (Figure 7)	V _{ISO}	3.0 4.5 5.5	-93 -93 -93	dB
Charge Injection Select Input to Common I/O (Figure 15)	V _{IN} = V _{CC} to GND, F _{IS} = 20 kHz t _r = t _f = 3 ns R _{IS} = 0 Ω, C _L = 1000 pF Q = C _L * ΔV _{OUT} (Figure 8)	Q	3.0 5.5	1.5 3.0	pC
Total Harmonic Distortion THD + Noise (Figure 14)	F _{IS} = 20 Hz to 100 kHz, R _L = R _{gen} = 600 Ω C _L = 50 pF V _{IS} = 5.0 V _{PP} sine wave	THD	5.5	0.1	%

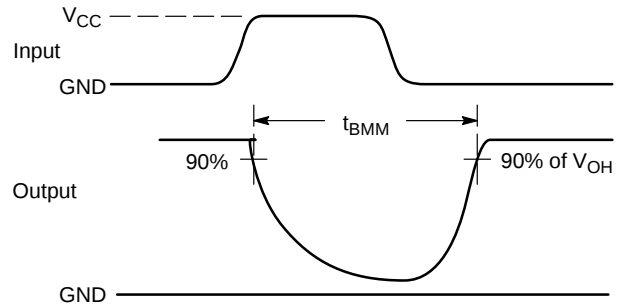
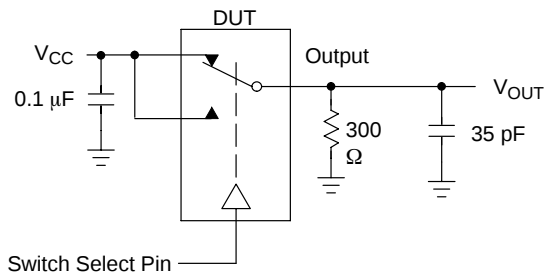


Figure 3. t_{BMM} (Time Break-Before-Make)

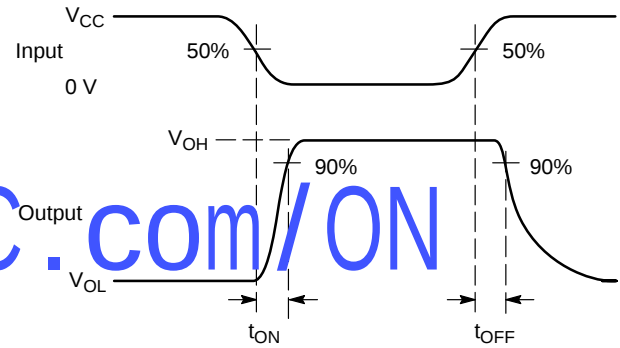
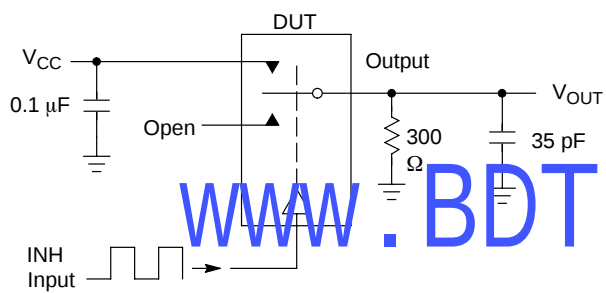


Figure 4. t_{ON}/t_{OFF}

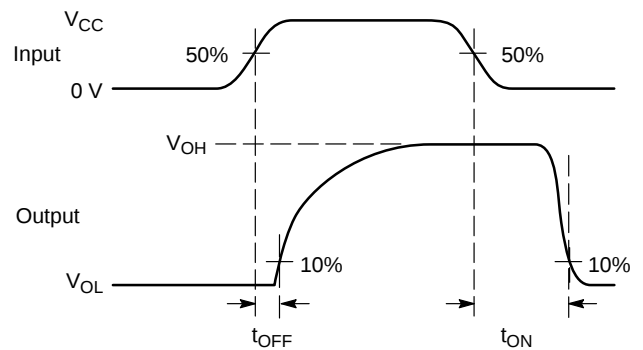
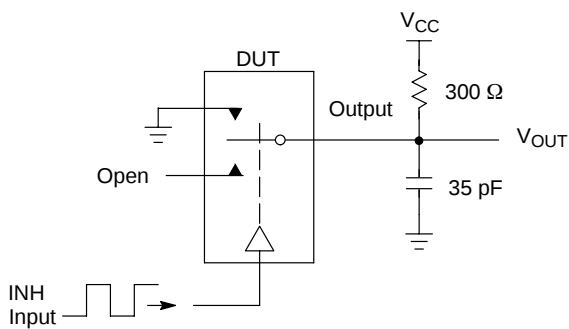


Figure 5. t_{ON}/t_{OFF}

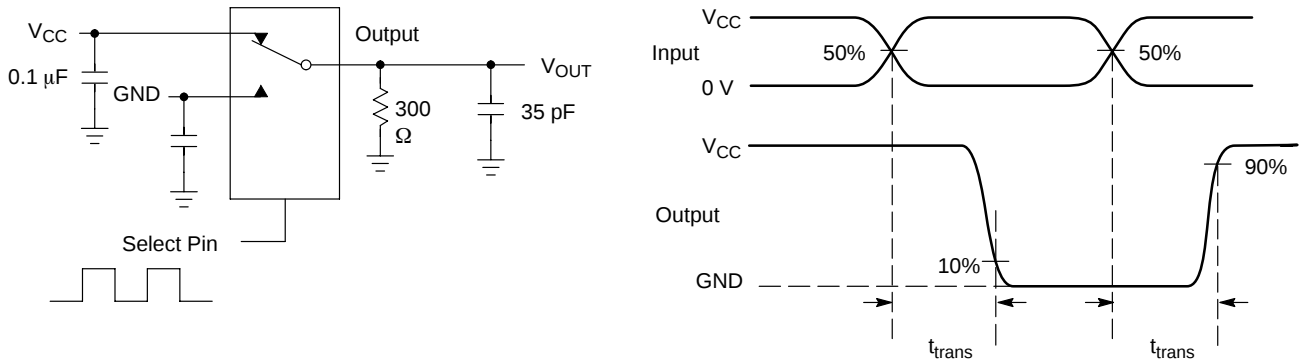
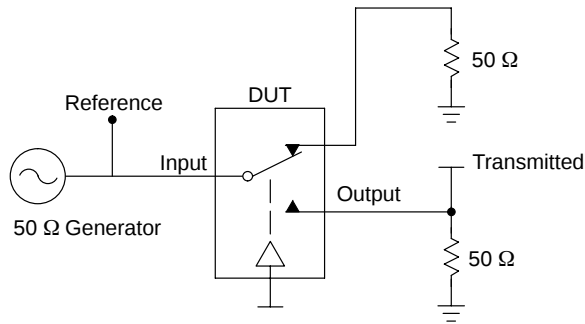


Figure 6. t_{trans} (Channel Selection Time)



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \log \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \log \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

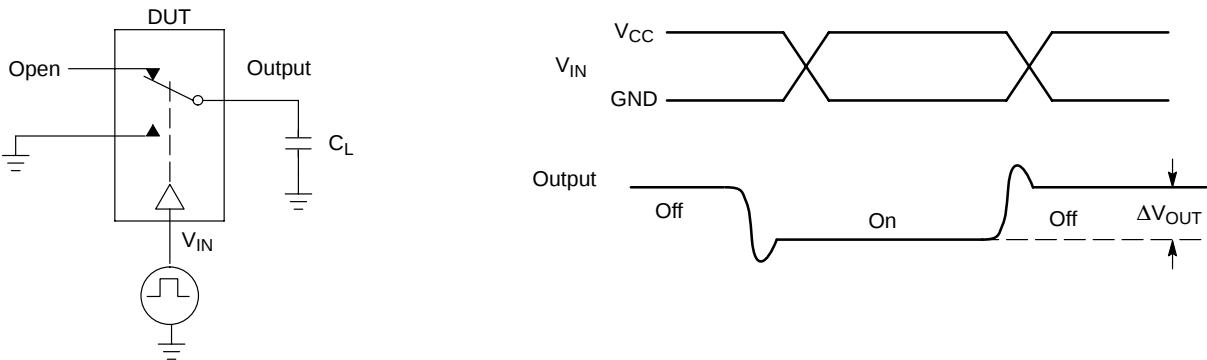


Figure 8. Charge Injection: (Q)

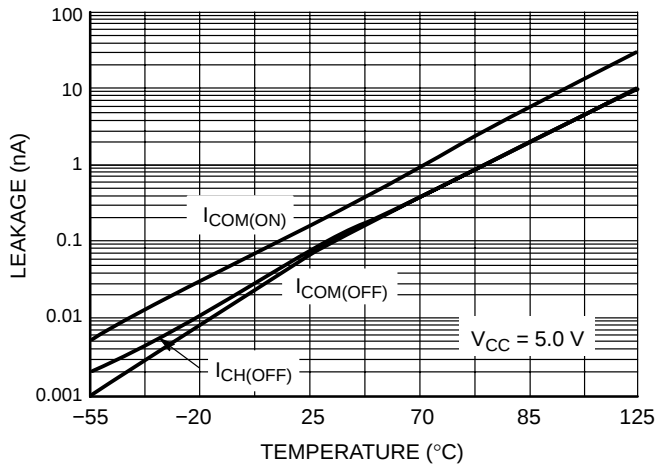


Figure 9. Switch Leakage versus Temperature

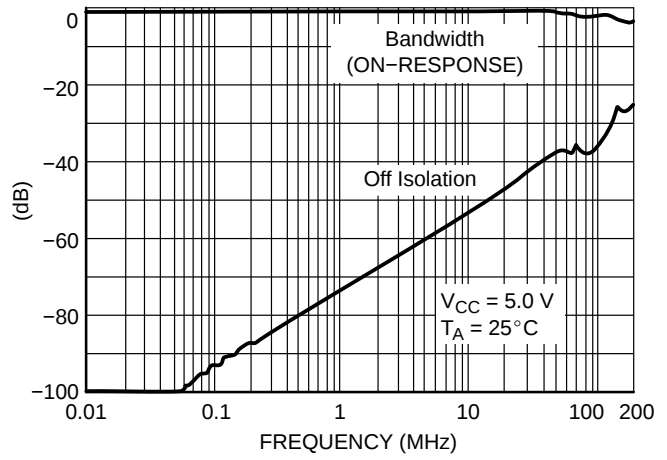


Figure 10. Bandwidth and Off-Channel Isolation

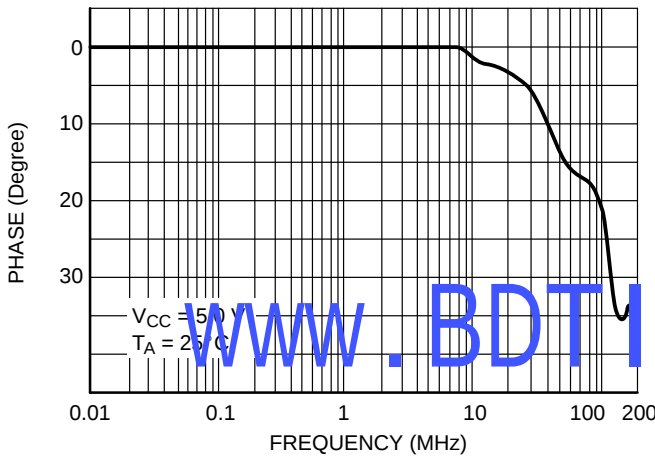


Figure 11. Phase versus Frequency

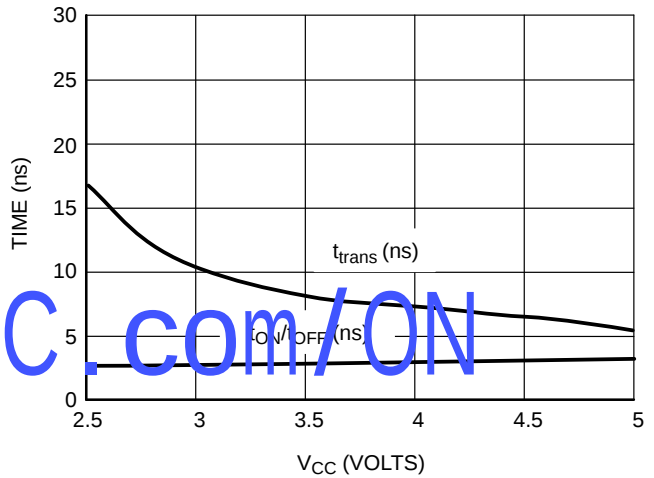


Figure 12. t_{ON} and t_{OFF} versus V_{CC} at 25°C

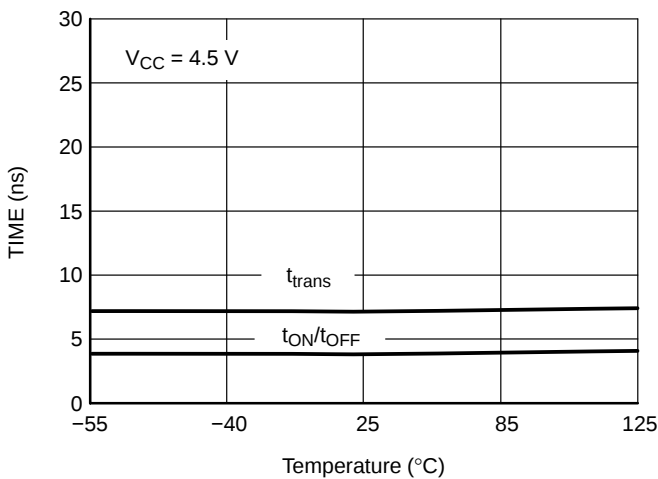


Figure 13. t_{ON} and t_{OFF} versus Temp

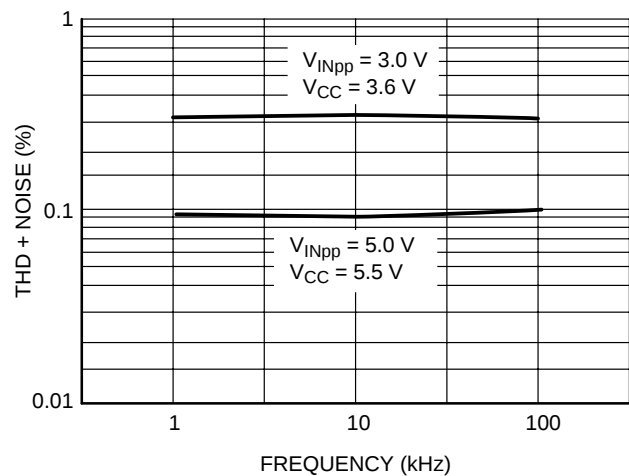


Figure 14. Total Harmonic Distortion Plus Noise versus Frequency

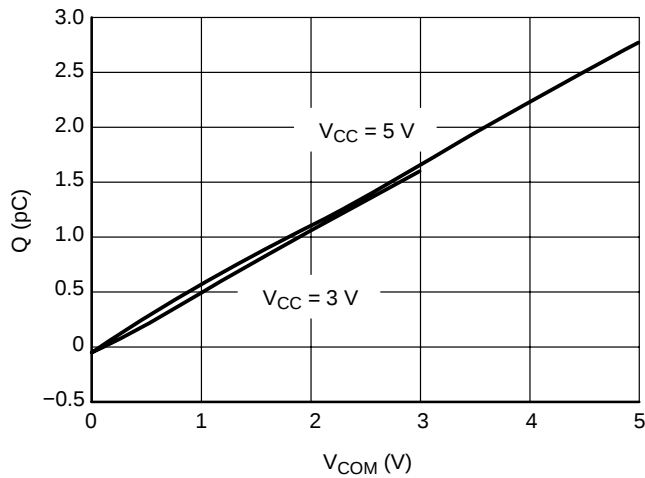


Figure 15. Charge Injection versus COM Voltage

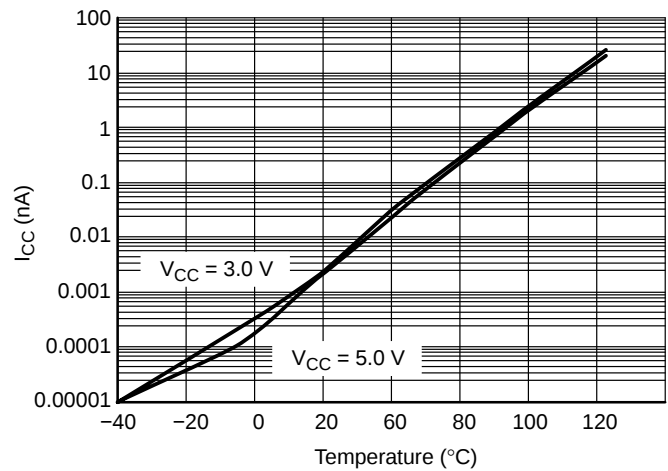


Figure 16. I_{CC} versus Temp, $V_{CC} = 3\text{ V}$ & 5 V

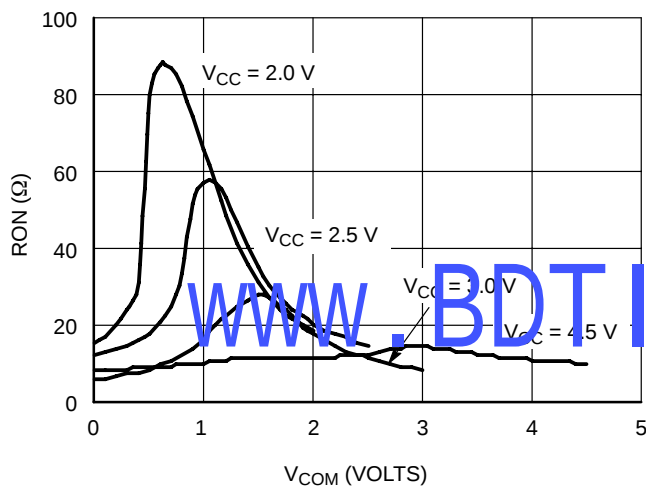


Figure 17. R_{ON} versus V_{COM} and V_{CC} (@ 25°C)

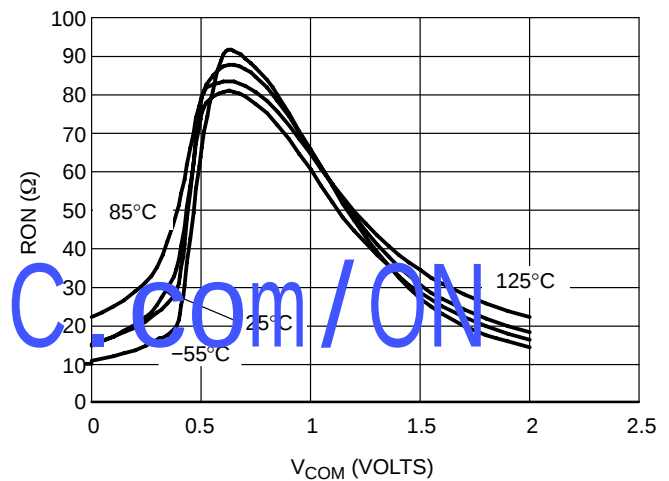


Figure 18. R_{ON} versus V_{COM} and Temperature, $V_{CC} 2.0\text{ V}$

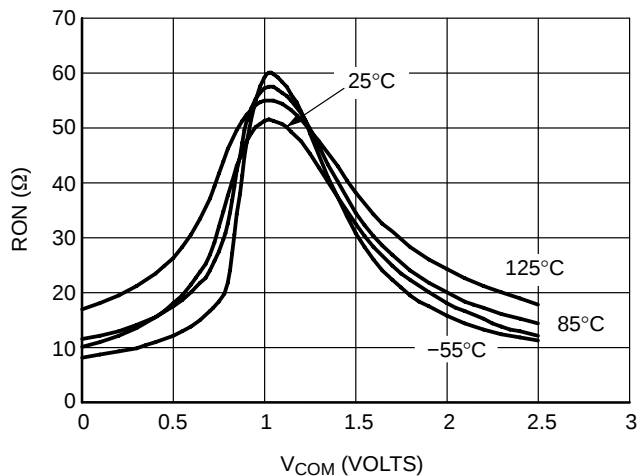


Figure 19. R_{ON} versus V_{COM} and Temperature, $V_{CC} = 2.5\text{ V}$

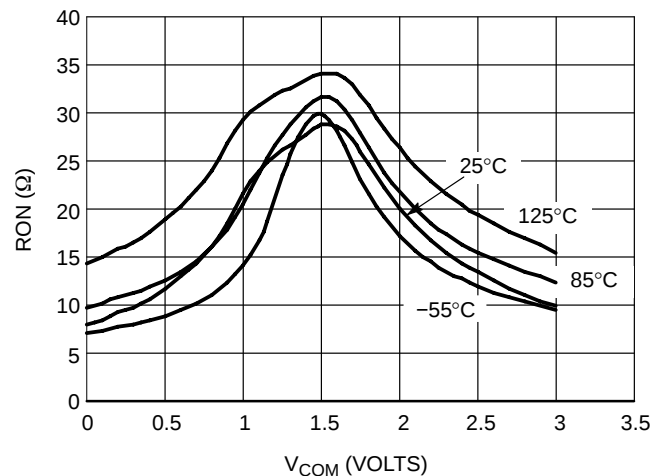


Figure 20. R_{ON} versus V_{COM} and Temperature, $V_{CC} = 3.0\text{ V}$

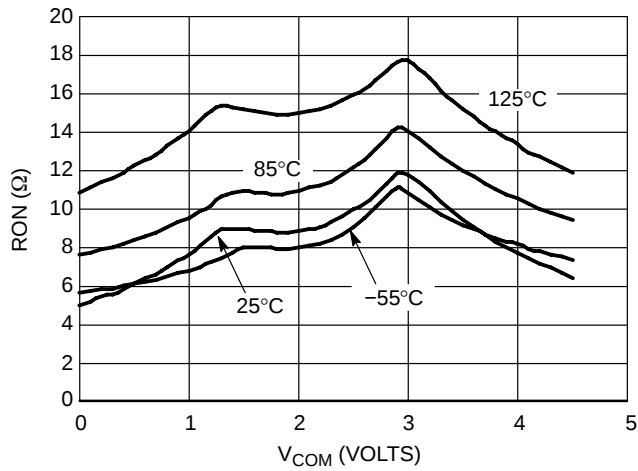


Figure 21. R_{ON} versus V_{COM} and Temperature, $V_{CC} = 4.5$ V

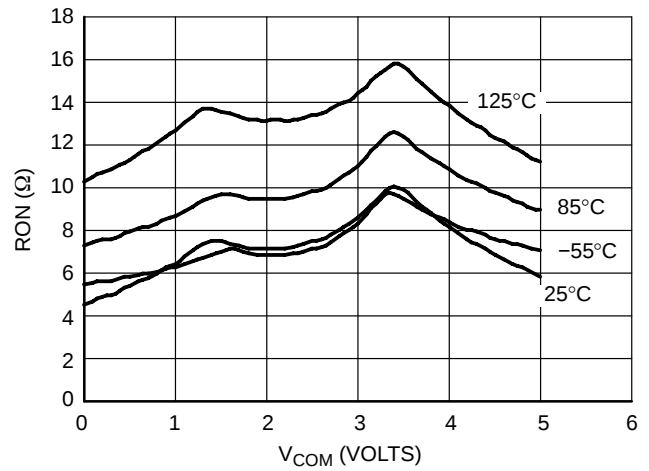


Figure 22. R_{ON} versus V_{COM} and Temperature, $V_{CC} = 5.0$ V

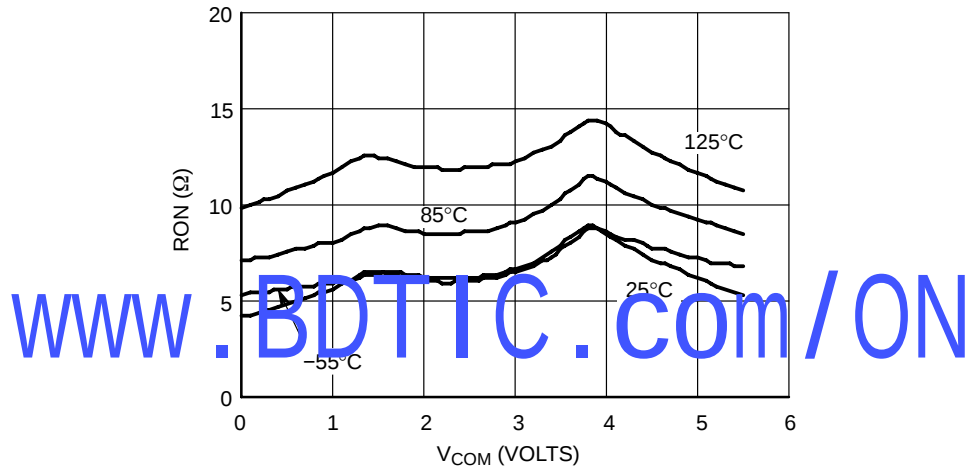
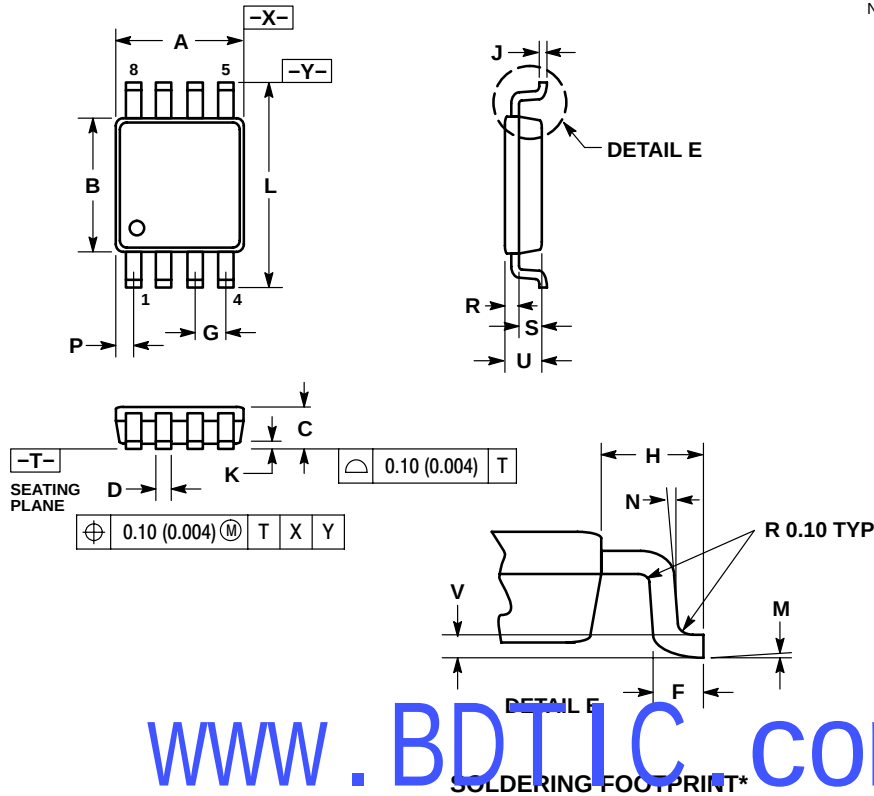


Figure 23. R_{ON} versus V_{COM} and Temperature, $V_{CC} = 5.5$ V

NLAS1053

PACKAGE DIMENSIONS

US8
CASE 493-02
ISSUE B



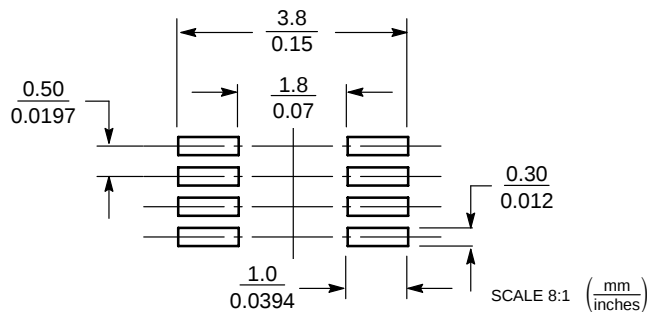
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 ").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0°	6°	0°	6°
N	5°	10°	5°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.15 BSC		0.005 BSC	

www.BDTIC.com/ON

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative