

# NLAS4157

## SPDT, 1 $\Omega$ $R_{ON}$ Switch

The NLAS4157 is a low  $R_{ON}$  SPDT analog switch. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS4157 can handle a balanced microphone/speaker/ringtone generator in a monophone mode. The device contains a break-before-make (BBM) feature.

### Features

- Single Supply Operation:
  - 1.65 V to 5.5 V  $V_{CC}$
  - Function Directly from LiON Battery
- Tiny SC88 6-Pin Pb-Free Package:
  - Meets JEDEC MO-220 Specifications
- $R_{ON}$  Typical = 0.8  $\Omega$  @  $V_{CC} = 4.5$  V
- Low Static Power
- This is a Pb-Free Device

### Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Stereo Balanced (Push-Pull) Switching

### Important Information

- Ringtone-Chip/Amplifier Switching
- Continuous Current Rating Through each Switch  $\pm 300$  mA
- Conforms to: JEDEC MO-220, Issue H, Variation VEED-6
- Pin for Pin Compatible with FSA4157



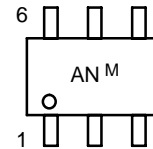
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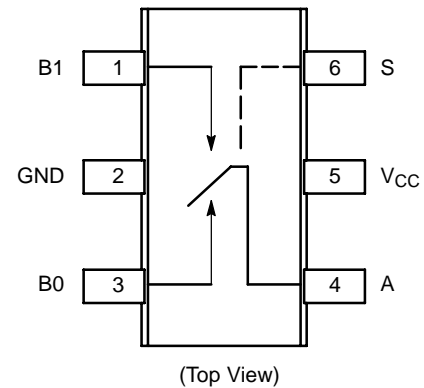
SC-88 (SOT-363)  
CASE 419B

### MARKING DIAGRAM



AN = Specific Device Code  
M = Date Code

### PIN ASSIGNMENTS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.7 4.5				2.0 2.4		V
V <sub>IL</sub>	LOW Level Input Voltage		2.7 4.5					0.6 0.8	V
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0-5.5			±0.1		±1	μA
I <sub>OFF</sub>	OFF State Leakage Current (Note 7)	0 ≤ A, B ≤ V <sub>CC</sub>	5.5	-2.0		+2.0		±20	nA
I <sub>ON</sub>	ON State Leakage Current (Note 7)	0 ≤ A, B ≤ V <sub>CC</sub>	5.5	-4.0		+4.0		±40	nA
R <sub>ON</sub>	Switch On Resistance (Note 2)	I <sub>O</sub> = -100 mA, B <sub>0</sub> or B <sub>1</sub> = 3.5 V	2.7		2.0	4.0		4.3	Ω
		I <sub>O</sub> = -100 mA, B <sub>0</sub> or B <sub>1</sub> = 1.5 V	4.5		0.8	1.15		1.3	
I <sub>CC</sub>	Quiescent Supply Current All Channels ON or OFF	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			0.5		1.0	μA

Analog Signal Range

ΔR <sub>ON</sub>	On Resistance Match Between Channels (Notes 2, 3, 4)	I <sub>A</sub> = -100 mA, B <sub>0</sub> or B <sub>1</sub> = 1.5 V	2.7		0.15				Ω
		I <sub>A</sub> = -100 mA, B <sub>0</sub> or B <sub>1</sub> = 3.5 V	4.5		0.12			0.15	
R <sub>flat</sub>	On Resistance Flatness (Notes 2, 3, 5)	I <sub>A</sub> = -100 mA, B <sub>0</sub> or B <sub>1</sub> = 0 V, 0.75 V, 1.5 V	2.7		1.4				Ω
		I <sub>A</sub> = -100 mA, B <sub>0</sub> or B <sub>1</sub> = 0 V, 1.0 V, 2.0 V	4.5		0.3			0.4	

2. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
3. Parameter is characterized but not tested in production.
4. ΔR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> min measured at identical V<sub>CC</sub>, temperature and voltage levels.
5. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
6. Guaranteed by Design.
7. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Unit	Figure #
				Min	Typ	Max	Min	Max		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Bus-to-Bus (Note 9)	V <sub>I</sub> = OPEN	2.7 4.5			2.0 0.3			ns	3, 4
t <sub>ON</sub>	Output Enable Time Turn On Time (A to B <sub>n</sub> )	B <sub>0</sub> or B <sub>1</sub> = 1.5 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF B <sub>0</sub> or B <sub>1</sub> = 3.0 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	2.7 4.5			30 20		35 25	ns	3, 4
t <sub>OFF</sub>	Output Disable Time Turn Off Time (A Port to B Port)	B <sub>0</sub> or B <sub>1</sub> = 1.5V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF B <sub>0</sub> or B <sub>1</sub> = 3.0 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	2.7 4.5			20 15		25 20	ns	3, 4
t <sub>BBM</sub>	Break Before Make Time (Note 8)		2.7 4.5	0.5 0.5			0.5 0.5		ns	2
Q	Charge Injection (Note 8)	C <sub>L</sub> = 1.0 nF, V <sub>GEN</sub> = 0 V R <sub>GEN</sub> = 0 Ω	2.7 4.5		26 48				pC	6
O <sub>IRR</sub>	Off Isolation (Note 10)	R <sub>L</sub> = 50 Ω f = 1.0 MHz	2.7 – 5.5		-52				dB	5
X <sub>talk</sub>	Crosstalk	R <sub>L</sub> = 50 Ω f = 1.0 MHz	2.7 – 5.5		-57				dB	7
BW	-3 dB Bandwidth	R <sub>L</sub> = 50 Ω	2.7 – 5.5		40				MHz	8
THD	Total Harmonic Distortion (Note 8)	R <sub>L</sub> = 600 Ω 0.5 V <sub>P-P</sub> f = 20 Hz to 20 kHz	2.7 – 5.5		0.012				%	9

8. Guaranteed by Design.

9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

10. Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub>/V<sub>Bn</sub>].

## CAPACITANCE (Note 11)

Symbol	Parameter	Test Conditions	Typ	Max	Unit	Figure #
C <sub>IN</sub>	Select Pin Input Capacitance	V <sub>CC</sub> = 0 V, f = 1 MHz	10		pF	
C <sub>IO-B</sub>	B Port Off Capacitance	V <sub>CC</sub> = 4.5 V, f = 1 MHz	25		pF	
C <sub>IOA-ON</sub>	A Port Capacitance when Switch is Enabled	V <sub>CC</sub> = 4.5 V, f = 1 MHz	87		pF	

11. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

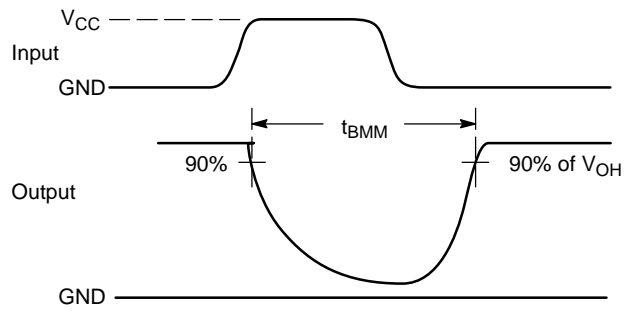
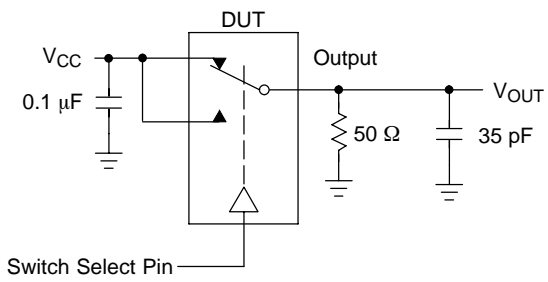
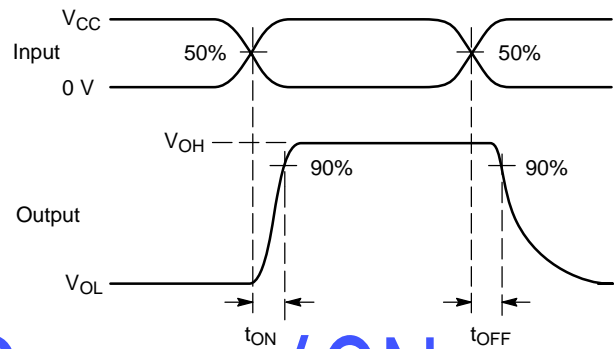
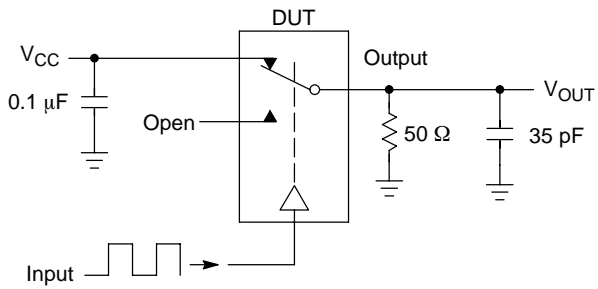


Figure 2.  $t_{BMM}$  (Time Break-Before-Make)



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Figure 3.  $t_{ON}/t_{OFF}$

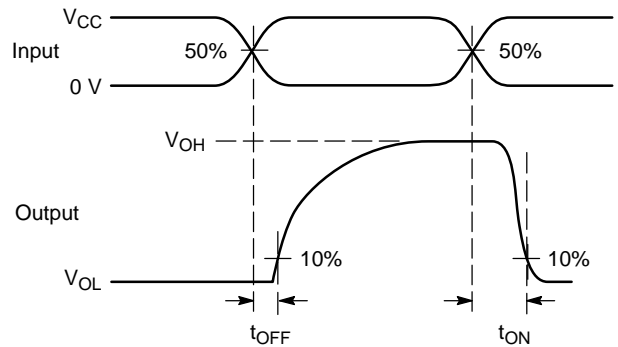
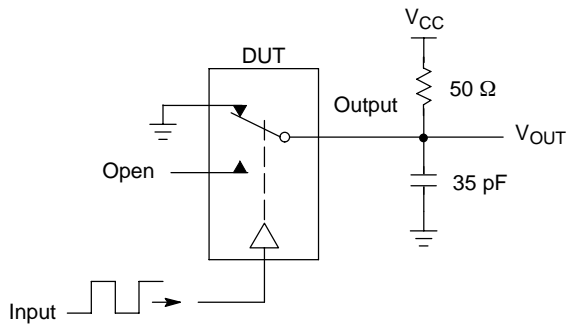
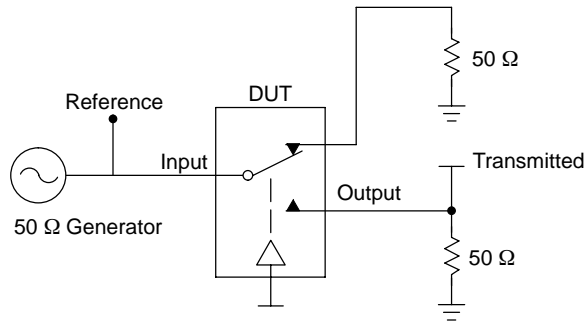


Figure 4.  $t_{ON}/t_{OFF}$

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

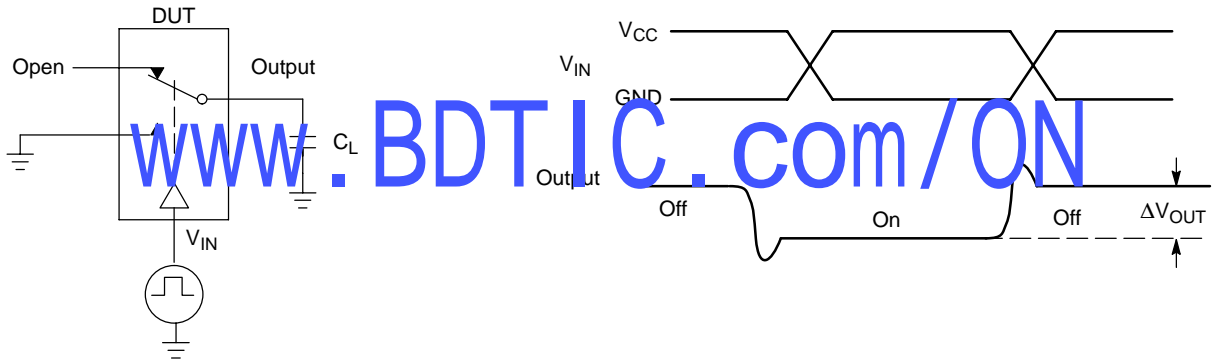
$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

$V_{CT}$  = Use  $V_{ISO}$  setup and test to all other switch analog input/outputs terminated with 50 Ω

**Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**



**Figure 6. Charge Injection: (Q)**

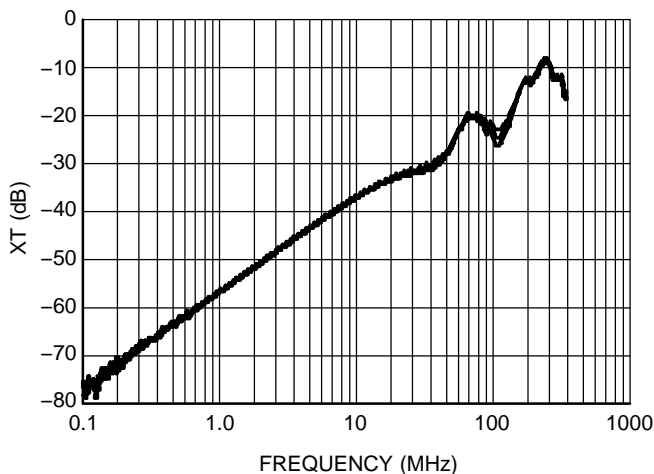


Figure 7. Cross Talk vs. Frequency  
@  $V_{CC} = 4.5\text{ V}$

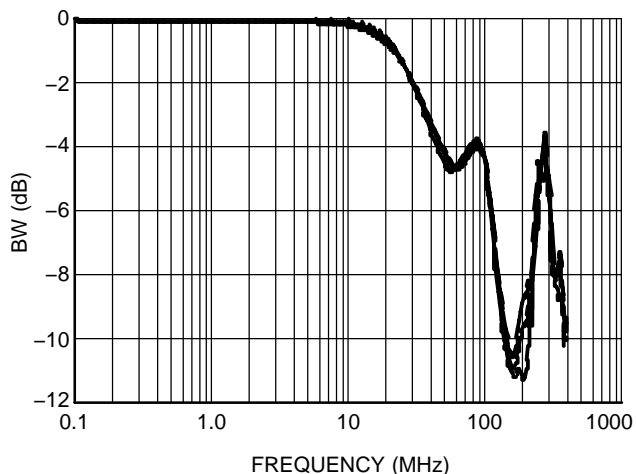


Figure 8. Bandwidth vs. Frequency

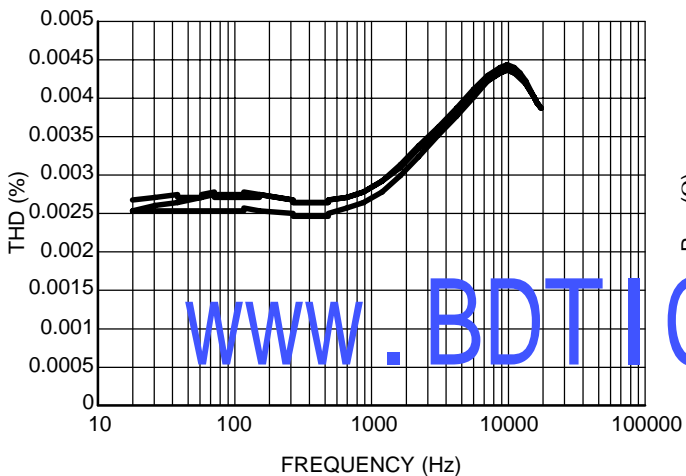


Figure 9. Total Harmonic Distortion

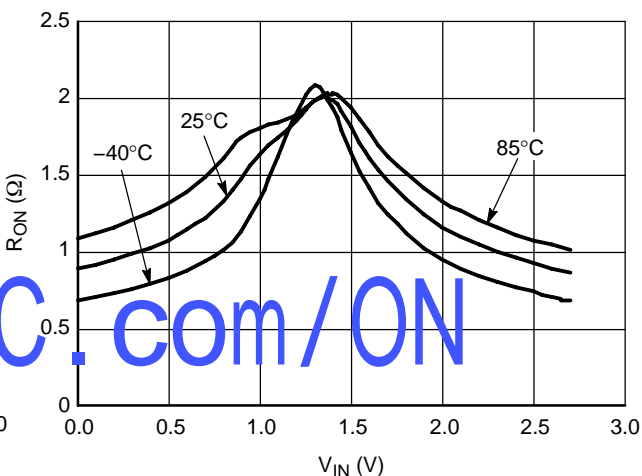


Figure 10. On-Resistance vs. Input Voltage  
@  $V_{CC} = 2.7\text{ V}$

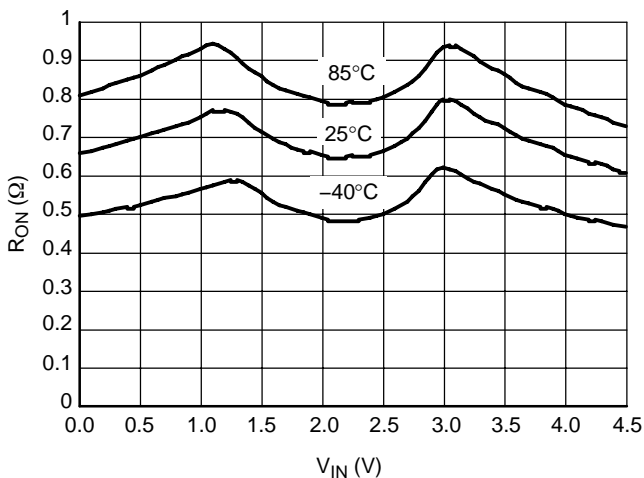


Figure 11. On-Resistance vs. Input Voltage  
@  $V_{CC} = 4.5\text{ V}$

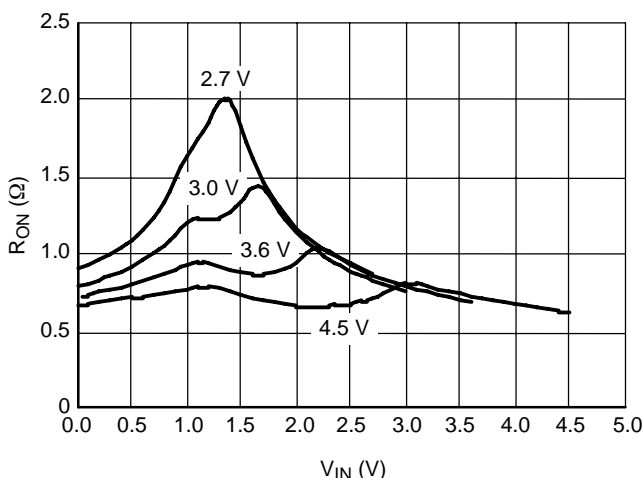


Figure 12. On-Resistance vs. Input Voltage

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## DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature					Package Type	Tape & Reel Size <sup>†</sup>
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAS4157DFT2G	NL	AS	4157	DFT	2	SC-88 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

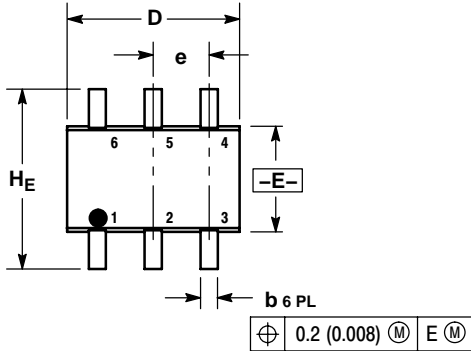
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## PACKAGE DIMENSIONS

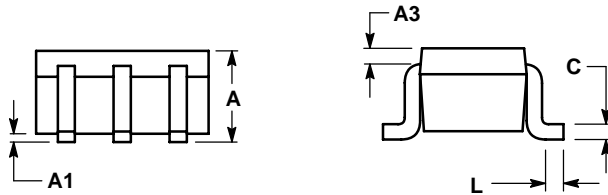
SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE V



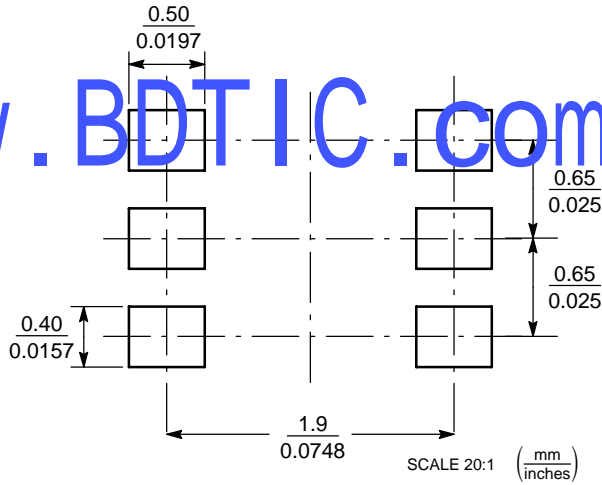
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	2.00	2.10	2.20	0.078	0.082	0.086



### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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