NLAS4599

Low Voltage Single Supply SPDT Analog Switch

The NLAS4599 is an advanced high speed CMOS single pole − double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power−supply range (from V_{CC} to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel select input is compatible with standard CMOS outputs.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

- Channel Select Input Over−Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break−Before−Make Circuitry
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch−up Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V; Machine Model > 200 V
- Chip Complexity: 38 FETs
- Pb−Free Packages are Available

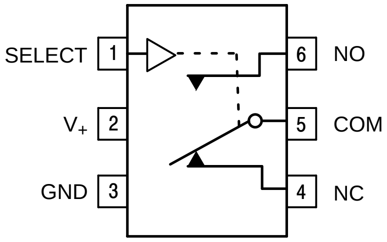

Figure 1. Pin Assignment

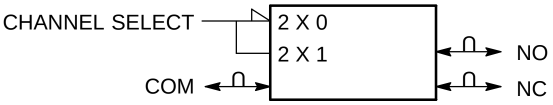

Figure 2. Logic Symbol

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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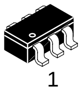
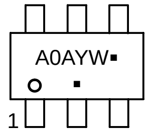
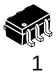
http://onsemi.com

MARKING DIAGRAMS

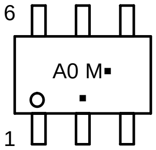


TSOP−6
DT SUFFIX
CASE 318G





SC−88
DF SUFFIX
CASE 419B



A0 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

FUNCTION TABLE

Select	ON Channel
L H	NC NO

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IS}	Analog Input Voltage (V_{NO} or V_{COM})		$-0.5 \le V_{IS} \le V_{CC} + 0.5$	V
V_{IN}	Digital Select Input Voltage		$-0.5 \le V_I \le +7.0$	V
I_{IK}	DC Current, Into or Out of Any Pin		± 50	mA
P_D	Power Dissipation in Still Air	SC−88 TSOP−6	200 200	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1mm from Case for 10 seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	2000 200 N/A	V
$I_{LATCH-UP}$	Latch−Up Performance	Above V_{CC} and Below GND at 125°C (Note 4)	± 300	mA
θ_{JA}	Thermal Resistance	SC−88 TSOP−6	333 333	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	Digital Select Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)		GND	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Rise or Fall Time, SELECT	$V_{CC} = 3.3\ V \pm 0.3\ V$ $V_{CC} = 5.0\ V \pm 0.5\ V$	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

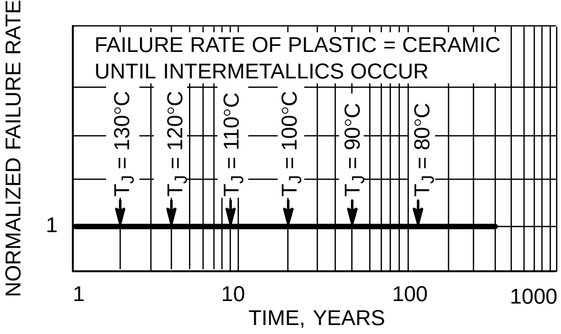


Figure 3. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS − Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				−55 to 25°C	<85°C	<125°C	
V_{IH}	Minimum High−Level Input Voltage, Select Input		2.0 2.5 3.0 4.5 5.5	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	V
V_{IL}	Maximum Low−Level Input Voltage, Select Input		2.0 2.5 3.0 4.5 5.5	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current, Select Input	V_{IN} = 5.5 V or GND	5.5	±0.1	±1.0	±1.0	µA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or GND	0	± 10	± 10	± 10	µA
I_{CC}	Maximum Quiescent Supply Current	Select and V_{IS} = V_{CC} or GND	5.5	1.0	1.0	2.0	µA

DC ELECTRICAL CHARACTERISTICS − Analog Section

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				−55 to 25°C	<85°C	<125°C	
R_{ON}	Maximum “ON” Resistance (Figures 17 − 23)	V_{IN} = V_{IL} or V_{IH} V_{IS} = GND to V_{CC} I_{IN}I ≤ 10.0 mA	2.5 3.0 4.5 5.5	85 45 30 25	95 50 35 30	105 55 40 35	Ω
R_{FLAT} (ON)	ON Resistance Flatness (Figures 17 − 23)	V_{IN} = V_{IL} or V_{IH} I_{IN}I ≤ 10.0 mA V_{IS} = 1V, 2V, 3.5V	4.5	4	4	5	Ω
ΔR_{ON} (ON)	ON Resistance Match Between Channels	V_{IN} = V_{IL} or V_{IH} I_{IN}I ≤ 10.0 mA V_{NO} or V_{NC} = 3.5 V	4.5	2	2	3	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	NO or NC Off Leakage Current (Figure 9)	V_{IN} = V_{IL} or V_{IH} V_{NO} or V_{NC} = 1.0 V_{COM} 4.5 V	5.5	1	10	100	nA
$I_{COM(ON)}$	COM ON Leakage Current (Figure 9)	V_{IN} = V_{IL} or V_{IH} V_{NO} 1.0 V or 4.5 V with V_{NC} floating or V_{NO} 1.0 V or 4.5 V with V_{NO} floating V_{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	V_{IS} (V)	Guaranteed Max Limit							Unit
					−55 to 25°C			<85°C		<125°C		
					Min	Typ*	Max	Min	Max	Min	Max	
t_{ON}	Turn−On Time (Figures 12 and 13)	$R_L = 300\ \Omega$, $C_L = 35$ pF (Figures 5 and 6)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	5 5 2 2	23 16 11 9	28 21 16 14	5 5 2 2	30 25 20 20	5 5 2 2	30 25 20 20	ns
t_{OFF}	Turn−Off Time (Figures 12 and 13)	$R_L = 300\ \Omega$, $C_L = 35$ pF (Figures 5 and 6)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	1 1 1 1	7 5 4 3	12 10 9 8	1 1 1 1	15 15 12 12	1 1 1 1	15 15 12 12	ns
t_{BBM}	Minimum Break−Before−Make Time	$V_{IS} = 3.0$ V (Figure 4) $R_L = 300\ \Omega$, $C_L = 35$ pF	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	1 1 1 1	12 11 6 5		1 1 1 1		1 1 1 1		ns

*Typical Characteristics are at 25°C.

		Typical @ 25, VCC = 5.0 V	
C_{IN} C_{NO} or C_{NC} C_{COM} $C_{(ON)}$	Maximum Input Capacitance, Select Input Analog I/O (switch off) Common I/O (switch off) Feedthrough (switch on)	8 10 10 20	pF

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V_{CC} (V)	Typical 25°C	Unit
BW	Maximum On−Channel −3dB Bandwidth or Minimum Frequency Response (Figure 10)	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	170 200 200	MHz
V_{ONL}	Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	−3 −3 −3	dB
V_{ISO}	Off−Channel Isolation (Figure 10)	f = 100 kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	−93 −93 −93	dB
Q	Charge Injection Select Input to Common I/O (Figure 15)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0\ \Omega$, $C_L = 1000$ pF $Q = C_L * \Delta V_{OUT}$ (Figure 8)	3.0 5.5	1.5 3.0	pC
THD	Total Harmonic Distortion THD + Noise (Figure 14)	$F_{IS} = 20$ Hz to 100 kHz, $R_L = \text{Rgen} = 600\ \Omega$, $C_L = 50$ pF $V_{IS} = 5.0\ V_{PP}$ sine wave	5.5	0.1	%

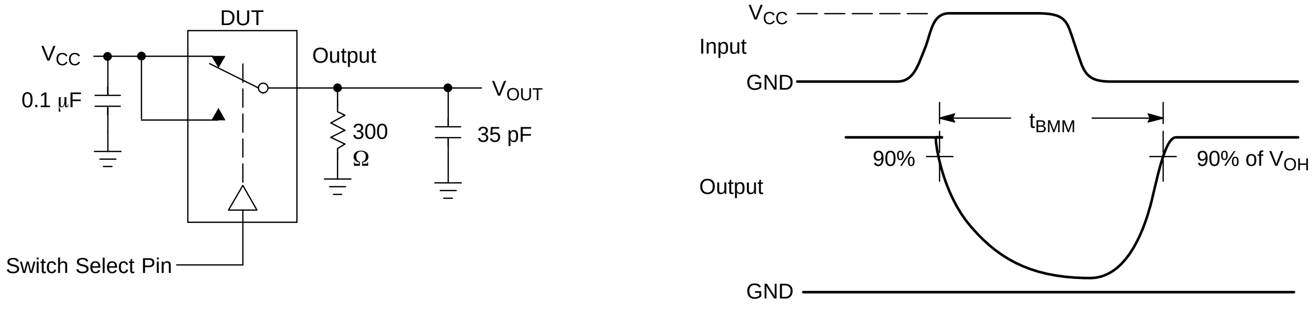


Figure 4. t_{BBM} (Time Break−Before−Make)

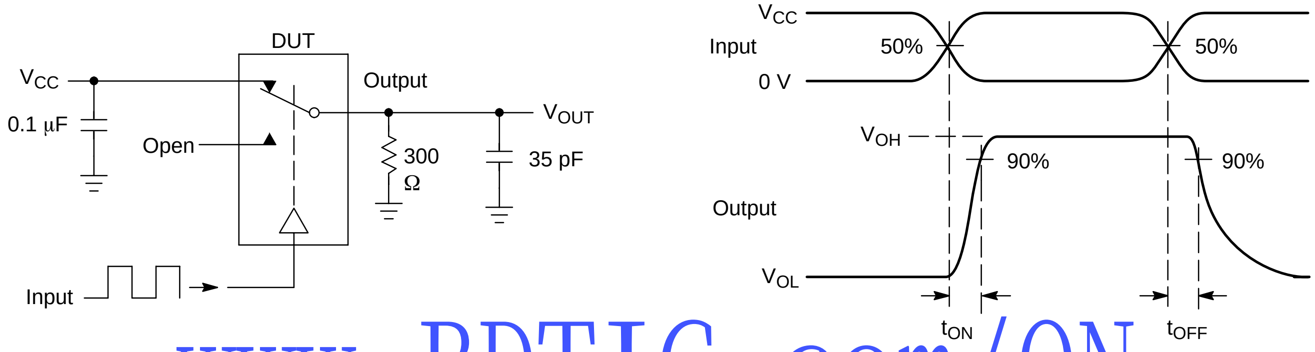


Figure 5. t_{ON}/t_{OFF}

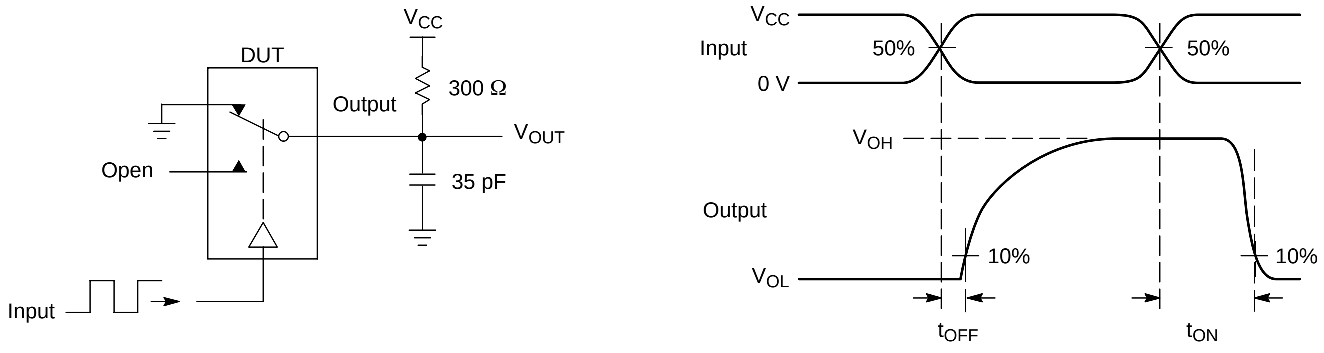
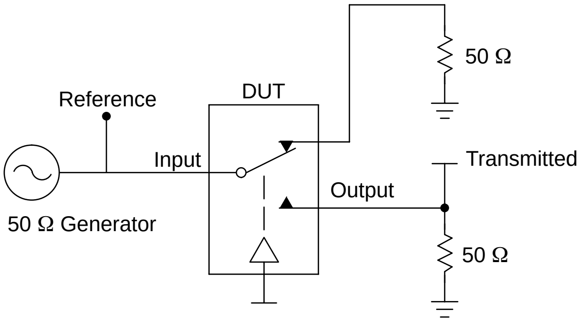


Figure 6. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log}\left(\frac{V_{OUT}}{V_{IN}}\right) \quad \text{for } V_{IN} \text{ at 100 kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log}\left(\frac{V_{OUT}}{V_{IN}}\right) \quad \text{for } V_{IN} \text{ at 100 kHz to 50 MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

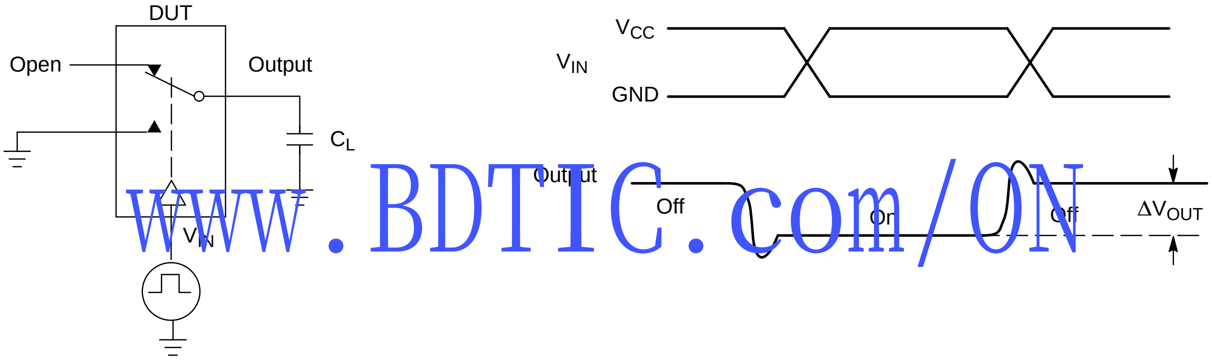


Figure 8. Charge Injection: (Q)

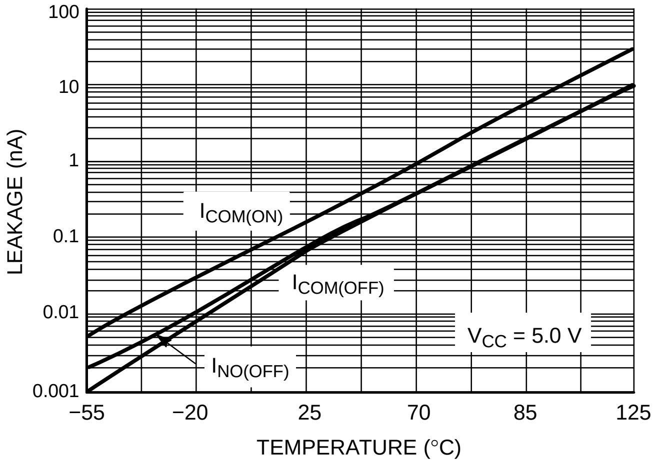


Figure 9. Switch Leakage vs. Temperature

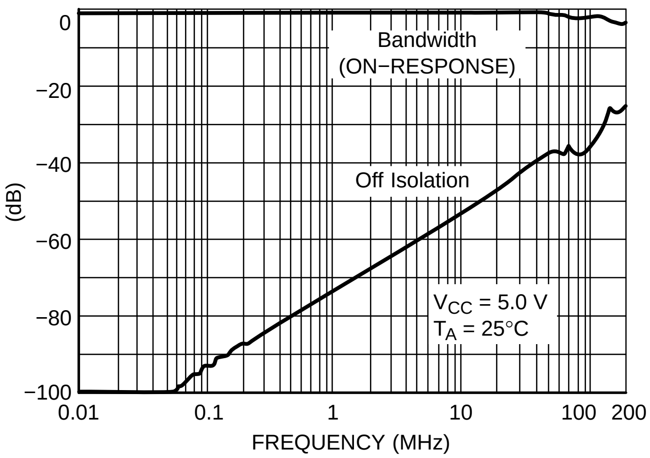


Figure 10. Bandwidth and Off−Channel Isolation

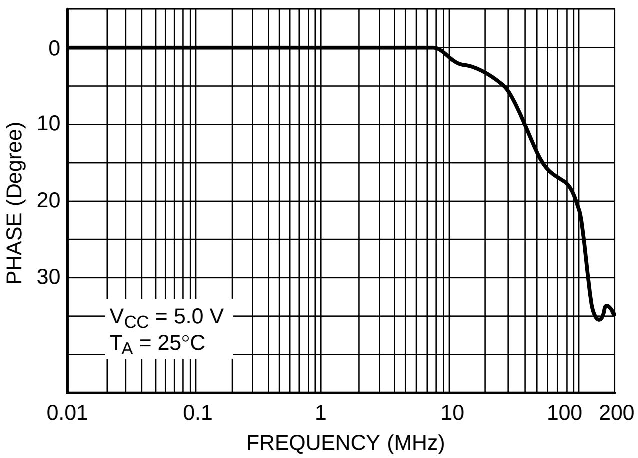


Figure 11. Phase vs. Frequency

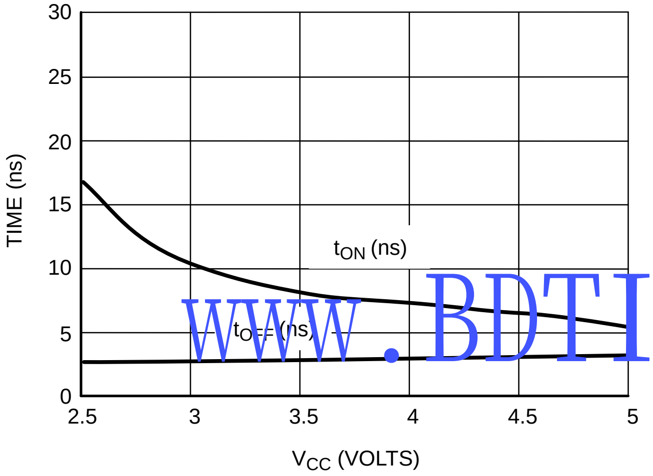


Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

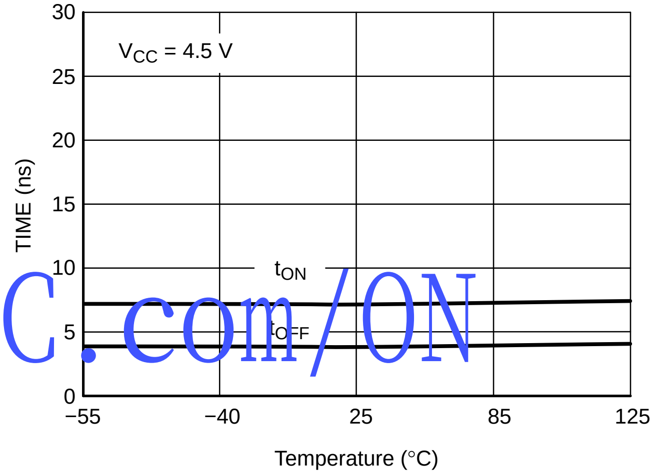


Figure 13. t_{ON} and t_{OFF} vs. Temp

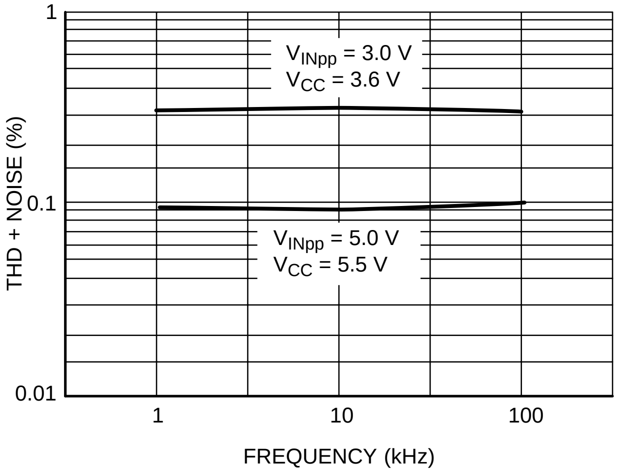


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

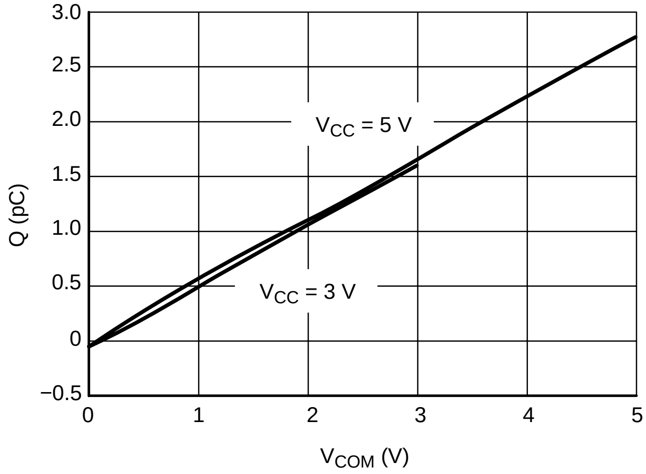


Figure 15. Charge Injection vs. COM Voltage

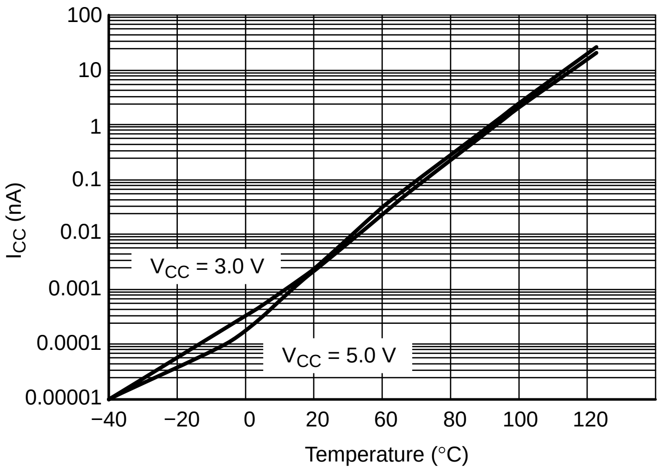


Figure 16. I_{CC} vs. Temp, V_{CC} = 3 V & 5 V

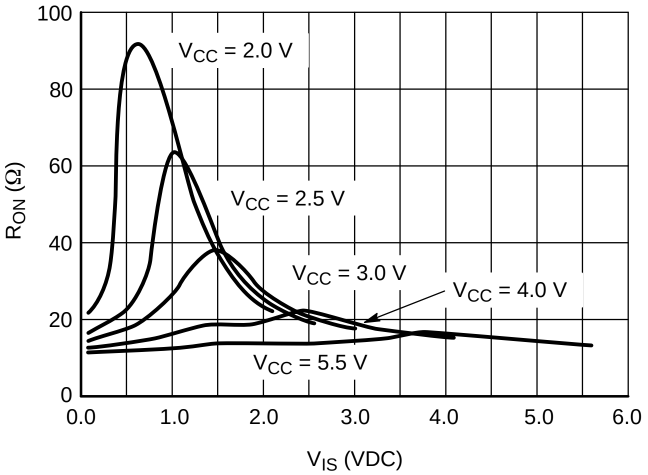


Figure 17. R_{ON} vs. $V_{CC,}$ Temp = 25°C

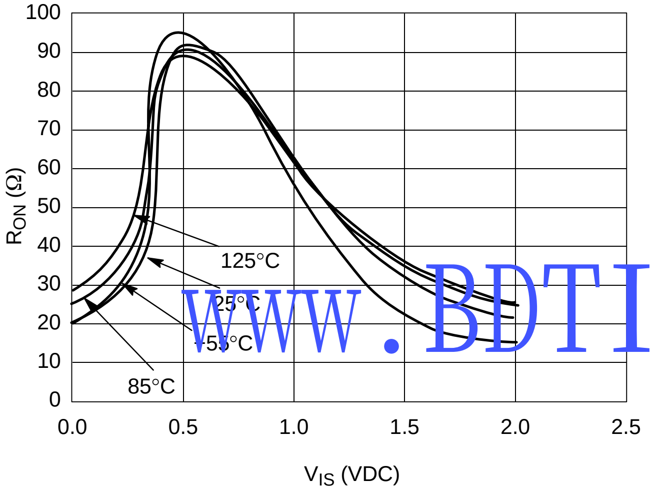


Figure 18. R_{ON} vs Temp, V_{CC} = 2.0 V

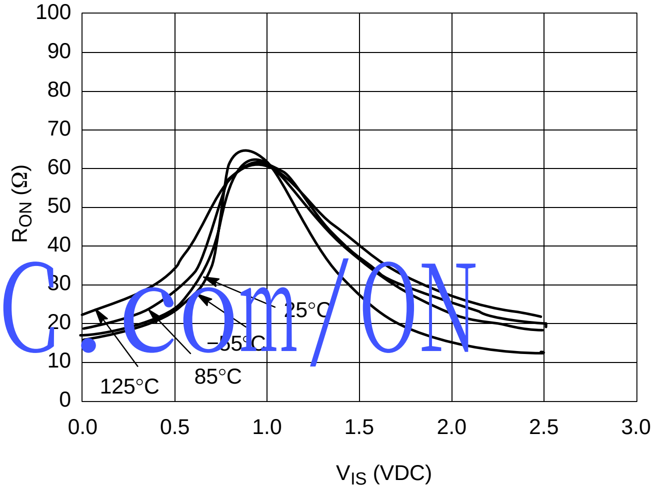


Figure 19. R_{ON} vs. Temp, V_{CC} = 2.5 V

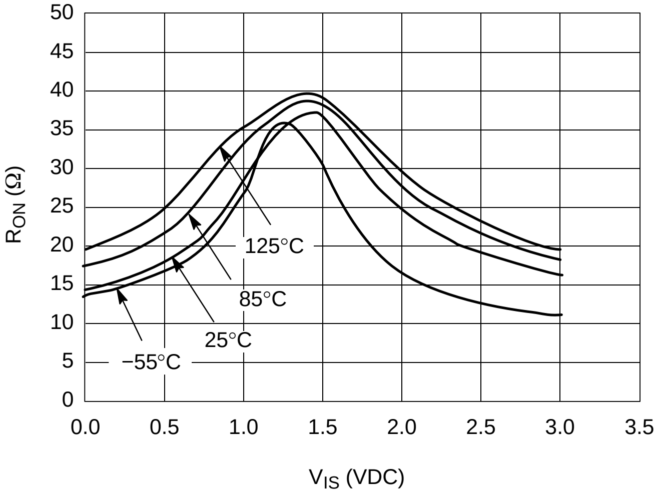


Figure 20. R_{ON} vs. Temp, V_{CC} = 3.0 V

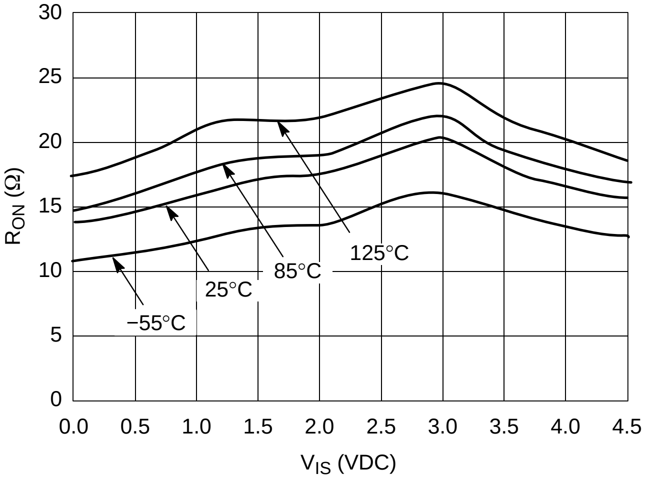


Figure 21. R_{ON} vs. Temp, V_{CC} = 4.5 V

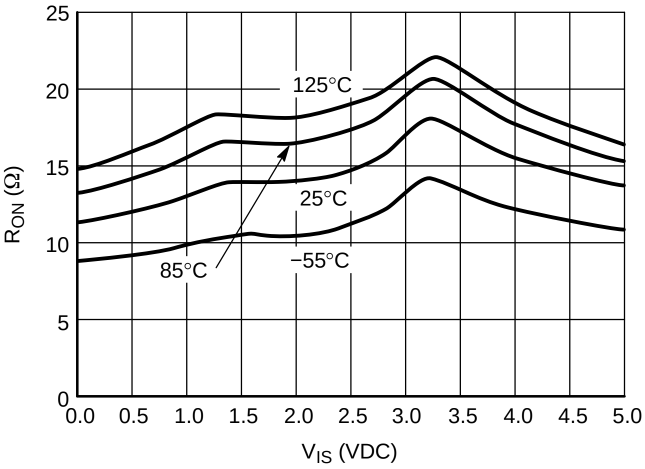


Figure 22. R_{ON} vs. Temp, V_{CC} = 5.0 V

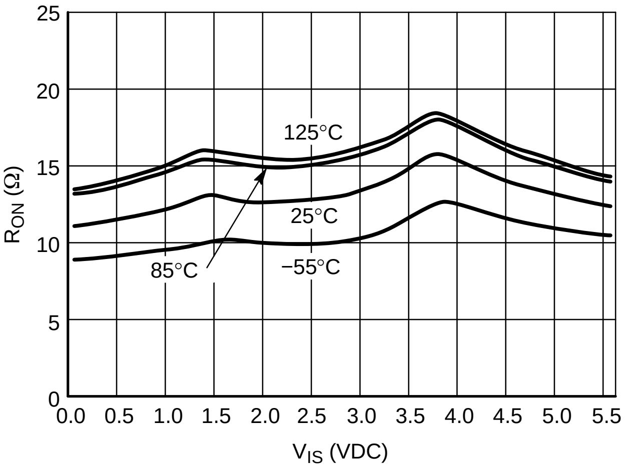


Figure 23. R_{ON} vs. Temp, V_{CC} = 5.5 V

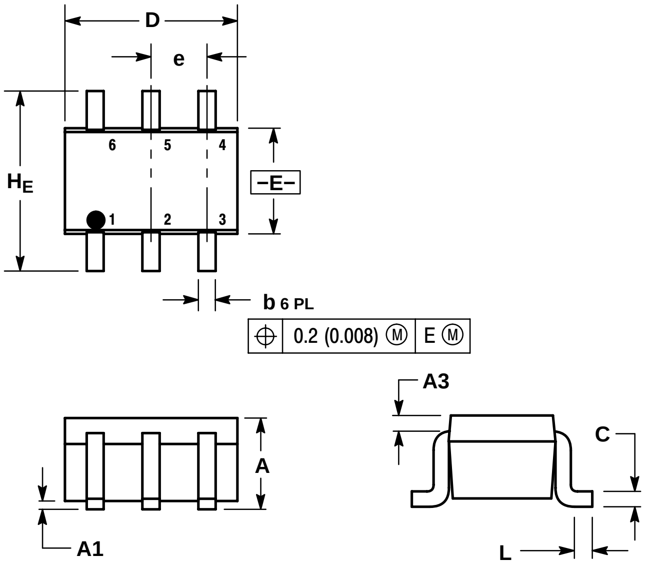
ORDERING INFORMATION

Device	Device Nomenclature				Package	Shipping†
	Circuit Indicator	Technology	Device Function	Suffix		
NLAS4599DFT2	NL	AS	DF	T2	SC−88	3000 / Tape & Reel
NLAS4599DFT2G	NL	AS	DF	T2G	SC−88 (Pb−Free)	3000 / Tape & Reel
NLAS4599DTT1	NL	AS	DT	T1	TSOP−6	3000 / Tape & Reel
NLAS4599DTT1G	NL	AS	DT	T1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NLVAS4599DFT2	NL	AS	DF	T2	SC−88	3000 / Tape & Reel
NLVAS4599DFT2G	NL	AS	DF	T2G	SC−88 (Pb−Free)	3000 / Tape & Reel
NLVAS4599DTT1	NL	AS	DT	T1	TSOP−6	3000 / Tape & Reel
NLVAS4599DTT1G	NL	AS	DT	T1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

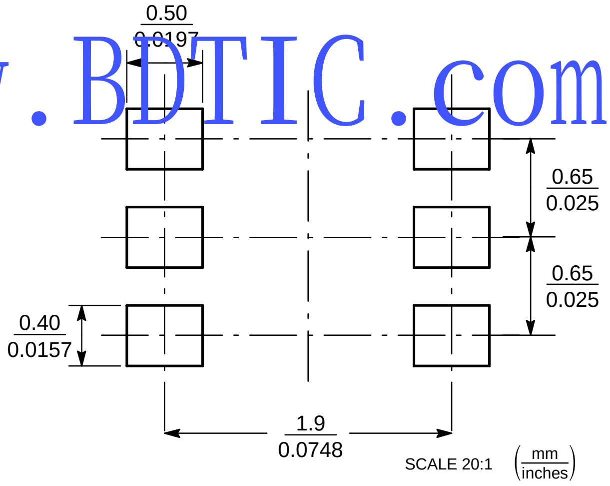
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*

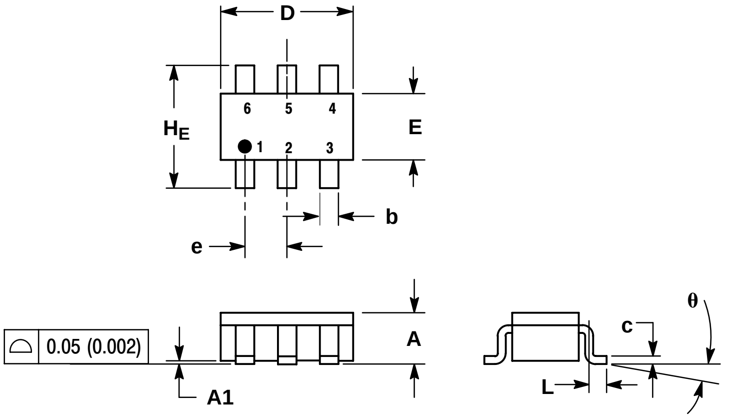


SC−88/SC70−6/SOT−363

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

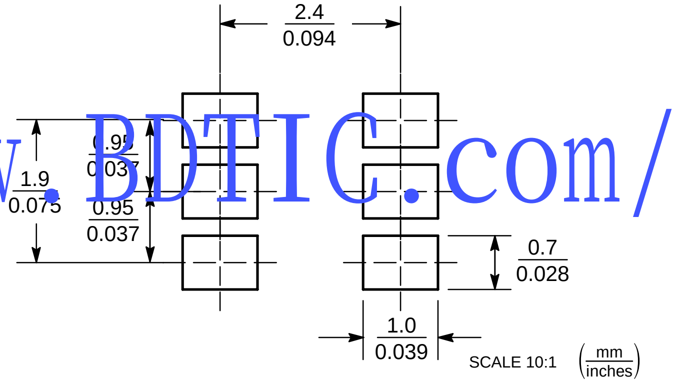
TSOP−6
CASE 318G−02
ISSUE S



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

SOLDERING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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