NLAS7242

High-Speed USB 2.0 (480 Mbps) DPDT Switches

The NLAS7242 is a DPDT switch optimized for high−speed USB 2.0 applications within portable systems. It features ultra−low on capacitance, C_{ON} = 7.5 pF (typ), and a bandwidth above 900 MHz. It is optimized for applications that use a single USB interface connector to route multiple signal types. The C_{ON} and R_{ON} of both channels are suitably low to allow the NLAS7242 to pass any speed USB data or audio signals going to a moderately resistive terminal such as an external headset. The device is offered in a UQFN10 1.4 mm x 1.8 mm package.

Features

- Optimized Flow−Through Pinout
- R_{ON}: 7.5 Ω Typ @ V_{CC} = 4.2 V
- C_{ON}: 7.5 pF Typ @ V_{CC} = 3.3 V
- V_{CC} Range: 1.65 V to 4.5 V
- Typical Bandwidth: 900 MHz
- 1.4 mm x 1.8 mm x 0.50 mm UQFN10
- OVT on Common Signal Pins D+/D− up to 5.25 V
- 8 kV ESD Protection on D+/D− to GND
- This is a Pb−Free Device

Typical Applications

- High Speed USB 2.0 Data
- Mobile Phones
- Portable Devices

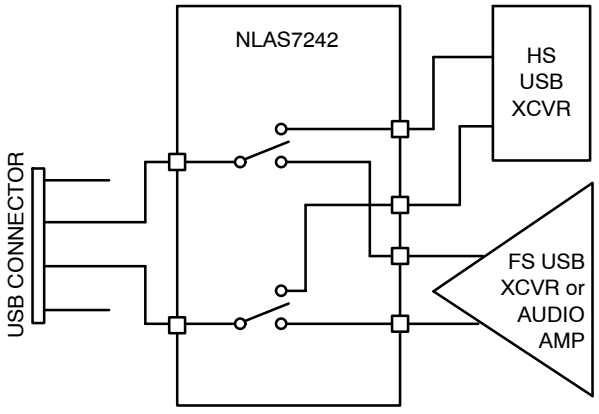

Figure 1. Application Diagram

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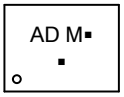
MARKING DIAGRAM

UQFN10
CASE 488AT



AD = Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NLAS7242MUTBG	UQFN0 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

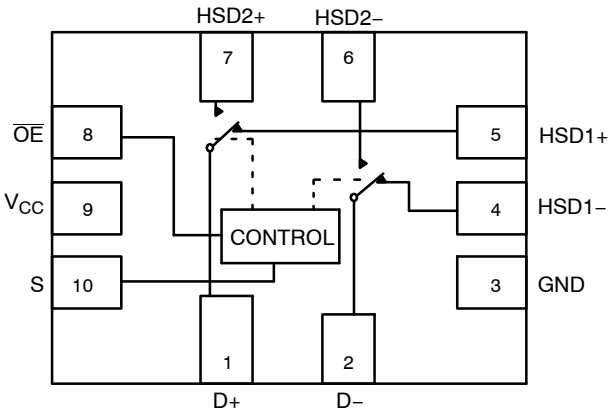


Figure 2. Pin Connections and Logic Diagram
(Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Control Input
$\overline{OE}$	Output Enable
HSD1+, HSD1−, HSD2+, HSD2−, D+, D−	Data Ports

Table 2. TRUTH TABLE

$\overline{OE}$	S	HSD1+, HSD1−	HSD2+, HSD2−
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	−0.5 to +5.5	V
V_{IS}	HSDn+, HSDn−	Analog Signal Voltage	−0.5 to V_{CC} + 0.3	V
	D+, D−		−0.5 to +5.25	
V_{IN}	S	Control Input Voltage	−0.5 to +5.5	V
I_{CC}	V_{CC}	Positive DC Supply Current	50	mA
T_S		Storage Temperature	−65 to +150	°C
I_{IS_CON}	HSDn+, HSDn−, D+, D−	Analog Signal Continuous Current−Closed Switch	±300	mA
I_{IS_PK}	HSDn+, HSDn−, D+, D−	Analog Signal Continuous Current 10% Duty Cycle	±500	mA
I_{IN}	S	Control Input Current	±20	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}		Positive DC Supply Voltage	1.65	4.5	V
V_{IS}	HSDn+, HSDn−	Analog Signal Voltage	GND	V_{CC}	V
	D+, D−		GND	4.5	

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{IN}	S	Control Input Voltage	GND	V_{CC}	V
T_A		Operating Temperature	–40	+85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

ESD PROTECTION

Symbol	Parameter	Value	Unit
ESD	Human Body Model – All Pins	3.0	kV

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT VOLTAGE (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
V_{IH}	S	Control Input HIGH Voltage (See Figure 11)		2.7 3.3 4.2	1.25 1.25 1.25	–	–	V
V_{IL}	S	Control Input LOW Voltage (See Figure 11)		2.7 3.3 4.2	–	–	0.4 0.4 0.5	V
I_{IN}	S	Current Input Leakage Current	$0 \le V_{IS} \le V_{CC}$	1.65 – 4.5	–	–	±1.0	μA

SUPPLY CURRENT AND LEAKAGE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
I_{CC}	V_{CC}	Quiescent Supply Current	$V_{IS} = V_{CC}$ or GND; I_D = 0 A	1.65 – 4.5	–	–	1.0	μA
I_{OZ}		OFF State Leakage	$0 \le V_{IS} \le V_{CC}$	1.65 – 4.5	–	±0.1	±1.0	μA
I_{OFF}	D+, D–	Power OFF Leakage Current	$0 \le V_{IS} \le V_{CC}$	0	–	–	±1.0	μA

LIMITED V_{IS} SWING ON RESISTANCE (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
R_{ON}		On–Resistance	I_{ON} = 8 mA V_{IS} = 0 V to 0.4 V	2.7 3.3 4.2	–	6.0 6.0 5.5	–	Ω
R_{FLAT}		On–Resistance Flatness	I_{ON} = 8 mA V_{IS} = 0 V to 0.4 V	2.7 3.3 4.2	–	0.35 0.35 0.20	–	Ω
ΔR_{ON}		On–Resistance Matching	I_{ON} = 8 mA V_{IS} = 0 V to 0.4 V	2.7 3.3 4.2	–	0.8 0.7 0.5	–	Ω

FULL V_{IS} SWING ON RESISTANCE (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	–40°C to +85°C			Unit
					Min	Typ	Max	
R_{ON}		On–Resistance	I_{ON} = 8 mA V_{IS} = 0 V to V_{CC}	2.7 3.3 4.2	–	9.3 8.7 7.5	–	Ω
R_{FLAT}		On–Resistance Flatness	I_{ON} = 8 mA V_{IS} = 0 V to V_{CC}	2.7 3.3 4.2	–	3.6 3.3 2.9	–	Ω
ΔR_{ON}		On–Resistance	I_{ON} = 8 mA V_{IS} = 0 V to V_{CC}	2.7 3.3 4.2	–	0.8 0.7 0.5	–	Ω

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 35 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
					Min	Typ	Max	
t_{ON}	Closed to Open	Turn−ON Time (See Figures 4 and 5)		1.65 – 4.5	–	13.0	30.0	ns
t_{OFF}	Open to Closed	Turn−OFF Time (See Figures 4 and 5)		1.65 – 4.5	–	12.0	25.0	ns
T_{BBM}		Break−Before−Make Time (See Figure 3)		1.65 – 4.5	2.0	–	–	ns
BW		−3 dB Bandwidth	C_L = 5 pF	1.65 – 4.5	–	900	–	MHz

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
					Min	Typ	Max	
O_{IRR}	Open	OFF−Isolation (See Figure 6)	f = 240 MHz	1.65 – 4.5	–	−21	–	dB
X_{TALK}	HSD+ to HSD−	Non−Adjacent Channel Crosstalk	f = 240 MHz	1.65 – 4.5	–	−21	–	dB

CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF)

Symbol	Pins	Parameter	Test Conditions	−40°C to +85°C			Unit
				Min	Typ	Max	
C_{IN}	$\overline{OE}$	Control Pin Input Capacitance	V_{CC} = 0 V, f = 1 MHz	–	1.5	–	pF
			V_{CC} = 0 V, f = 10 MHz	–	1.0	–	
C_{ON}	HSD+ to D+	HSD+, HSD− ON Capacitance	V_{CC} = 3.3 V; $\overline{OE}$ = 0 V, f = 1 MHz	–	7.5	–	
			V_{CC} = 3.3 V; $\overline{OE}$ = 0 V, f = 10 MHz	–	6.5	–	
C_{OFF}	D+, D−	HSD+, HSD− OFF Capacitance	V_{CC} = V_{IS} = 3.3 V; $\overline{OE}$ = 3.3 V, f = 1 MHz	–	3.8	–	
			V_{CC} = V_{IS} = 3.3 V; $\overline{OE}$ = 3.3 V, f = 10 MHz	–	2.0	–	

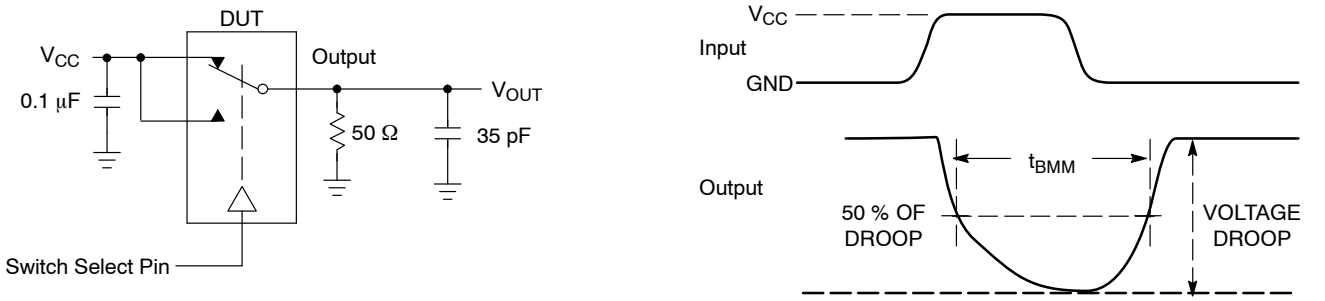


Figure 3. t_{BBM} (Time Break−Before−Make)

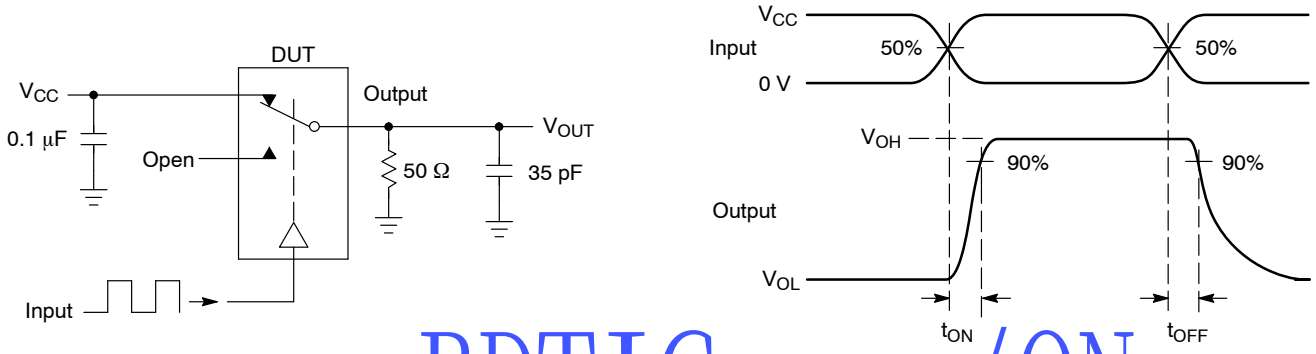


Figure 4. t_{ON}/t_{OFF}

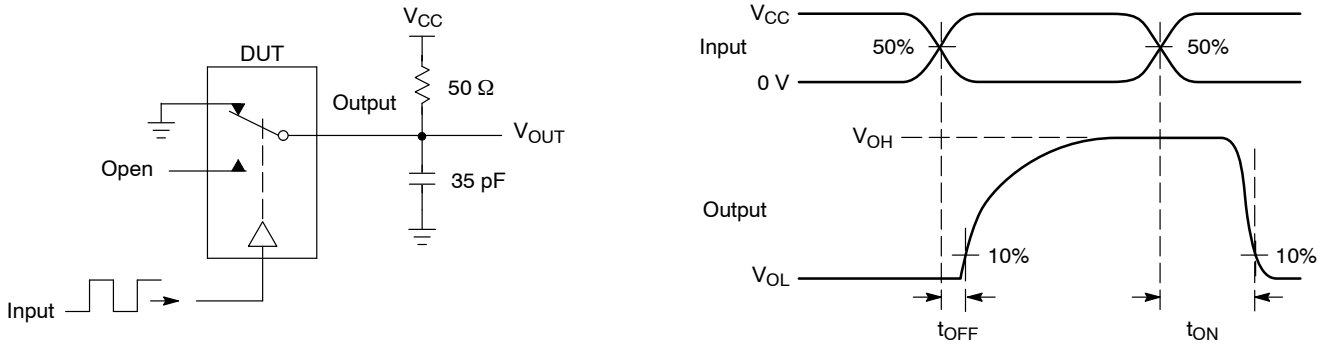
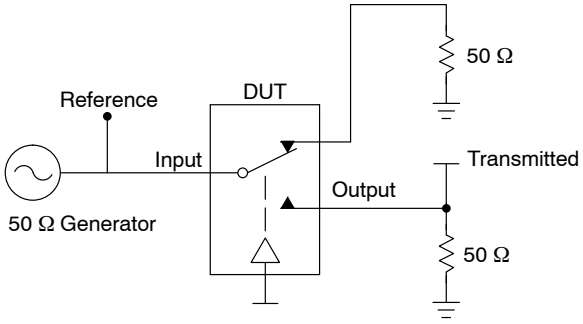


Figure 5. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

DETAILED DESCRIPTION

High Speed (480Mbps) USB 2.0 Optimized

The NLAS7242 is a DPDT switch designed for USB applications within portable systems. The R_{ON} and C_{ON} of both switches are maintained at industry−leading low levels in order to ensure maximum signal integrity for USB 2.0 high speed data communication. The NLAS7242 switch can be used to switch between high speed (480Mbps) USB signals and a variety of audio or data signals such as full speed USB, UART or even a moderately resistive audio terminal.

Over Voltage Tolerant

The NLAS7242 features over voltage tolerant I/O protection on the common signal pins D+/D−. This allows the switch to interface directly with a USB connector. The D+/D− pins can withstand a short to V_{BUS}, up to 5.25 V, continuous DC current for up to 24 hours as specified in the USB 2.0 specification. This protection is achieved without the need for any external resistors or protection devices.

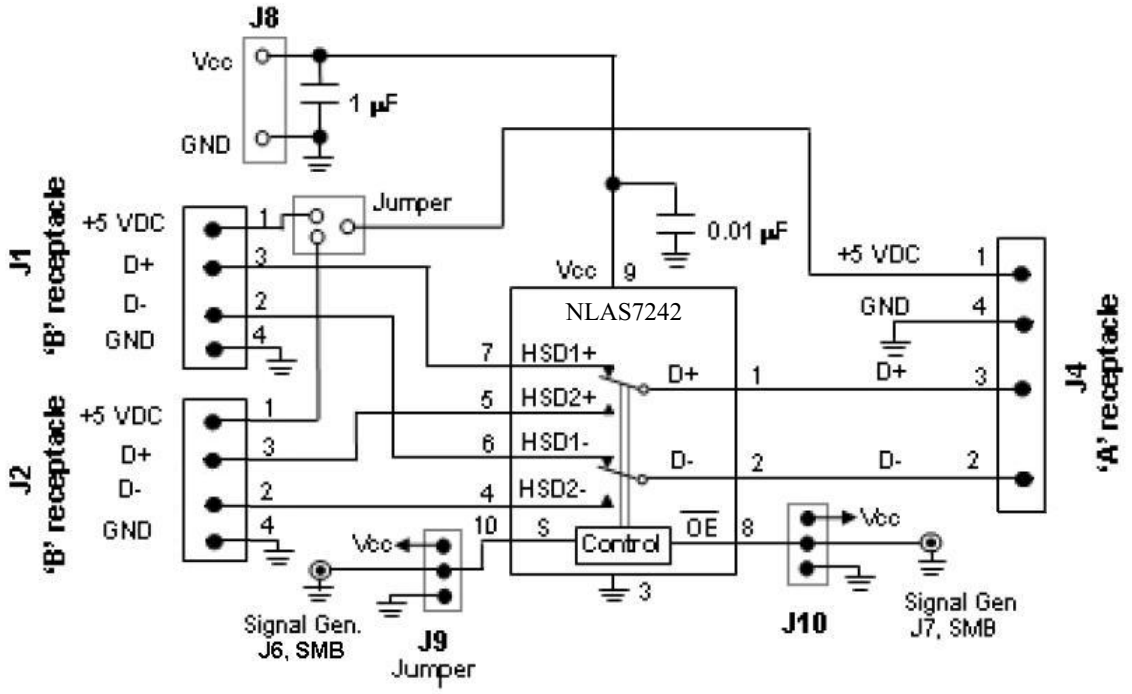


Figure 7. Board Schematic

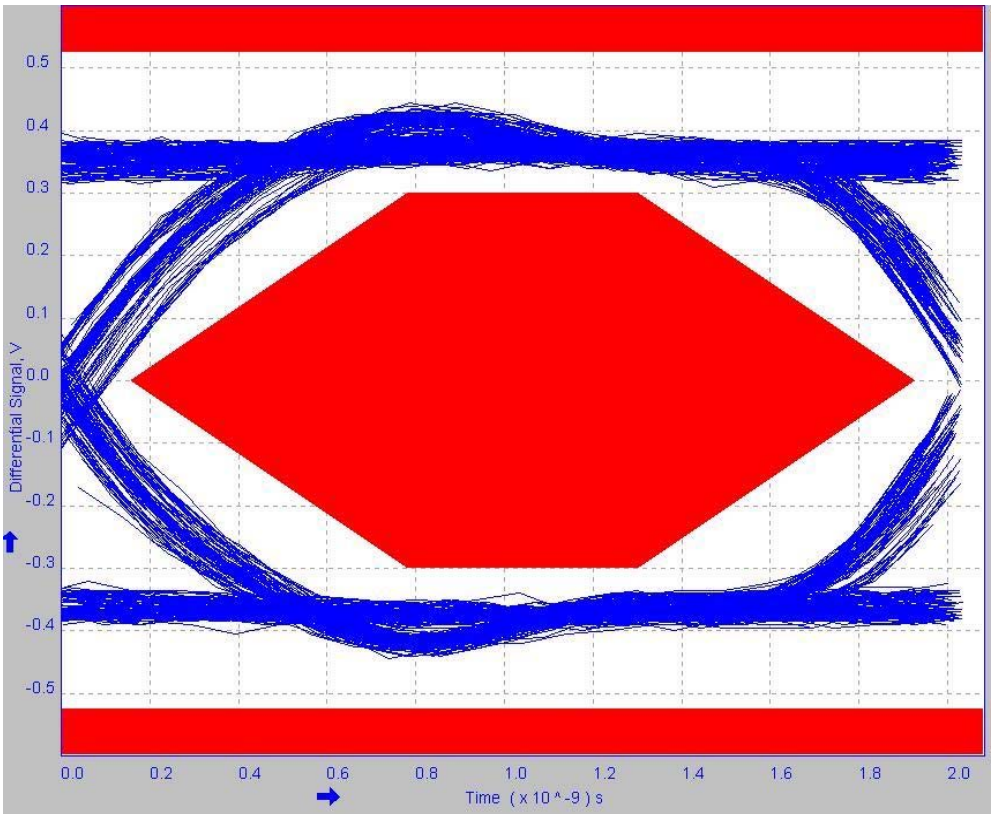


Figure 8. Signal Quality

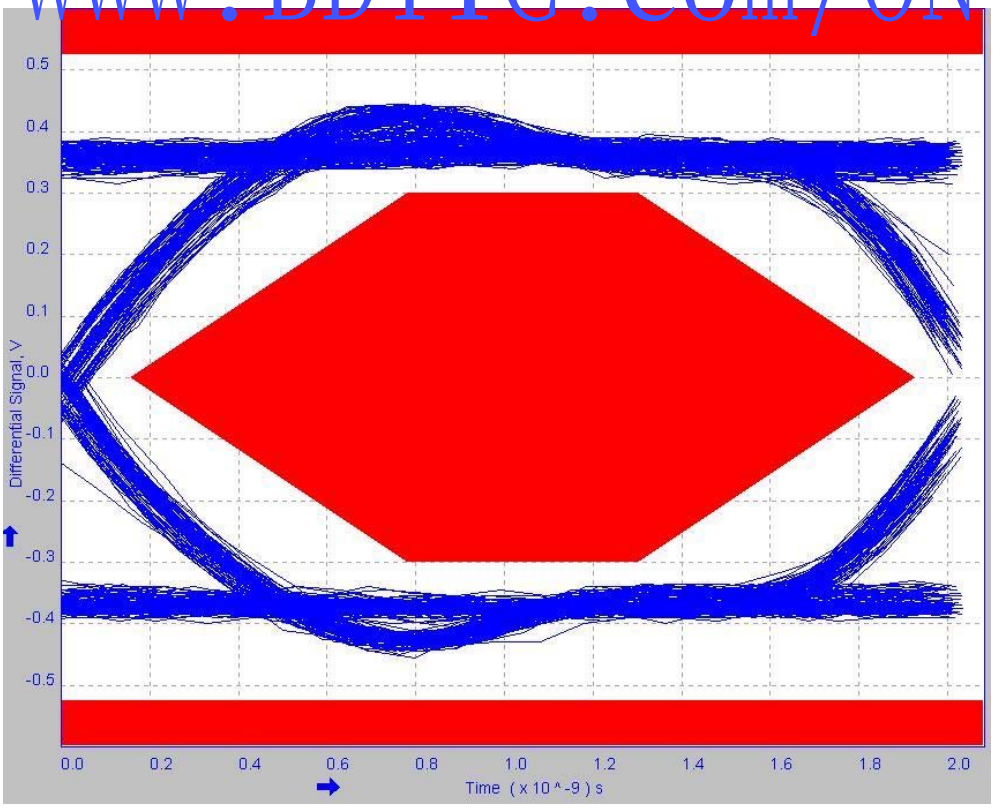


Figure 9. Near End Eye Diagram

Near End Test Data:					Min	Max
Std.	Consecutive jitter range	-61.64	113.30	ps	-200 ps	+200 ps
	Paired JK jitter range	-58.36	46.47	ps		
	Paired KJ jitter range	-62.00	81.30	ps		
NO	Consecutive jitter range	-66.69	69.37	ps	-200 ps	+200 ps
	Paired JK jitter range	-74.71	60.06	ps		
	Paired KJ jitter range	-58.86	70.90	ps		

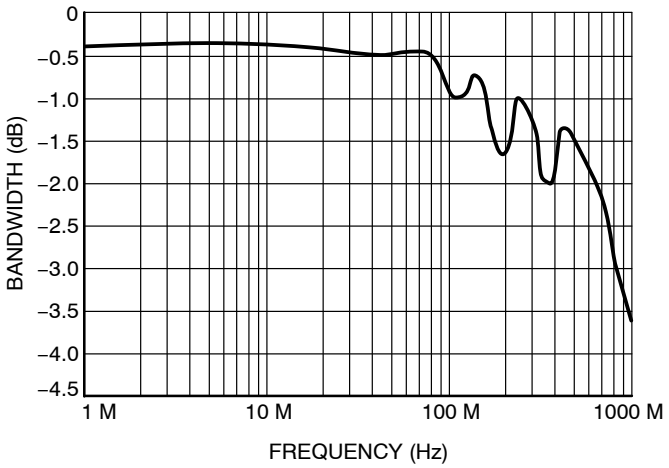


Figure 10. Bandwidth vs. Frequency

I_{CC} Leakage Current as a Function of V_{IN} Voltage

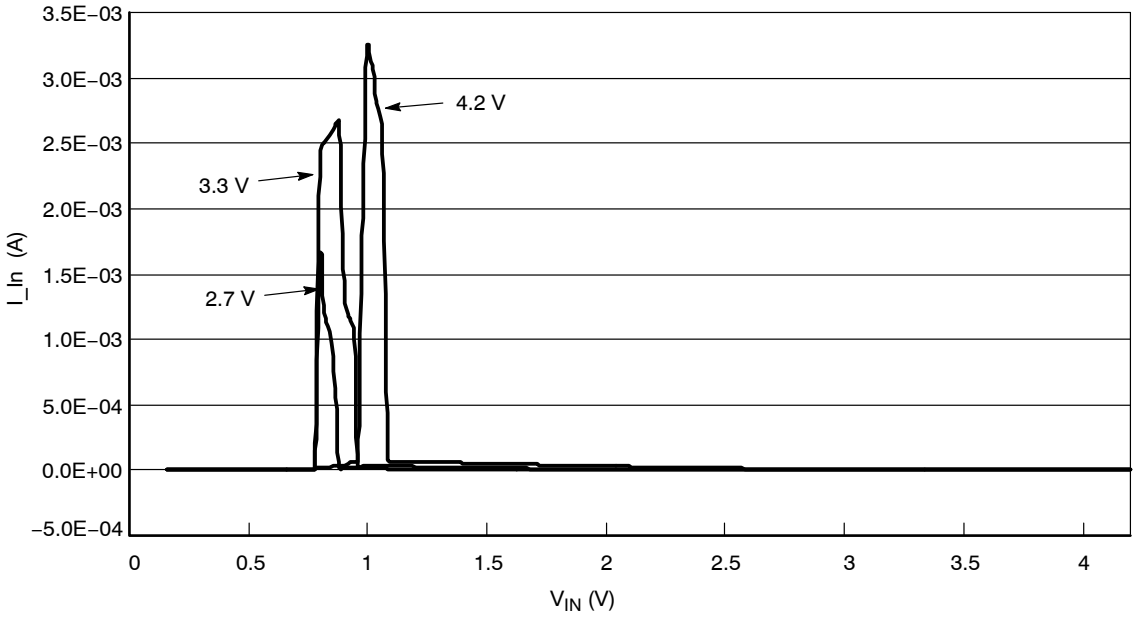
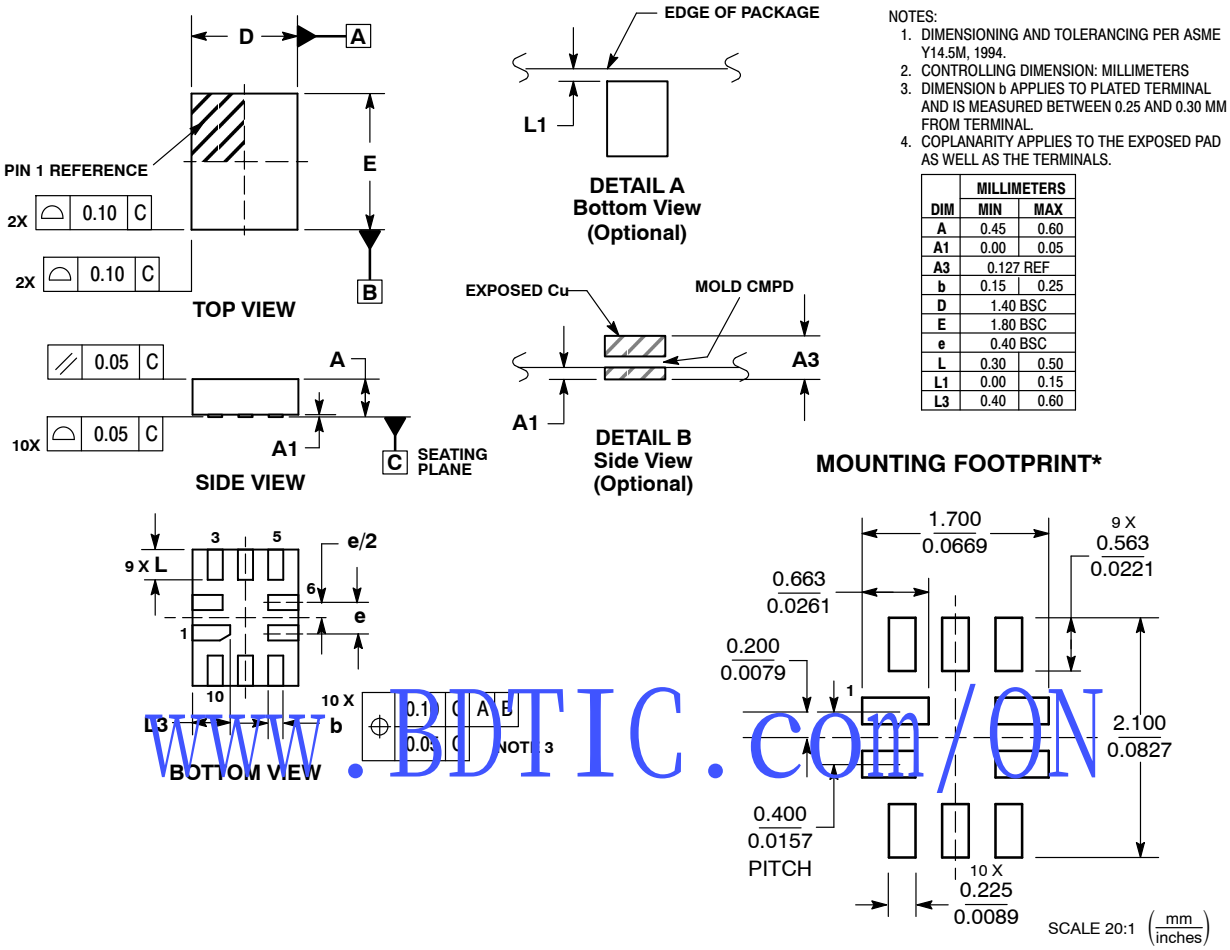


Figure 11. I_{CC} Leakage Current vs. V_{IN} Voltage

PACKAGE DIMENSIONS

UQFN10 1.4x1.8, 0.4P
CASE 488AT−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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