

NTLJS3A18PZ

Power MOSFET

-20 V, -8.2 A, μ Cool™ Single P-Channel, 2.0x2.0x0.8 mm WDFN Package

Features

- WDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile WDFN (2.0x2.0x0.8 mm) for Board Space Saving
- Ultra Low $R_{DS(on)}$
- ESD Diode-Protected Gate
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Optimized for Power Management Applications for Portable Products, such as Smart Phones, Media Tablets, PMP, DSC, GPS, and Others
- Battery Switch
- High Side Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	-20	V	
Gate-to-Source Voltage		V_{GS}	± 8.0	V	
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-8.2	A
			$T_A = 85^\circ\text{C}$	-5.9	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	-11.2		
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	1.8	W
			$t \leq 5 \text{ s}$	3.4	
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-5.0	A
			$T_A = 85^\circ\text{C}$	-3.6	
Power Dissipation (Note 2)	Steady State	P_D	$T_A = 25^\circ\text{C}$	0.7	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-40	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
ESD (HBM, JESD22-A114)		V_{ESD}	2000	V	
Source Current (Body Diode) (Note 2)		I_S	-1.1	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

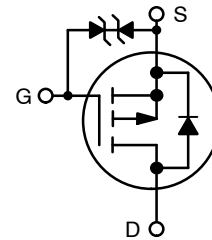
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size, (30 mm², 2 oz Cu).



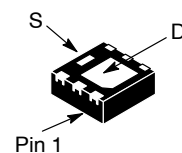
ON Semiconductor®

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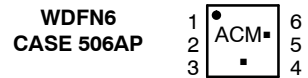
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-20 V	18 m Ω @ -4.5 V	-8.2 A
	25 m Ω @ -2.5 V	
	50 m Ω @ -1.8 V	
	90 m Ω @ -1.5 V	



P-CHANNEL MOSFET

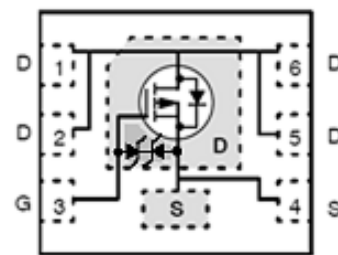


MARKING DIAGRAM



AC = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJS3A18PZTWG	WDFN6	10000/Tape & Reel
NTLJS3A18PZTXG	(Pb-Free)	Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	69	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 1)	$R_{\theta JA}$	37	
Junction-to-Ambient – Steady State Min Pad (Note 2)	$R_{\theta JA}$	186	

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}, \text{Ref to } 25^\circ\text{C}$		11.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$			-1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5.0\text{ V}$			± 5.0	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.4		-1.0	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.9		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -7.0\text{ A}$		14.6	18	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -5.0\text{ A}$		20	25	
		$V_{GS} = -1.8\text{ V}, I_D = -3.0\text{ A}$		25	50	
		$V_{GS} = -1.5\text{ V}, I_D = -1.0\text{ A}$		40	90	
Forward Transconductance	g_{FS}	$V_{DS} = -15\text{ V}, I_D = -3.0\text{ A}$		40		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -15\text{ V}$		2240		pF
Output Capacitance	C_{OSS}			240		
Reverse Transfer Capacitance	C_{RSS}			210		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V}, I_D = -4.0\text{ A}$		28		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.0		
Gate-to-Source Charge	Q_{GS}			2.9		
Gate-to-Drain Charge	Q_{GD}			8.8		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -15\text{ V}, I_D = -4.0\text{ A}, R_G = 1.0\ \Omega$		8.6		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(OFF)}$			150		
Fall Time	t_f			88		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$	-0.63	-1.0	V
			$T_J = 125^\circ\text{C}$	-0.50		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, d_{ISD}/d_t = 100\text{ A}/\mu\text{s}, I_S = -1.0\text{ A}$		26.1		ns
Charge Time	t_a			10.2		
Discharge Time	t_b			15.9		
Reverse Recovery Time	Q_{RR}			12		

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

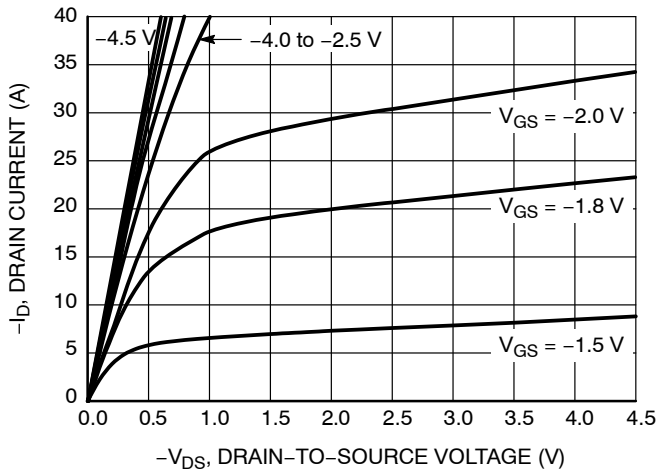


Figure 1. On-Region Characteristics

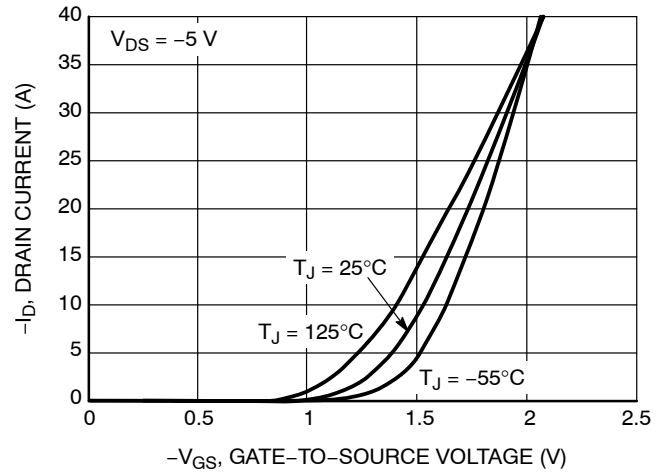


Figure 2. Transfer Characteristics

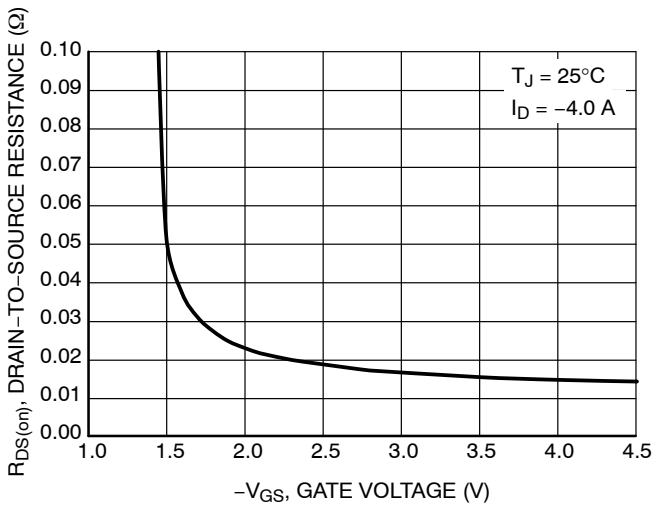


Figure 3. On-Resistance vs. Gate-to-Source Voltage

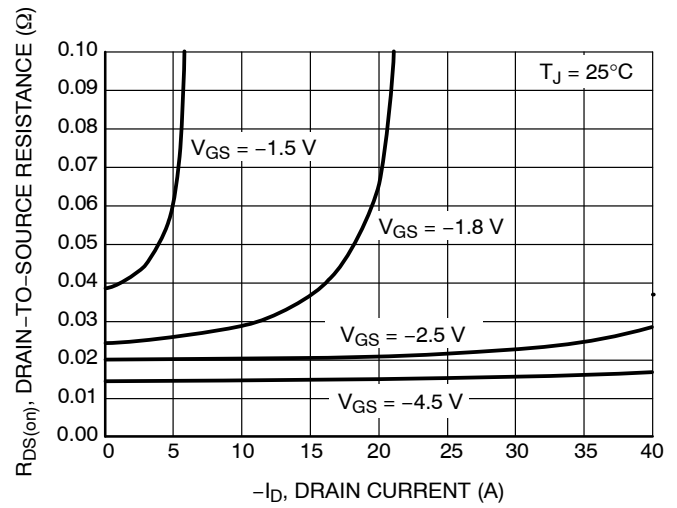


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

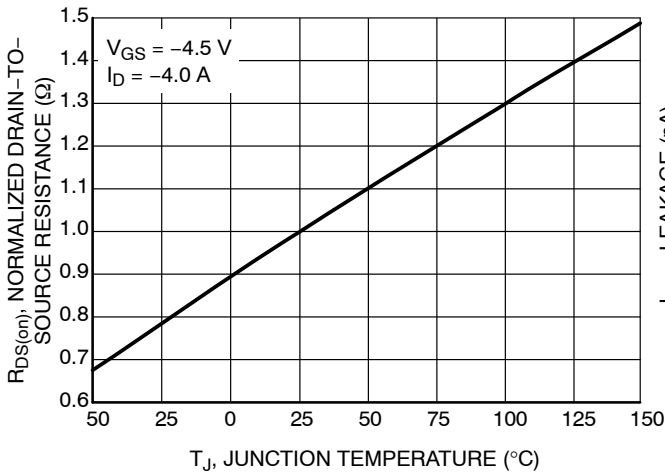


Figure 5. On-Resistance Variation with Temperature

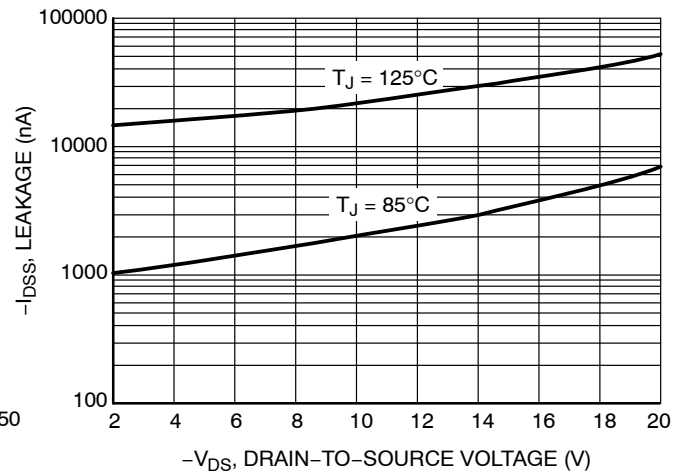


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

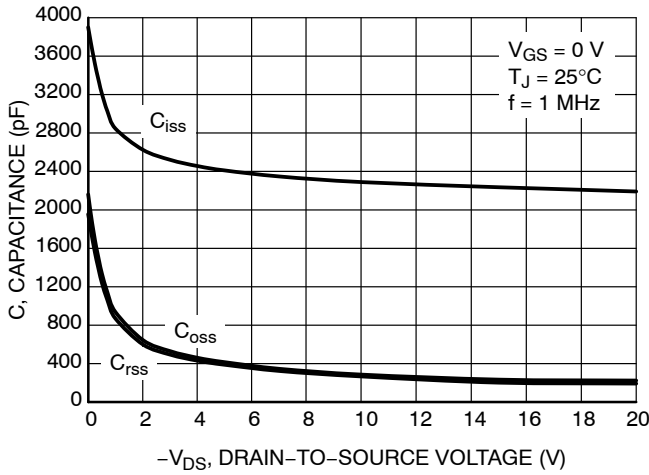


Figure 7. Capacitance Variation

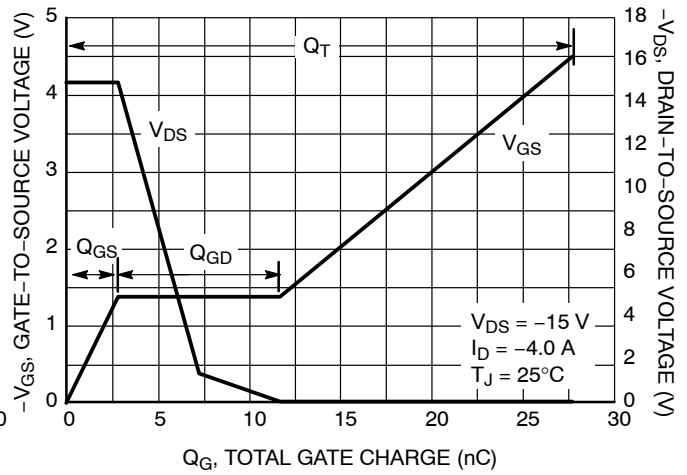


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

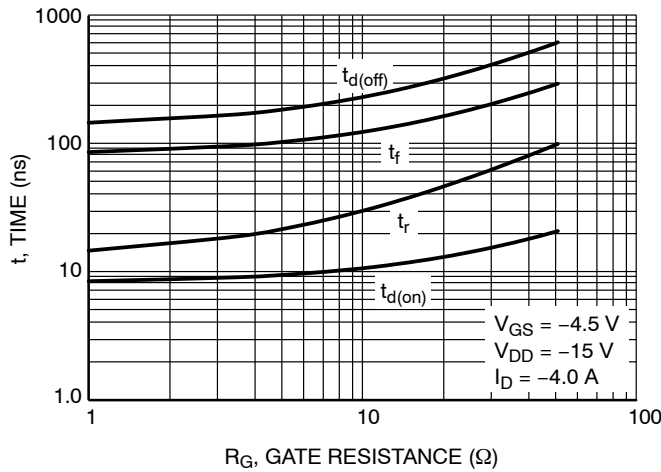


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

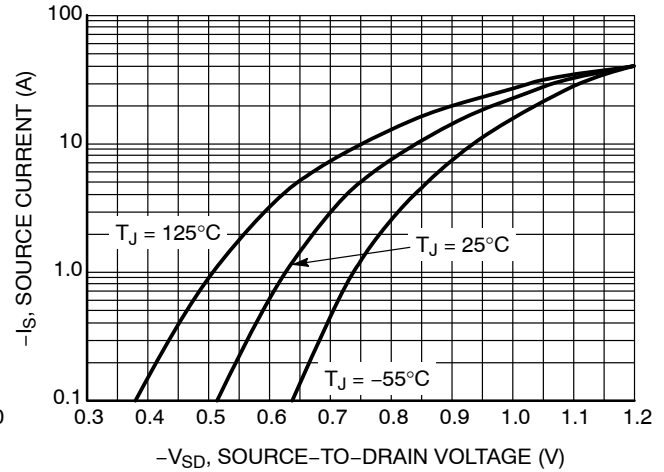


Figure 10. Diode Forward Voltage vs. Current

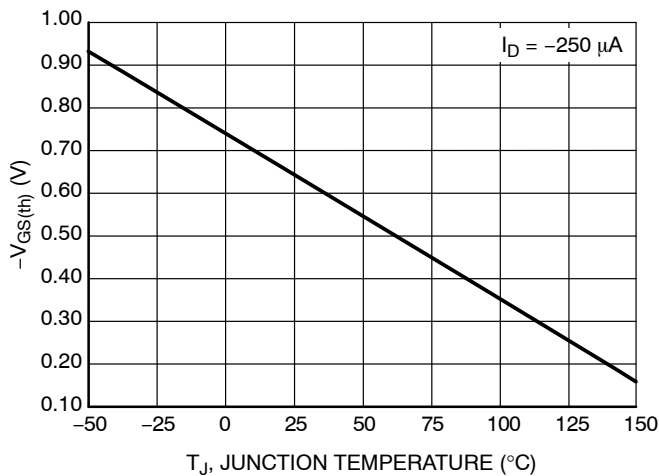


Figure 11. Threshold Voltage

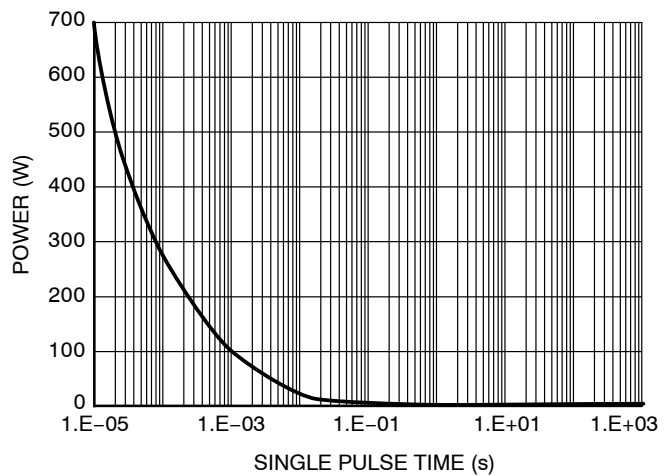


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

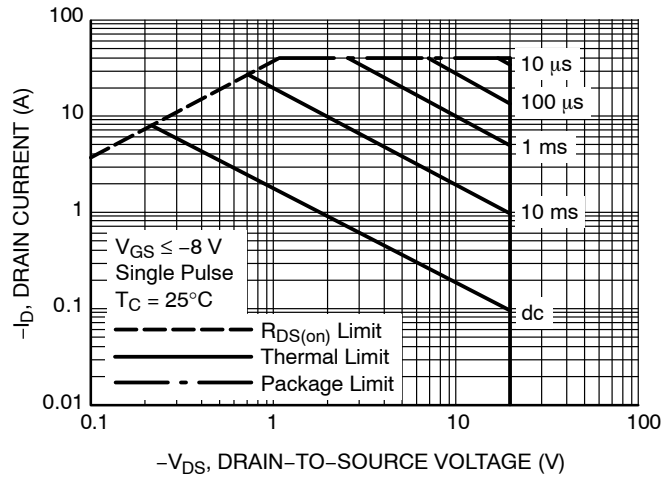


Figure 13. Maximum Rated Forward Biased Safe Operating Area

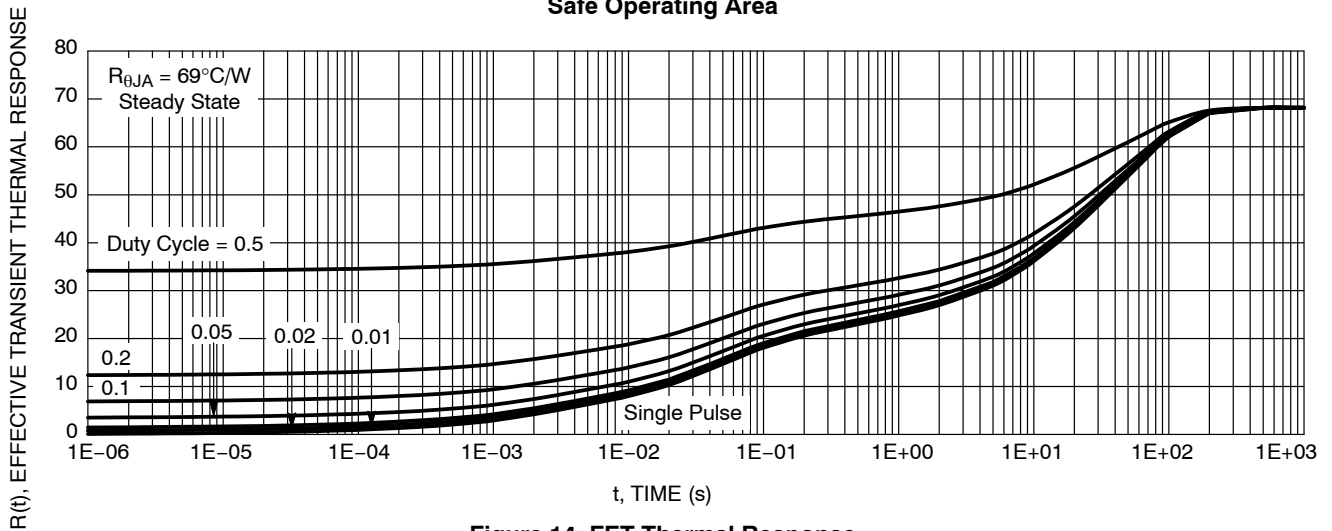
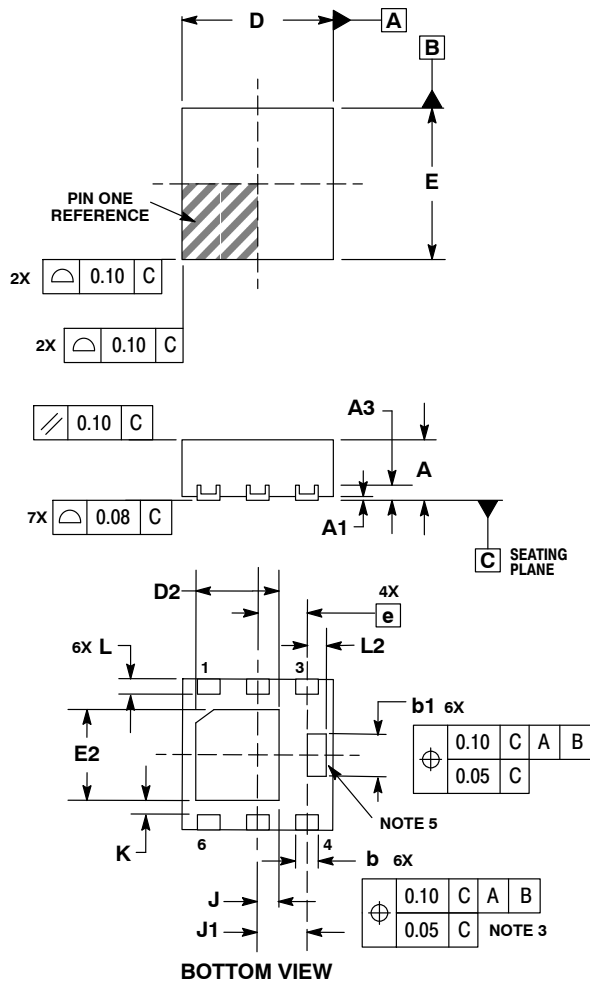


Figure 14. FET Thermal Response

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PACKAGE DIMENSIONS

WDFN6 CASE 506AP ISSUE B

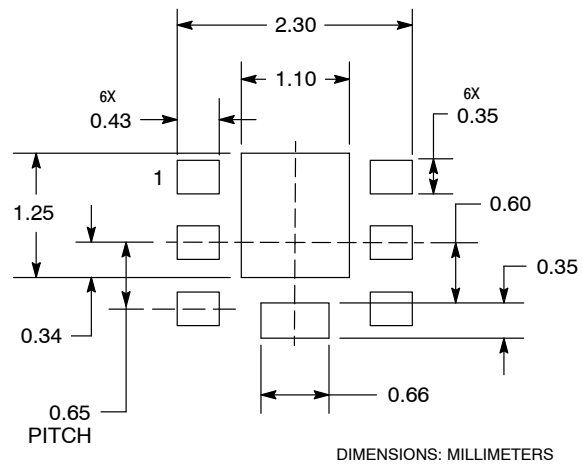


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT



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