NTMFS4982NF

Power MOSFET

30 V, 207 A, Single N−Channel, SO−8 FL

Features

- Integrated Schottky Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Server, Netcom, POL
- Synchronous Rectification for DC−DC Converters
- Low Side Switching
- High Performance Applications

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	36	A
		T_A = 85°C		26	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.7	W
Continuous Drain Current $R_{\theta JA}$ ≤ 10 sec		T_A = 25°C	I_D	60	A
		T_A = 85°C		43	
Power Dissipation $R_{\theta JA}$, t ≤ 10 sec		T_A = 25°C	P_D	7.4	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	26.5	A
		T_A = 85°C		19	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	1.5	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	207	A
		T_C = 85°C		149	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	89.3	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	350	A
Current limited by package		T_A = 25°C	$I_{Dmaxpkg}$	100	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	54	A
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 50 V, V_{GS} = 10 V, I_L = 50 A_{pk}, L = 0.1 mH, R_G = 25 Ω)			EAS	125	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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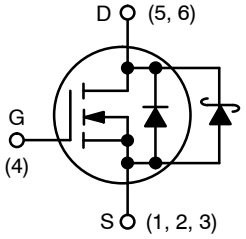
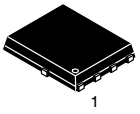
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	1.3 mΩ @ 10 V	207 A
	1.9 mΩ @ 4.5 V	

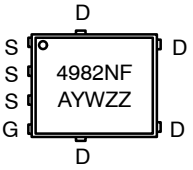
N−CHANNEL MOSFET





SO−8 FLAT LEAD CASE 488AA STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4982NFT1G	SO−8FL (Pb−Free)	1500 / Tape & Reel
NTMFS4982NFT3G	SO−8FL (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.4	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	46.6	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	84.1	
Junction−to−Ambient − t ≤ 10 sec	$R_{\theta JA}$	16.8	

1. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1.0 mA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 10 mA, referenced to 25°C			15		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			500	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 1.0 mA		1.0	1.7	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 10 mA, referenced to 25°C			5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 25 A		0.95	1.3	mΩ
		V_{GS} = 4.5 V	I_D = 25 A		1.4	1.9	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			60		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			6000		pF
Output Capacitance	C_{OSS}				2400		
Reverse Transfer Capacitance	C_{RSS}				160		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 25 A			40		nC
Threshold Gate Charge	$Q_{G(TH)}$				8.8		
Gate−to−Source Charge	Q_{GS}				15		
Gate−to−Drain Charge	Q_{GD}				12		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 25 A			84		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 25 A, R_G = 3 Ω			17.2		ns
Rise Time	t_r				31.6		
Turn−Off Delay Time	$t_{d(OFF)}$				34.3		
Fall Time	t_f				12		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 25 A, R_G = 3 Ω			12.7		ns
Rise Time	t_r				20.4		
Turn−Off Delay Time	$t_{d(OFF)}$				38.6		
Fall Time	t_f				11.3		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2 A	T_J = 25°C		0.4	0.7	V
			T_J = 125°C		0.32		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 25 A			58		ns
Charge Time	t_a				29		
Discharge Time	t_b				29		
Reverse Recovery Charge	Q_{RR}				71		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.65		nH
Drain Inductance	L_D				0.20		
Gate Inductance	L_G				1.5		
Gate Resistance	R_G				0.8		Ω

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

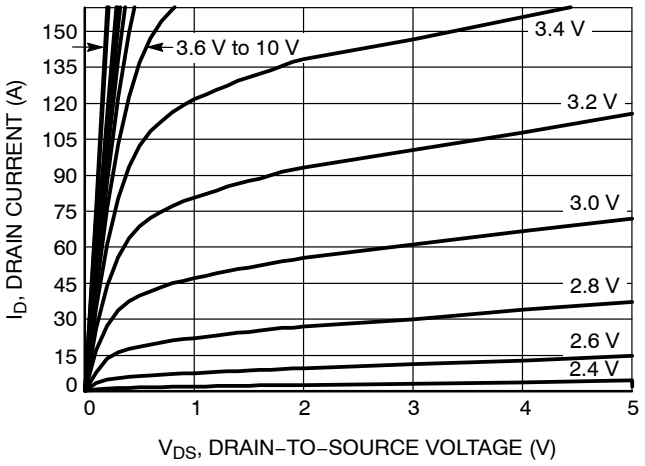


Figure 1. On−Region Characteristics

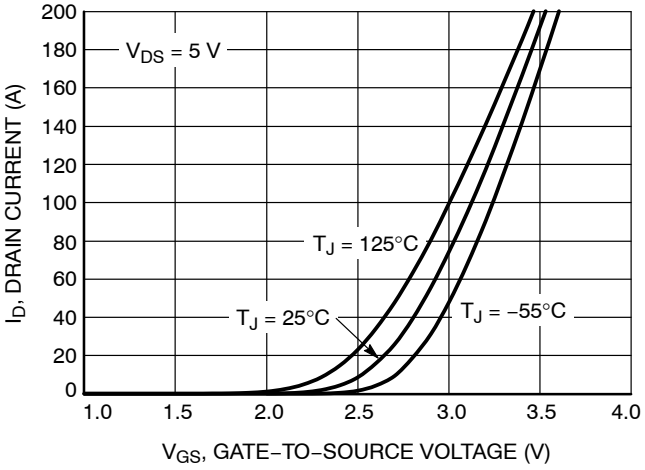


Figure 2. Transfer Characteristics

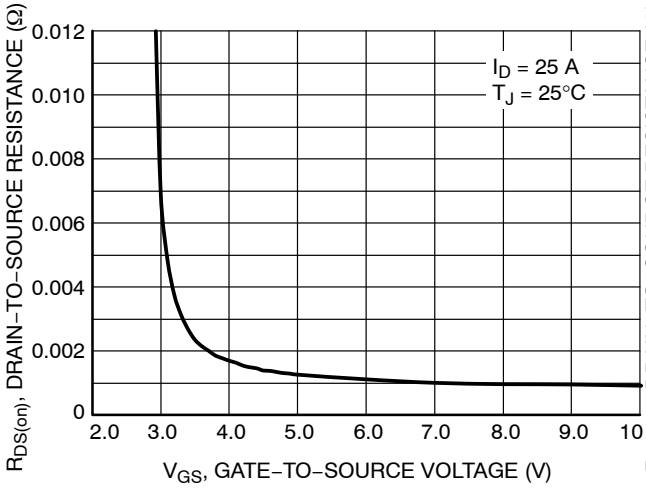


Figure 3. On−Resistance vs. V_{GS}

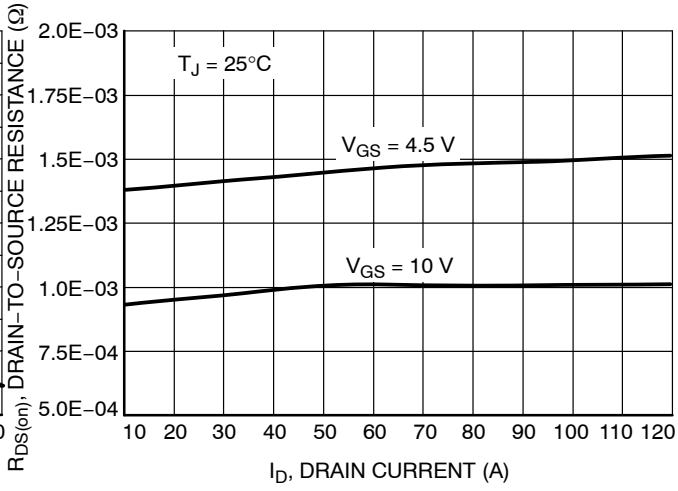


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

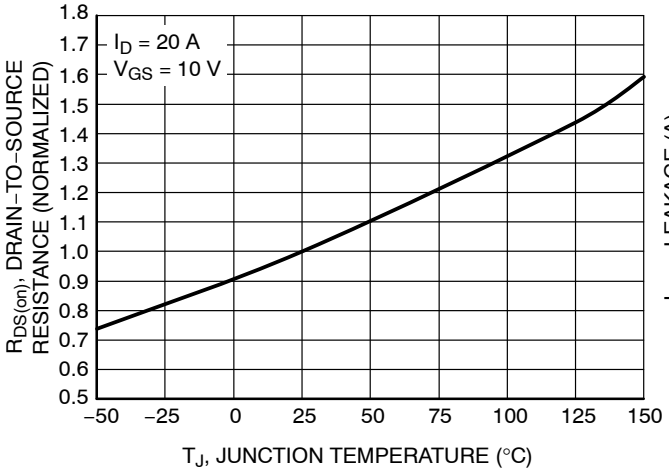


Figure 5. On−Resistance Variation with Temperature

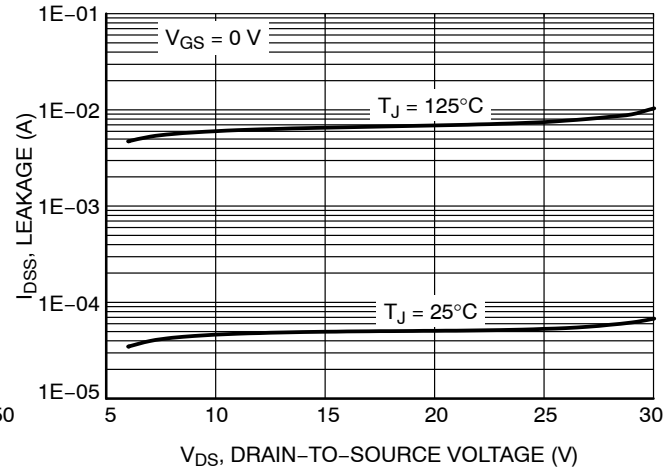


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

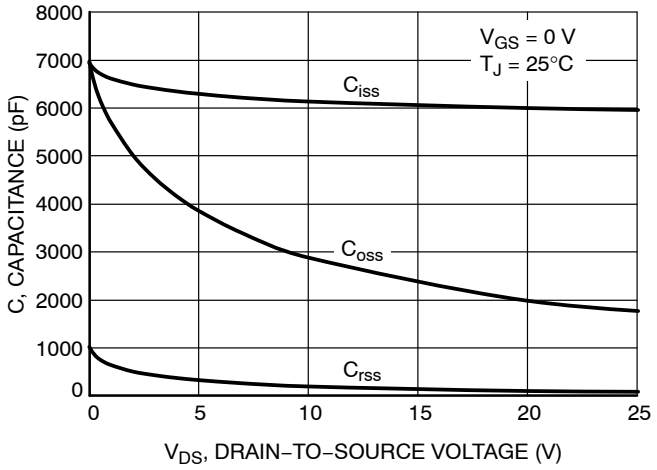


Figure 7. Capacitance Variation

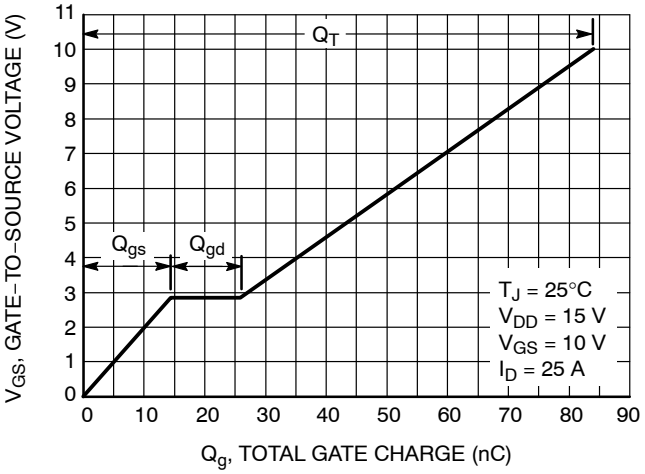


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

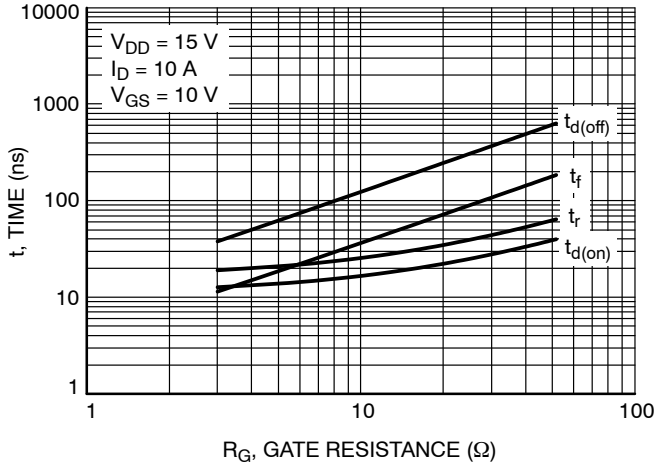


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

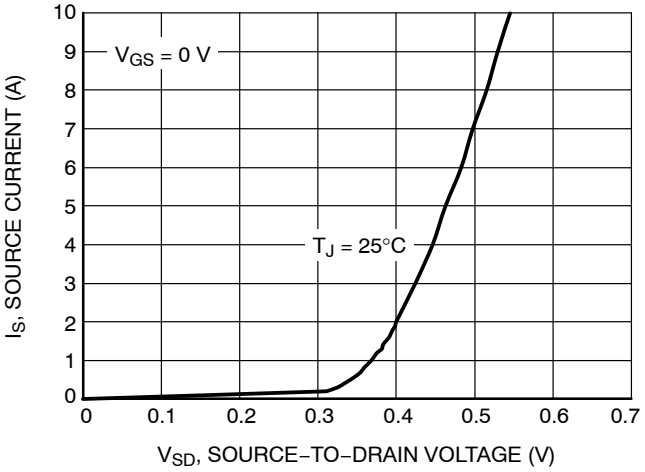


Figure 10. Diode Forward Voltage vs. Current

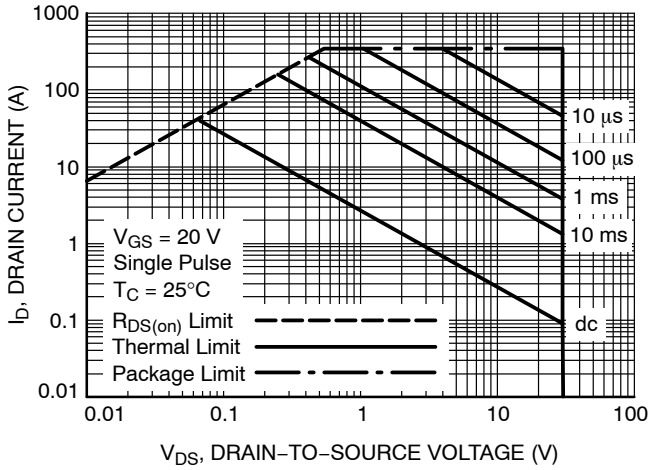


Figure 11. Maximum Rated Forward Biased Safe Operating Area

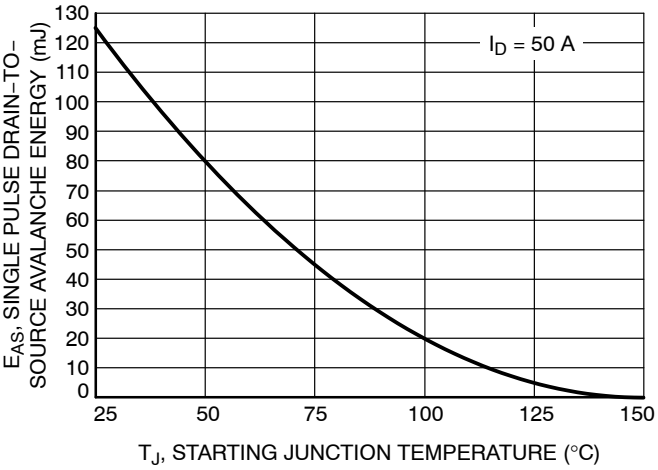


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

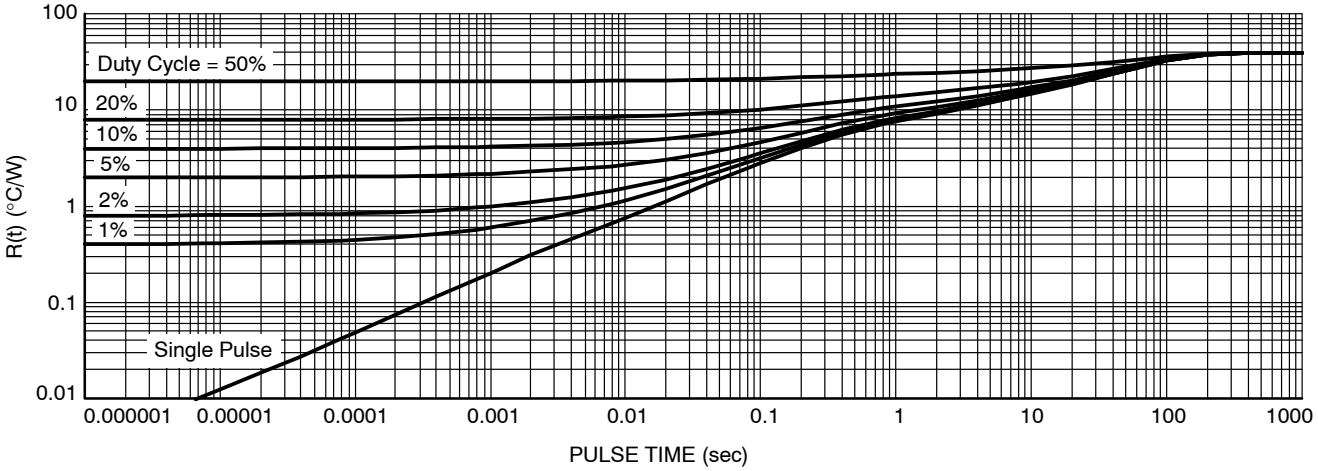
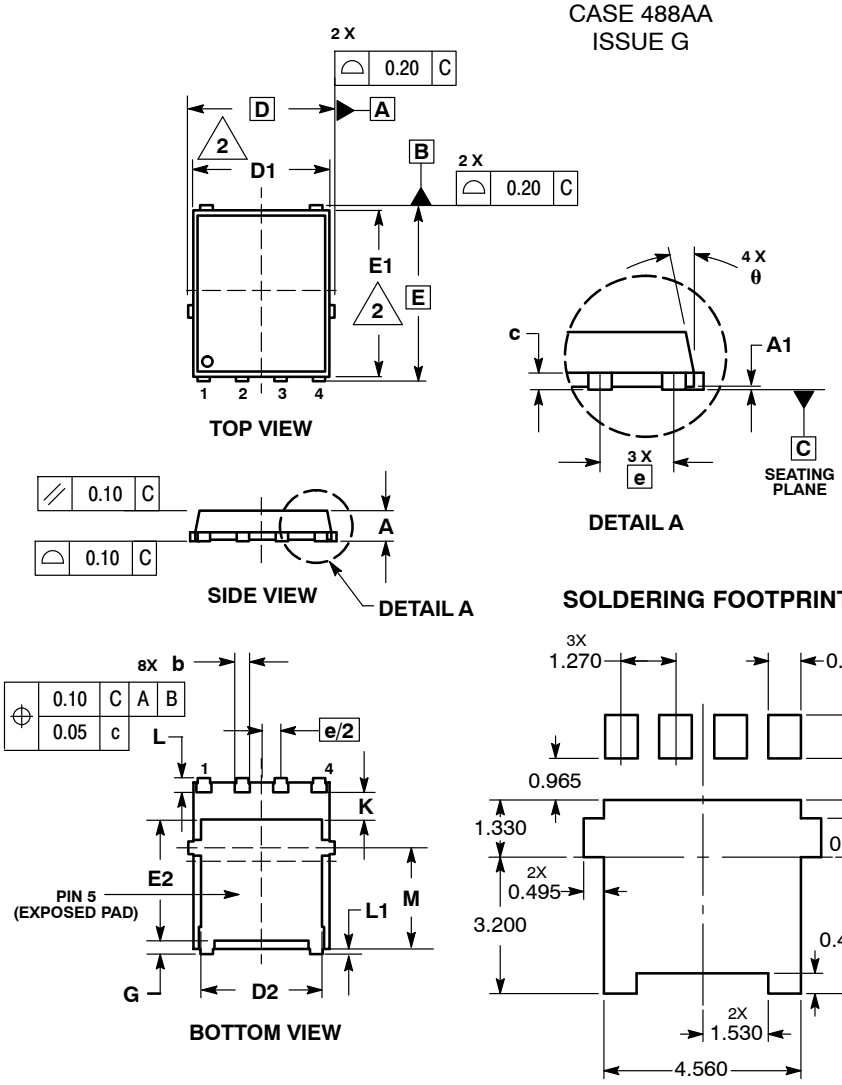


Figure 13. Thermal Response

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.50	4.90	5.10
D2	3.50	–––	4.22
E		6.15 BSC	
E1	5.50	5.80	6.10
E2	3.45	–––	4.30
e		1.27 BSC	
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	–––	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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