

NVMFD5852NL, NVMFD5852NLWF

Power MOSFET

40 V, 6.9 mΩ, 44 A, Dual N-Channel Logic Level, Dual SO-8FL

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5852NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DS}	40	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^\circ\text{C}$	44	A
		$T_{mb} = 100^\circ\text{C}$	31	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State	$T_{mb} = 25^\circ\text{C}$	27	W
		$T_{mb} = 100^\circ\text{C}$	13	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State	$T_A = 25^\circ\text{C}$	15	A
		$T_A = 100^\circ\text{C}$	10.6	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)	Steady State	$T_A = 25^\circ\text{C}$	3.2	W
		$T_A = 100^\circ\text{C}$	1.6	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	329	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	40	A	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 40 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	80	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	5.6	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

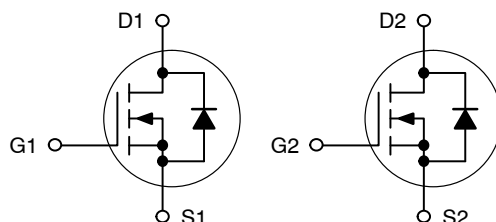


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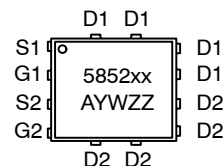
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	6.9 mΩ @ 10 V	44 A
	12.0 mΩ @ 4.5 V	

Dual N-Channel



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



5852NL = Specific Device Code for NVMFD5852NL
 5852LW = Specific Device Code for NVMFD5852NLWF
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5852NLT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5852NLWFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			37.3		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		1.0	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.4		2.4	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			6.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		5.3	6.9	mΩ
		V _{GS} = 4.5 V, I _D = 20 A		8.7	12	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 5 A		24		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		1800		pF
Output Capacitance	C _{oss}			240		
Reverse Transfer Capacitance	C _{rss}			180		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 32 V, I _D = 20 A		20		nC
Threshold Gate Charge	Q _{G(TH)}			1.5		
Gate-to-Source Charge	Q _{GS}			5.5		
Gate-to-Drain Charge	Q _{GD}			10.9		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32V, I _D = 20 A		36		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DS} = 32 V, I _D = 20 A, R _G = 2.5 Ω		12		ns
Rise Time	t _r			52		
Turn-Off Delay Time	t _{d(off)}			21		
Fall Time	t _f			13		
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 20 A, R _G = 2.5 Ω		12		ns
Rise Time	t _r			8.0		
Turn-Off Delay Time	t _{d(off)}			27		
Fall Time	t _f			5.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 20 A	T _J = 25°C		0.84	1.1	V
			T _J = 125°C		0.69		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, d _{IS} /d _t = 100 A/μs, I _S = 20 A		22.3		ns	
Charge Time	t _a			12.8			
Discharge Time	t _b			9.4			
Reverse Recovery Charge	Q _{RR}			15.2			nC

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

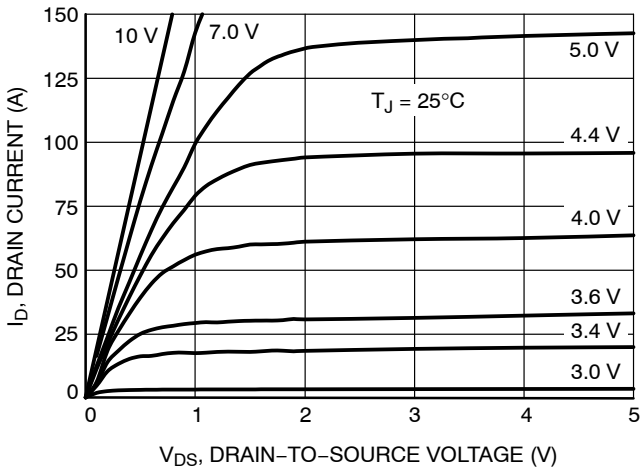


Figure 1. On-Region Characteristics

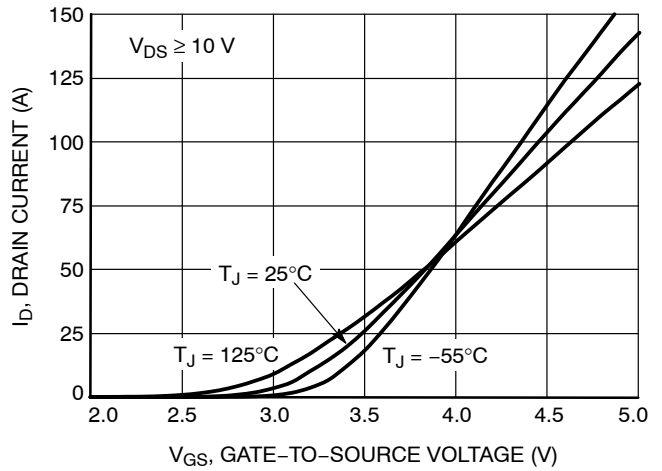


Figure 2. Transfer Characteristics

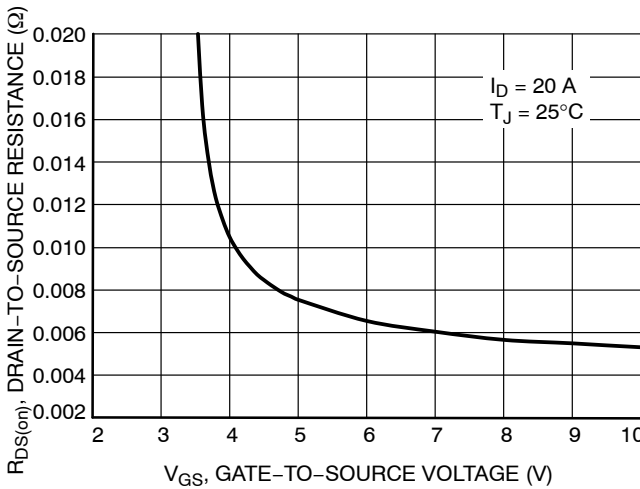


Figure 3. On-Resistance vs. V_{GS}

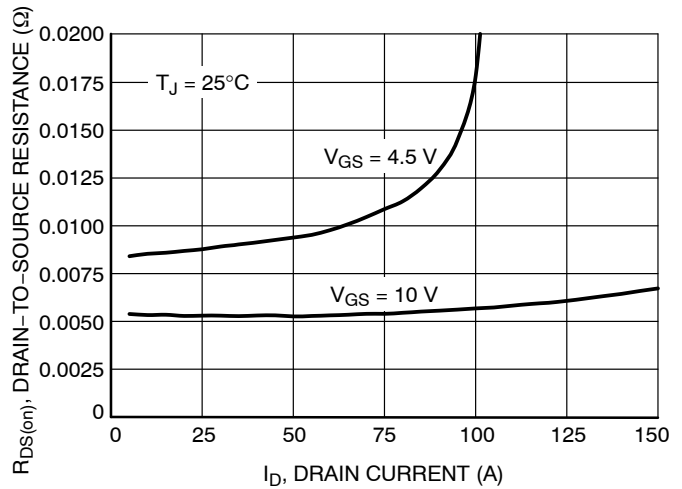


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

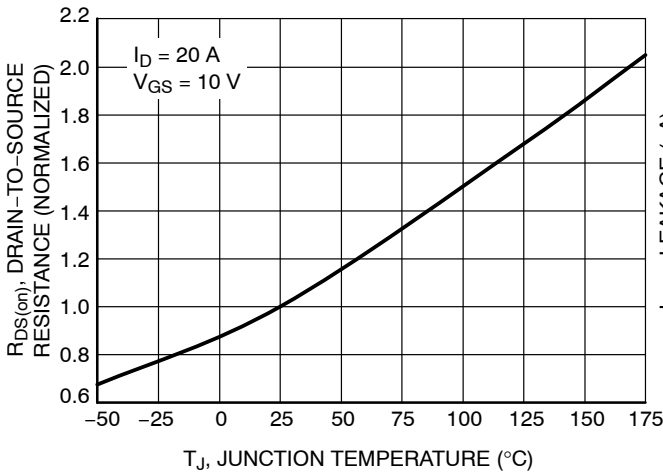


Figure 5. On-Resistance Variation with Temperature

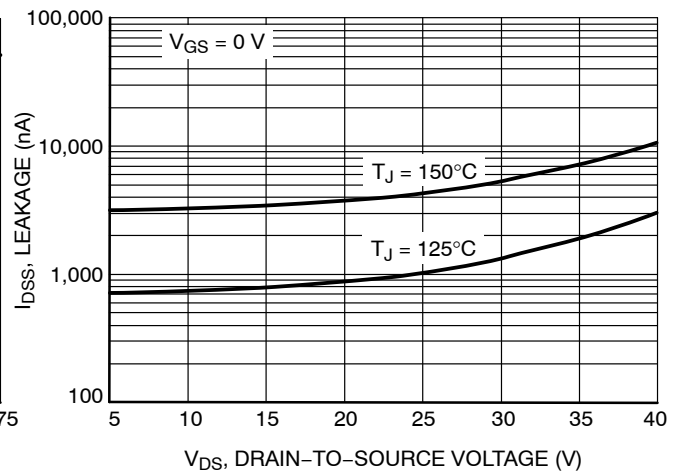


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

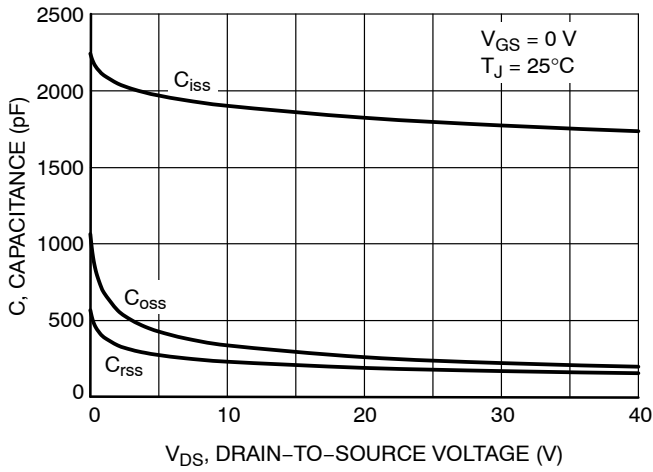


Figure 7. Capacitance Variation

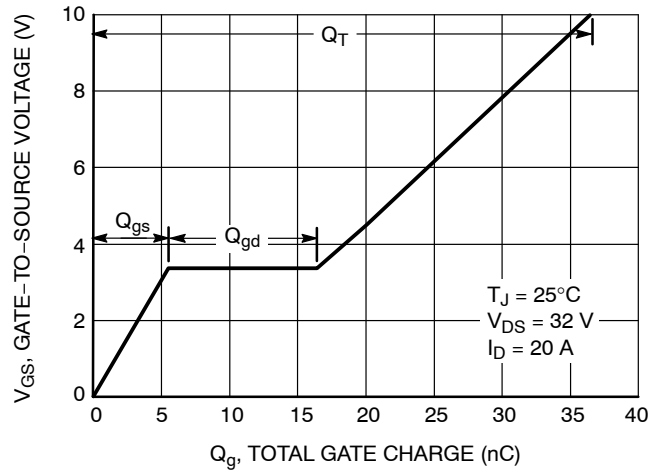


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

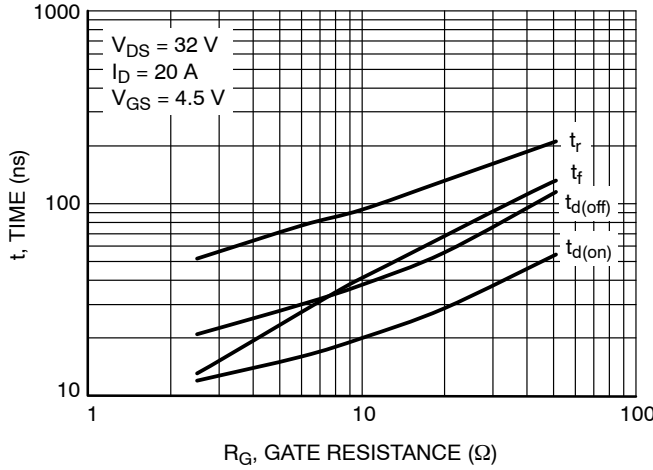


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

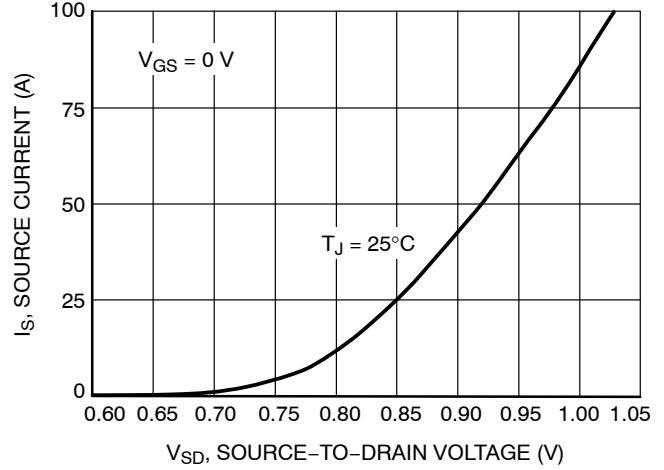


Figure 10. Diode Forward Voltage vs. Current

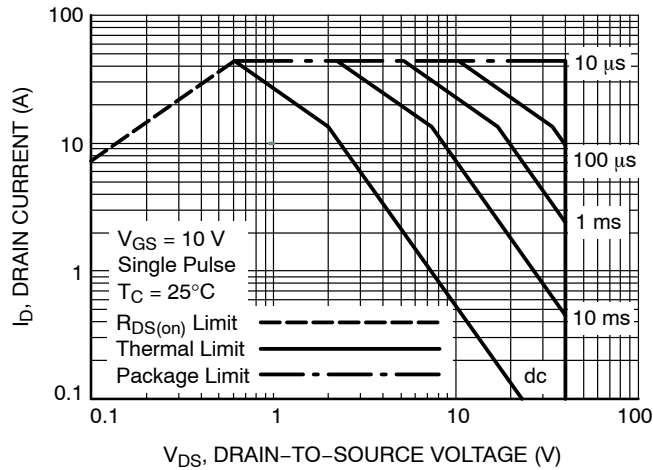


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

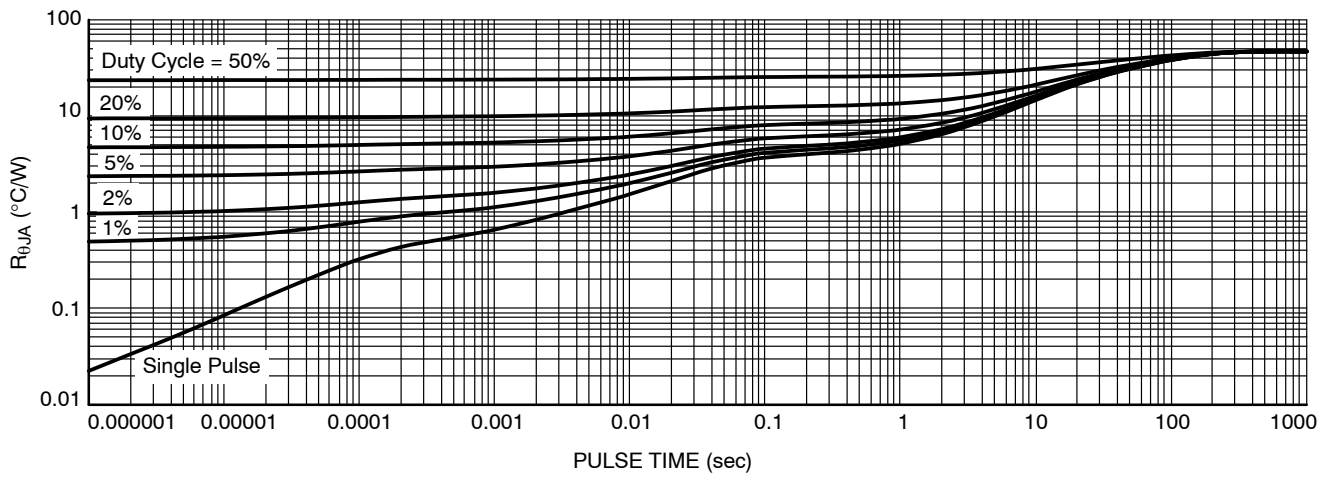


Figure 12. Thermal Response

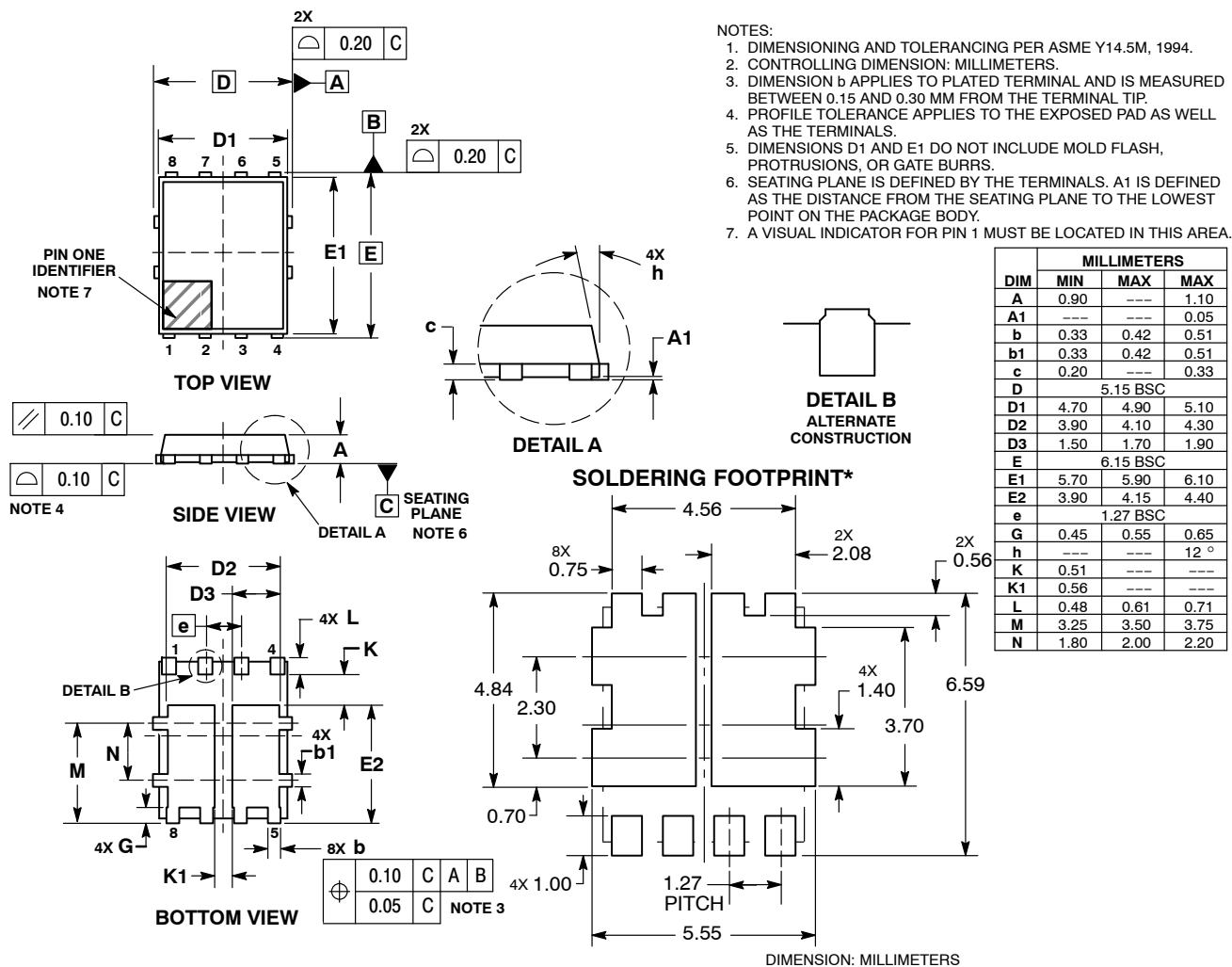
NVMFD5852NL, NVMFD5852NLWF

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT

ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
 4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
 7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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