



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## TND323VD — ExPD (Excellent Power Device) General Purpose Driver for PDP Sustain Pulse Drive, Motor Drive, Switching Power Supply, and DC / DC Converter Applications

### Features

- Inverter buffer
- Monolithic structure (High voltage CMOS process adopted)
- Withstand voltage of 25V is assured
- Wide range of operating voltage : 4.5V to 25V
- Peak output current :  $I_{O+}/I_{O-}=0.8A/1A$
- Fast switching time (30ns typical at 1000pF load)
- Fully compatible input to TTL / CMOS ( $V_{IH}$ =up to 2.6V, at  $V_{DD}$ =4.5 to 25V)
- Built-in input pull-down resistance

### Specifications

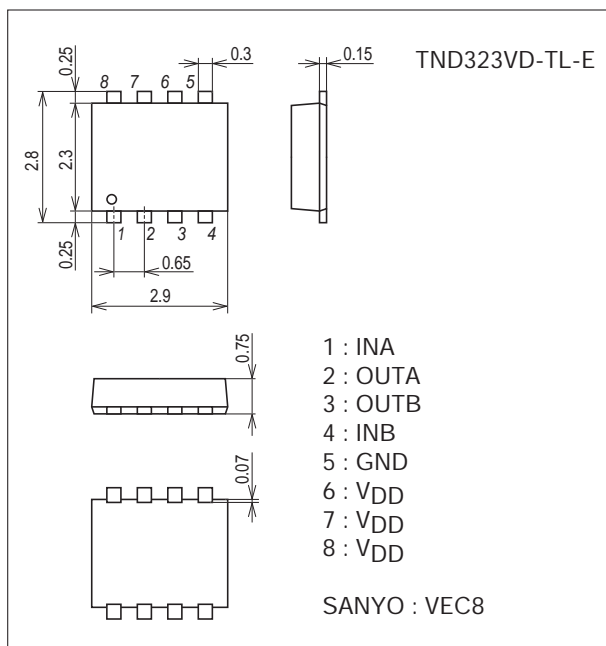
Absolute Maximum Ratings at  $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	$V_{DD}$		0 to 25	V
Input Voltage	$V_{IN}$		$GND-0.3$ to $V_{DD}+0.3$	V
Allowable Power Dissipation	$P_D$ max		0.2	W
Junction Temperature	$T_j$		-55 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

### Package Dimensions

unit : mm (typ)

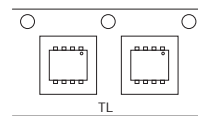
7012-006



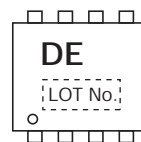
### Product & Package Information

- Package : VEC8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

### Packing Type : TL



### Marking



# TND323VD

## Recommend Operating Conditions at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Operating Supply Voltage	V <sub>DD</sub>		4.5 to 25	V
Operating Temperature	Topr		-40 to +125	°C

## Electrical Characteristics (AC Characteristics) at Ta=25°C, V<sub>DD</sub>=18V, V<sub>IN</sub>=5V

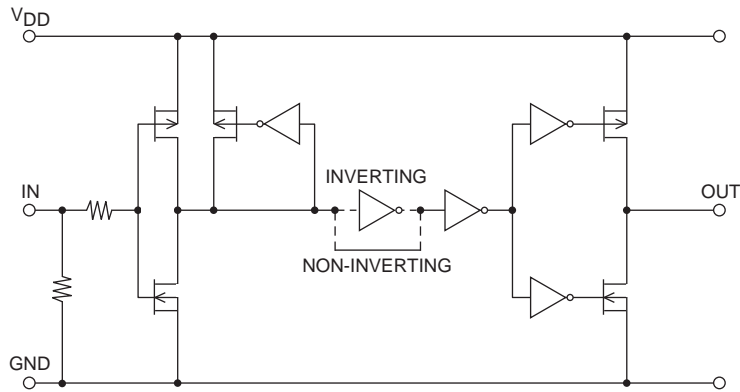
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Turn-On Rise Time	t <sub>r</sub>	C <sub>L</sub> =1000pF		35	50	ns
Turn-Off Fall Time	t <sub>f</sub>	C <sub>L</sub> =1000pF		30	45	ns
Delay Time	t <sub>D1</sub>	C <sub>L</sub> =1000pF		30	45	ns
	t <sub>D2</sub>	C <sub>L</sub> =1000pF		45	60	ns

## Electrical Characteristics (DC Characteristics) at Ta=25°C, V<sub>DD</sub>=4.5 to 25V

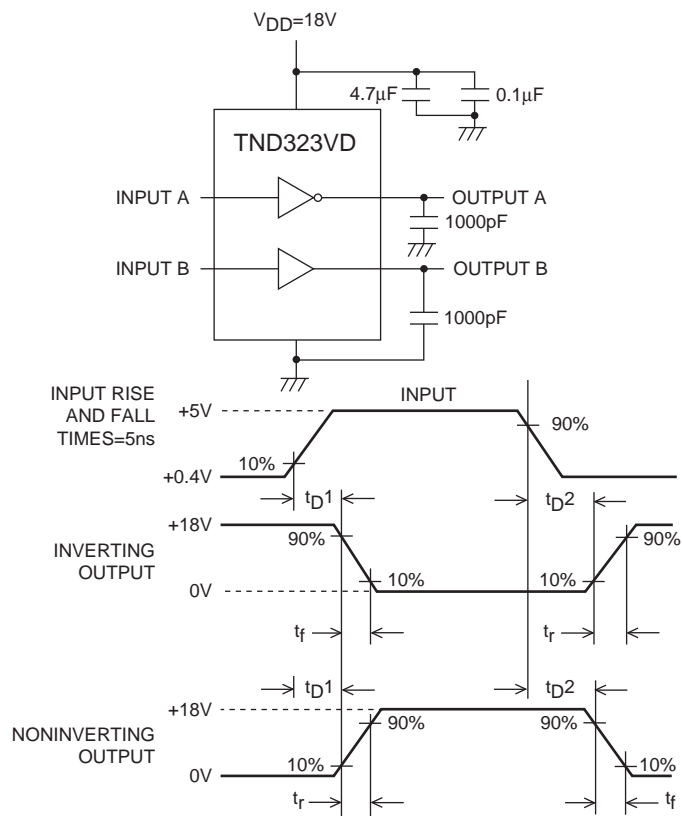
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic "1" Input Voltage	V <sub>IH</sub>		2.6			V
Logic "0" Input Voltage	V <sub>IL</sub>				0.8	V
Logic "1" Input Bias Current	I <sub>IN+</sub>	V <sub>IN</sub> =V <sub>DD</sub> =25V		40	100	μA
Logic "0" Input Bias Current	I <sub>IN-</sub>	V <sub>IN</sub> =0V	-1		1	μA
High-level Output Voltage	V <sub>OH</sub>	I <sub>O</sub> =0A	V <sub>DD</sub> -0.1			V
Low-level Output Voltage	V <sub>OL</sub>	I <sub>O</sub> =0A			0.1	V
V <sub>DD</sub> Supply Current	I <sub>supp</sub>	V <sub>DD</sub> =10V, V <sub>IN</sub> =3V, (both inputs)		1.0	4.5	mA
		V <sub>DD</sub> =10V, V <sub>IN</sub> =0V, (both inputs)			0.2	mA
Output High Short Circuit Pulsed Current	I <sub>O+</sub>	V <sub>DD</sub> =18V, PW≤10μs, V <sub>OUT</sub> =0V		0.8		A
Output Low Short Circuit Pulsed Current	I <sub>O-</sub>	V <sub>DD</sub> =18V, PW≤10μs, V <sub>OUT</sub> =18V		1.0		A
Output On Resistance	R <sub>OUT</sub>	V <sub>DD</sub> =18V, I <sub>load</sub> =10mA, V <sub>OUT</sub> ="H"		11	16.5	Ω
		V <sub>DD</sub> =18V, I <sub>load</sub> =10mA, V <sub>OUT</sub> ="L"		6	10	Ω

# TND323VD

## Block Diagram



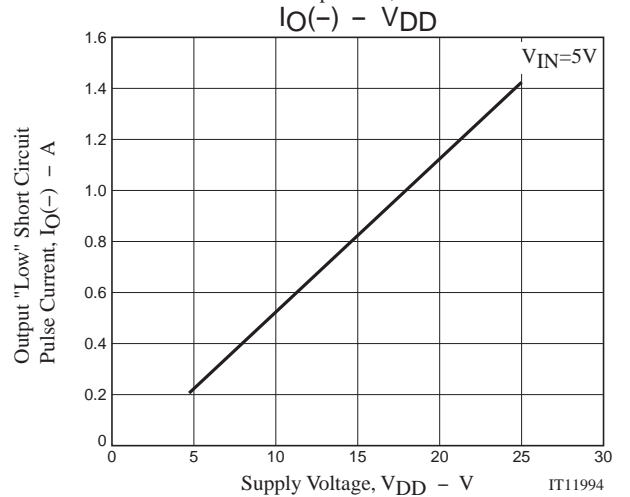
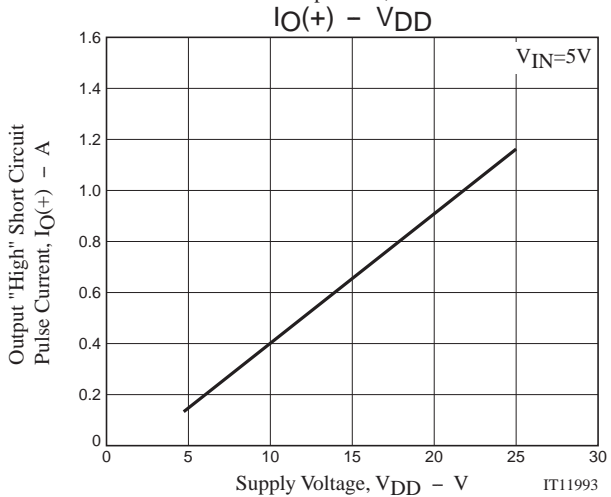
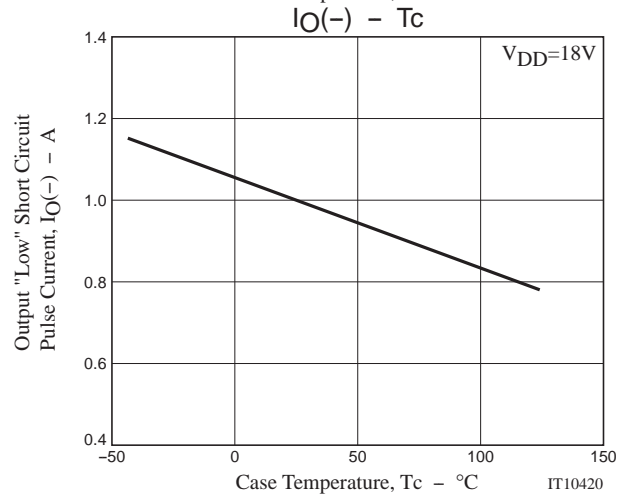
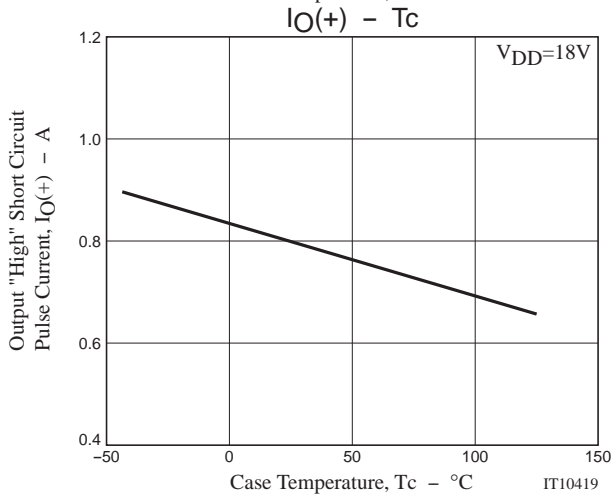
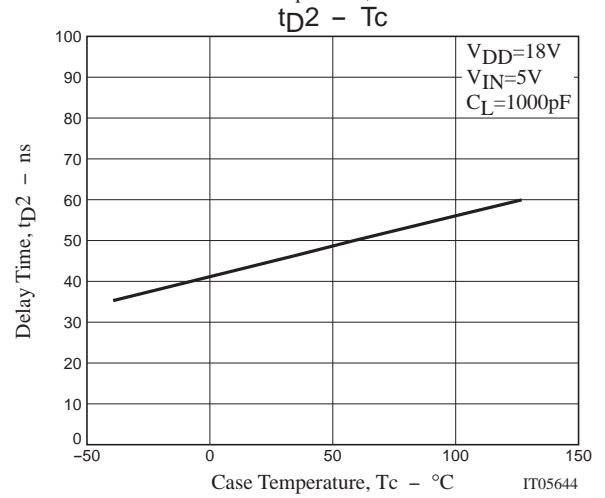
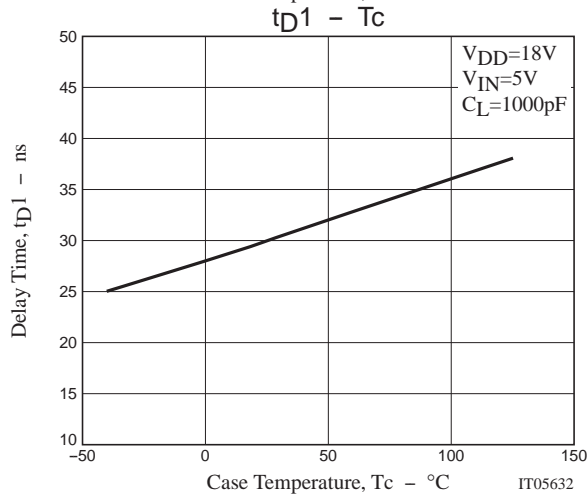
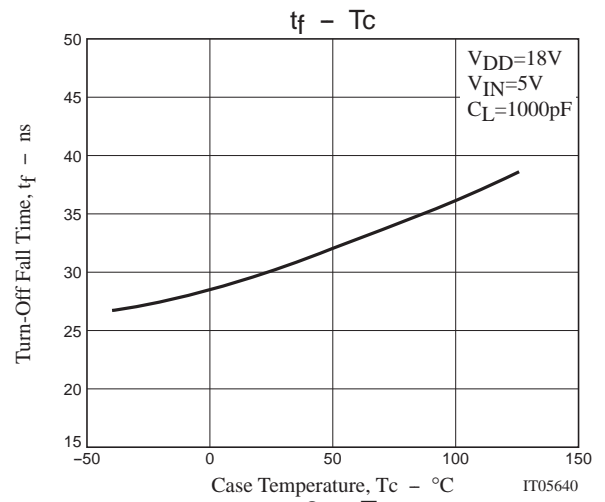
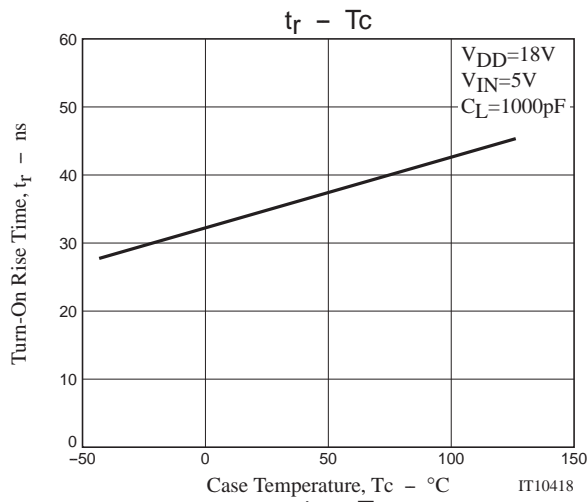
## Switching Time Test Circuit



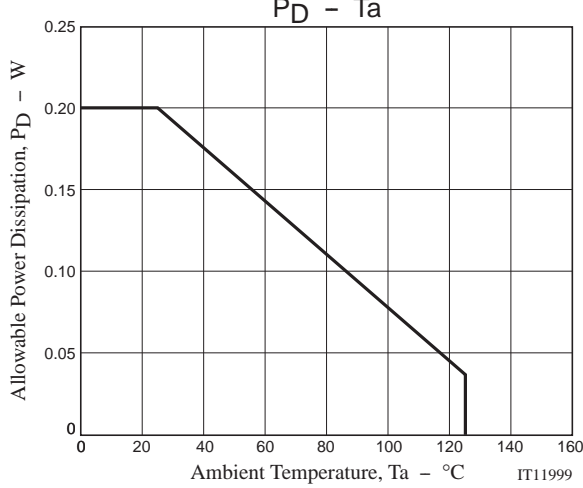
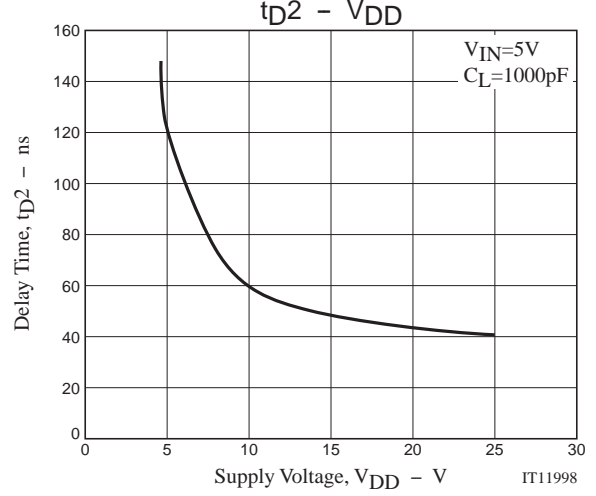
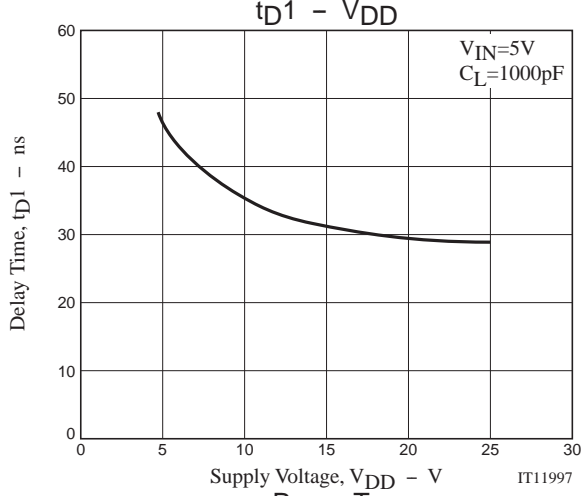
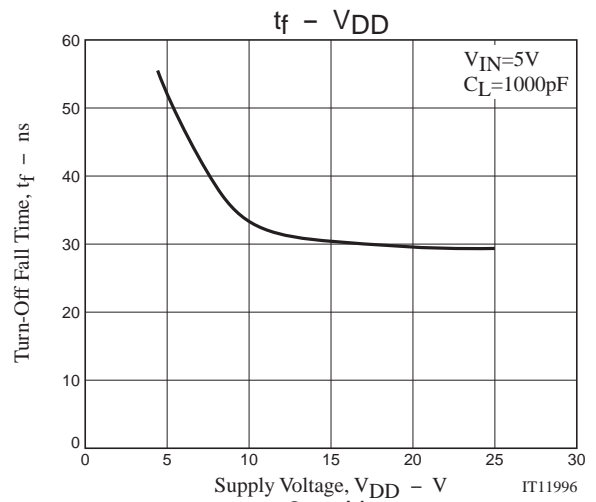
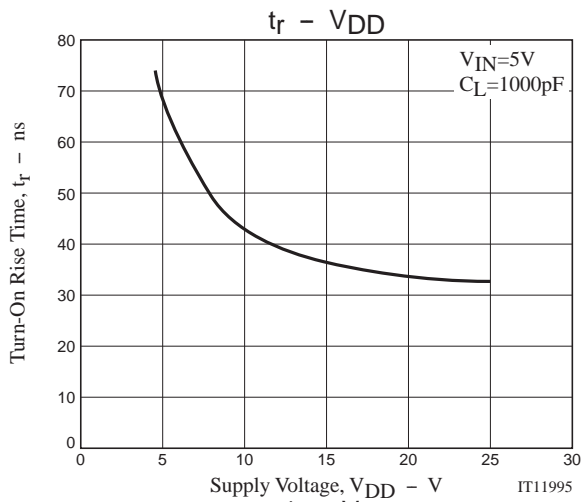
## Ordering Information

Device	Package	Shipping	memo
TND323VD-TL-E	VEC8	3,000pcs./reel	Pb Free

# TND323VD



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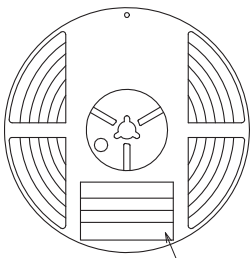
## Taping Specification

TND323VD-TL-E

### 1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1) Dimensions:mm (external) 183×72×185	Outer BOX (A-7) Dimensions:mm (external) 440×195×210
VEC8	CPH6	3,000	15,000	90,000	5 reels contained	6 inner boxes contained

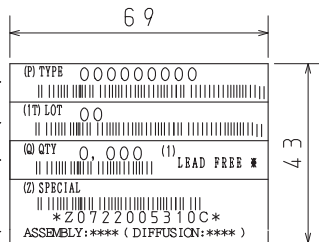
#### Packing method



Reel label

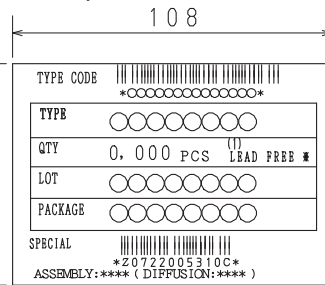
Type No.  
LOT No.  
Quantity  
Origin

Reel label, Inner box label  
(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



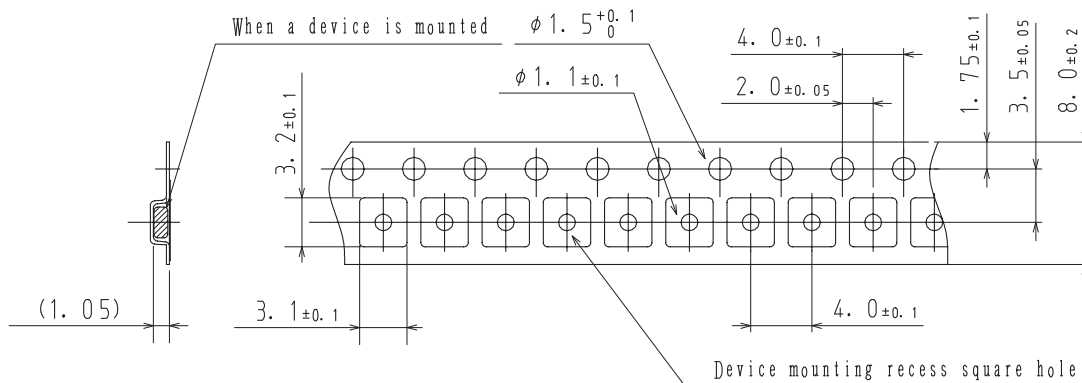
#### NOTE (1)

The LEAD FREE \* description shows that the surface treatment of the terminal is lead free.

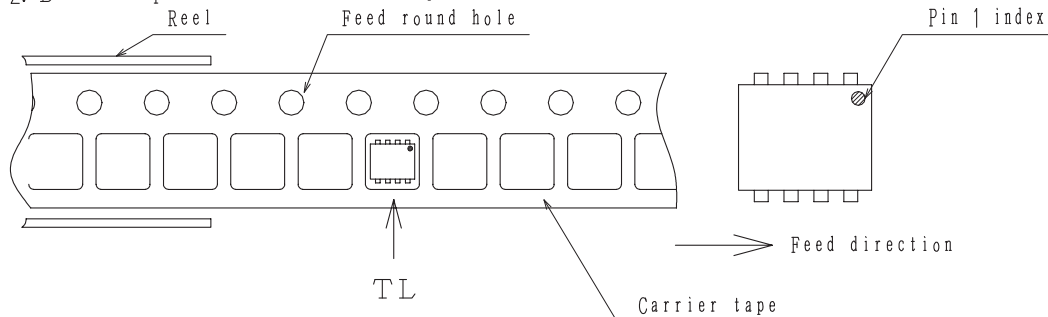
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

### 2. Taping configuration

#### 2-1. Carrier tape size (unit:mm)



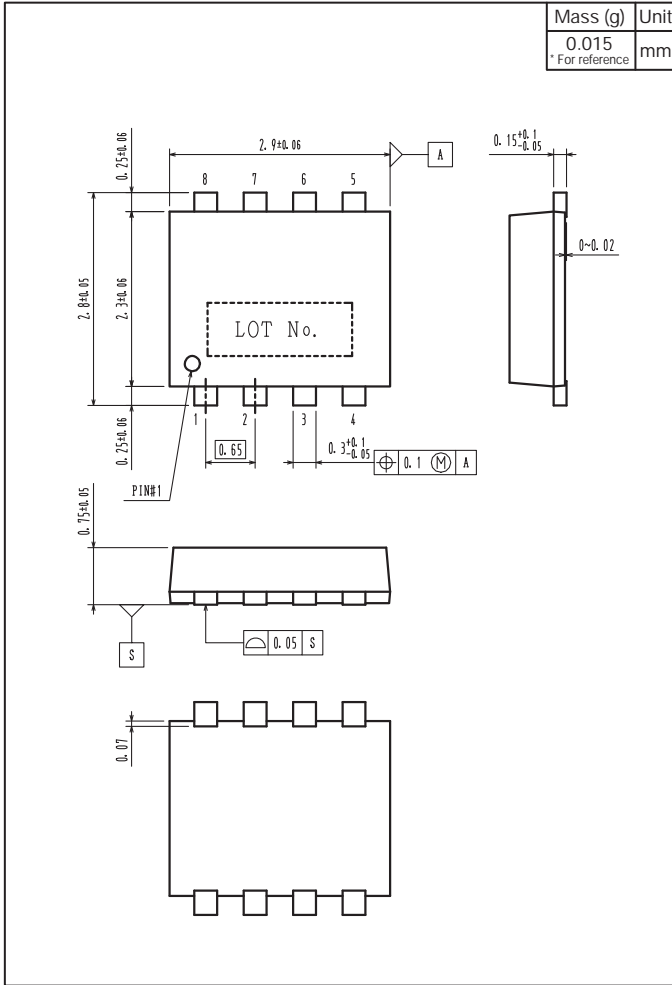
#### 2-2. Device placement direction



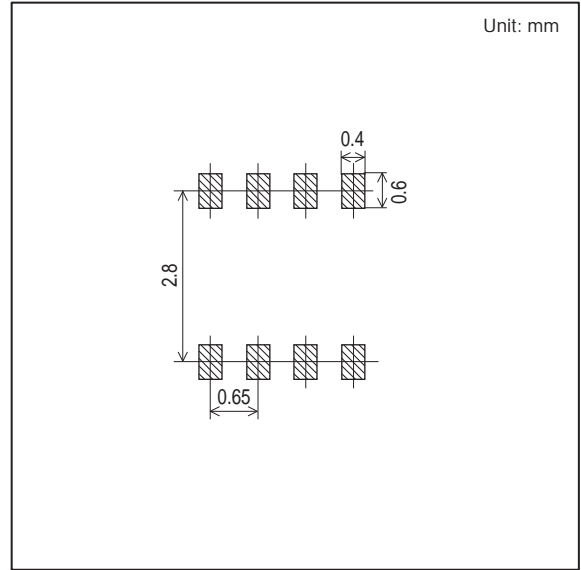
Those with oen electrode terminal on the feed hole side.....TL

# TND323VD

## Outline Drawing TND323VD-TL-E



## Land Pattern Example



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