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FPM2750QFN

LOW-NOISE HIGH-LINEARITY BALANCED AMPLIFIER MODULE

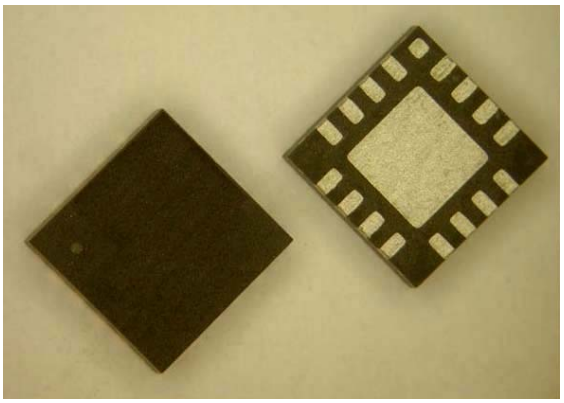
Package: 4mmx4mm QFN

Product Description

The FPM2750QFN is a packaged pair of transistors (pHEMT) specifically optimized for balanced configuration systems. Our 0.25µm process ensures class-leading noise performance. The use of a small footprint plastic package allows for a cost effective total system implementation.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



Features

- Balanced Low Noise Amplifier Module
- Excellent Noise figure: 0.4dB at 1850MHz
- Low Drive Current: 40mA (3.0V)
- Combined IP3: 36dBm (100mA)
- Combined P1dB: 23dBm (100mA)

Applications

- Wireless Infrastructure: Tower-Mounted Amplifiers and Front End LNAs for EGSM/PCS/WCDMA/UMTS Base Stations
- High Intercept-Point LNAs

RF/DC Parameter	Electrical Specification			Unit	Condition
	Min.	Typ.	Max.		
Noise Figure (NF)		0.4		dB	V_{DS}=3V, I_{DS}=40mA
		0.6		dB	V_{DS}=4V, I_{DS}=100mA
OIP_3 (15dB to 5dB below P_{1dB})		32		dBm	V_{DS}=3V, I_{DS}=40mA
	33	36		dBm	V_{DS}=4V, I_{DS}=100mA
Small-Signal Gain in Balanced Mode		18.5		dB	V_{DS}=3V, I_{DS}=40mA
	17.5	20		dB	V_{DS}=4V, I_{DS}=100mA
P_{1dB} in Balanced Mode		21		dBm	V_{DS}=3V, I_{DS}=40mA
	21.5	23.5		dBm	V_{DS}=4V, I_{DS}=100mA
Small-Signal Gain (SSG)		19.0		dB	V_{DS}=3V, I_{DS}=40mA
		19.5		dB	V_{DS}=4V, I_{DS}=100mA
OP_{1dB} at Gain Compression		17.5		dBm	V_{DS}=3V, I_{DS}=40mA
		17.5		dBm	V_{DS}=4V, I_{DS}=100mA
Saturated Drain-Source Current (I_{DSS})	185	230	280	mA	V_{DS}=1.3V, V_{GS}=0V
Maximum Drain-Source Current (I_{MAX})		375		mA	V_{DS}=1.3V, V_{GS}≅+1V
Transconductance (GM)		200		ms	V_{DS}=1.3V, V_{GS}=0V
Gate-Source Leakage Current (I_{GSO})				µA	V_{GS}=-5V
Pinch-Off Voltage (V_P)	|0.7|	|1.0|	|1.3|	V	V_{DS}=1.3V, I_{DS}=0.75mA
Gate-Source Breakdown Vltg (V_{BDGS})		|16|		V	I_{GS}=0.75mA
Gate-Drain Breakdown Vltg (V_{BDGD})		|18|		V	I_{DS}=0.75mA
Thermal Resistivity (θJC) *		124		°C/W	1W dissipation, case temperature 22°C

*Note: RF specification measured at f=1850MHz using CW signal (except as noted). $T_{AMBIENT}$=22°C.

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Absolute Maximum Ratings (per Transistor)[1]

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS})	6	V
Gate-Source Voltage (V_{GS})	-3	V
Drain-Source Current (I_{DS}) (V_{DS}<2V)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	7.5	mA
RF Input Power (P_{IN})[2] (Under any acceptable bias state)	150	mW
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-55 to 150	°C
Total Power Dissipation (P_{TOT})[3]	1	W
Gain Compression (Under bias conditions)	5	dB

Notes: [1]$T_{AMBIENT}$=22 °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2]Max. RF input limit must be further limited if input VSWR>2.5:1.
[3]Total Power Dissipation (P_{TOT}) defined as (P_{DC}+P_{IN})–P_{OUT}, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
Total Power Dissipation to be de-rated as follows above 22 °C:
P_{TOT}=(150-T_{CASE})/θJC, where T_{CASE}=temperature of the thermal pad on the underside of the package.
θJC increases linearly from 124 °C/W at a T_{CASE} of 22 °C to 145 °C/W at a T_{CASE} of 145 °C. (Coefficient of de-rating formula is Thermal Conductivity.)
Information on the mounting of QFN-style packages for optimum thermal performance is available on request.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Biasing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-biased or dual-biased circuits. Such circuits should include provisions to ensure that gate bias is applied before drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices used in the FPM2750QFN.

For standard Class A operation, a 50% I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Class A/B bias of 25% to 33% offers an optimized solution for NF and OIP_3.

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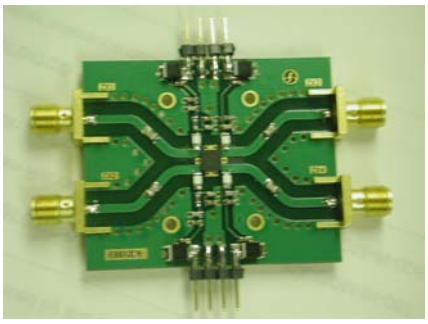
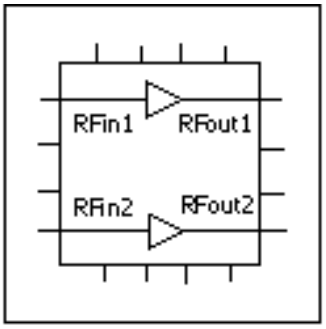
Reference Design (1850MHz Single-Ended Operation)

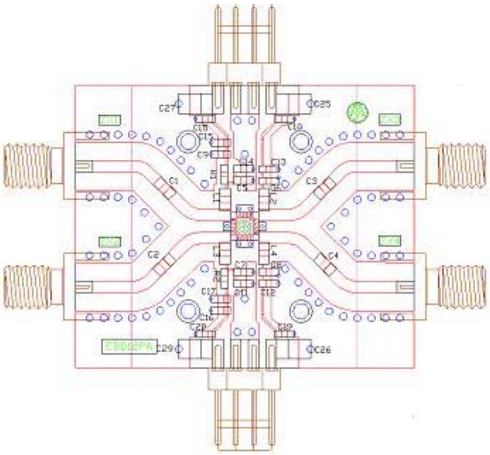
Evaluation board drawing in AutoCAD™ format available on request.





Package Schematic

Board Layout

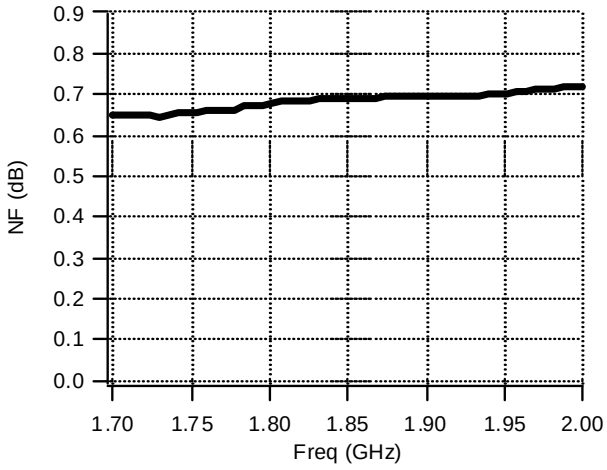


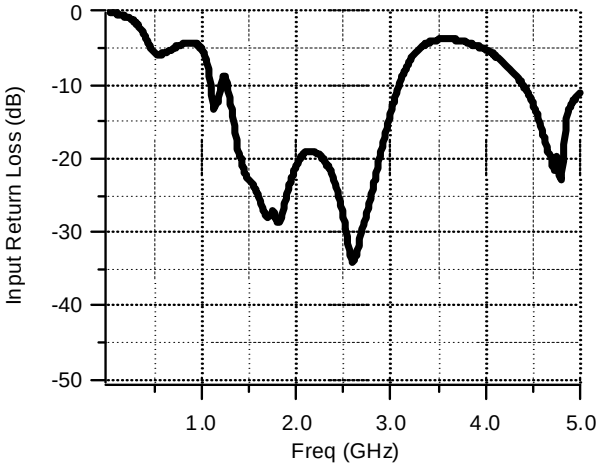
Bill of Materials

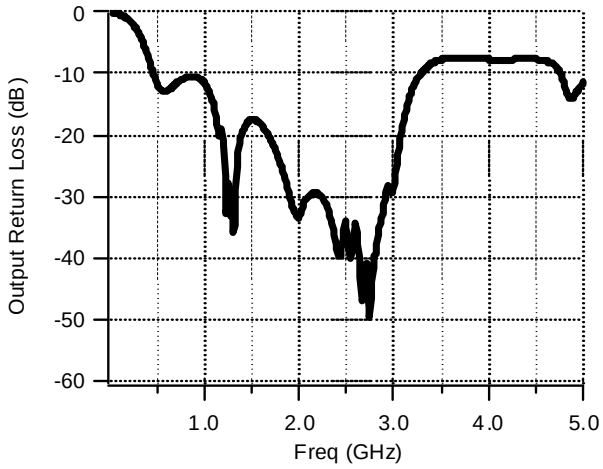
Designator	Supplier	Part Number	Description	Quantity
C1, C2, C3, C4	RS Components	464-6587	CAP-20pF-0805-±5%-50V(min)-LOW_ESR	4
C5, C6, C7, C8, C9, C17	RS Components	464-6385	CAP-10pF-0603-5%-50V-COG	6
C10, C18, C19, C20	RS Components	264-4602	CAP-22nF-0603-10%-50V	4
C11, C12, C13, C14, C15, C16	RS Components	464-6543	CAP-47nF-0603-+80/-20%-50V-Y5V	6
C25, C26, C27, C29	RS Components	406-0006	CAP-1uF-CASEB-20%-35V-TANT	4
L1, L2, L3, L4	RS Components	484-1372	IND-12nH-2012(0805)-5%-600mA-HQ	4
Q2	RFMD	FPM2750QFN	Dual FPD750-QFN 4x4	1
R1, R2	RS Components	213-2042	Resist-22Ω-1608(0603)-1%-0.1W	2
R3, R4, R5, R6	RS Components	363-4707	SMA Side-Mount RF Connector	4
(V1, V2)	RS Components	453-173	DC Connector (4-way)	2
Evaluation board	RFMD	EBD15PA	31mil thick FR4, 1/2 Ounce Cu on both sides	1

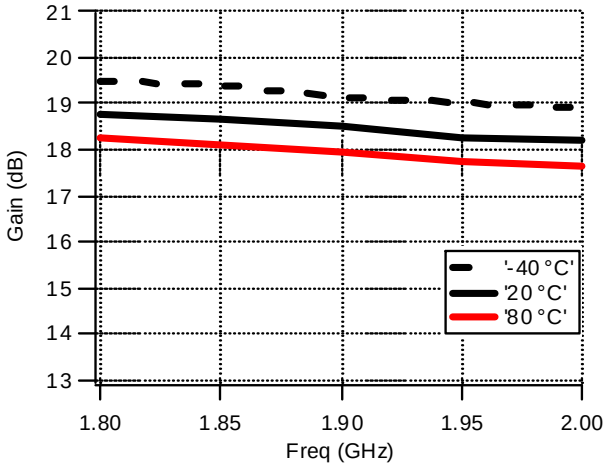
Typical Measured Evaluation Board Performance (Balanced Operation)

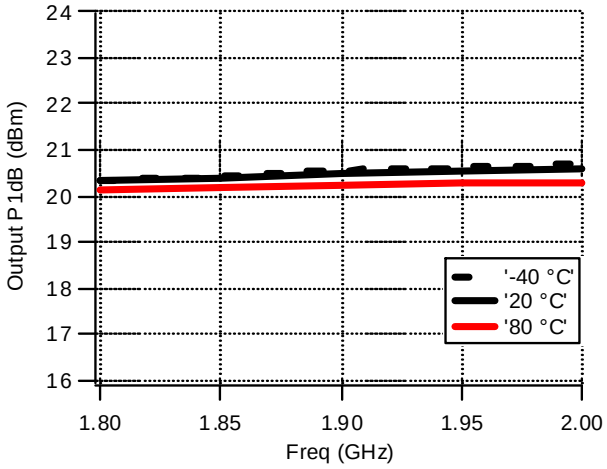
V_{DS}=3V, I_{DS}=40mA (per device), 50Ω environment and T_A=+22°C unless stated otherwise. All measurements shown are referenced to evaluation board connectors.

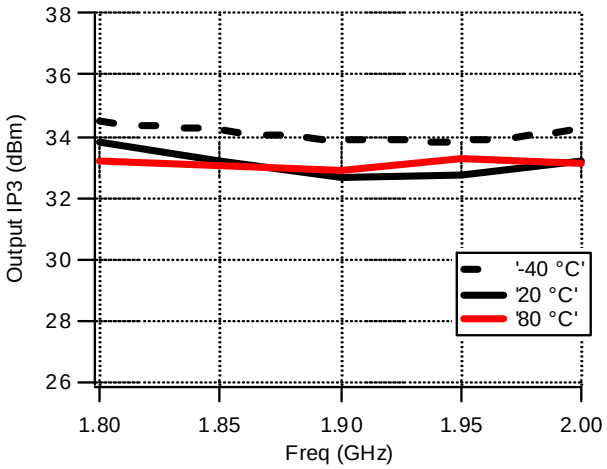












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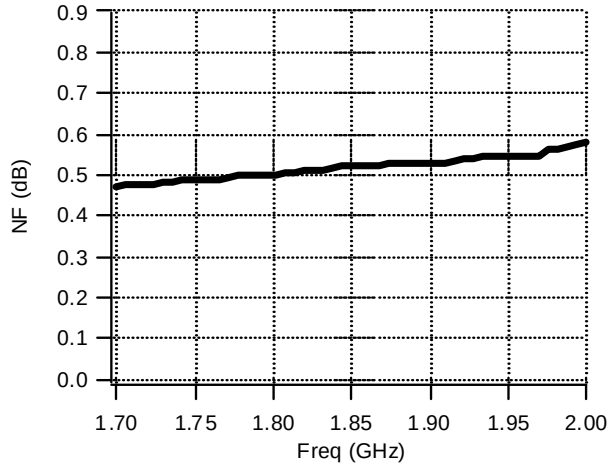
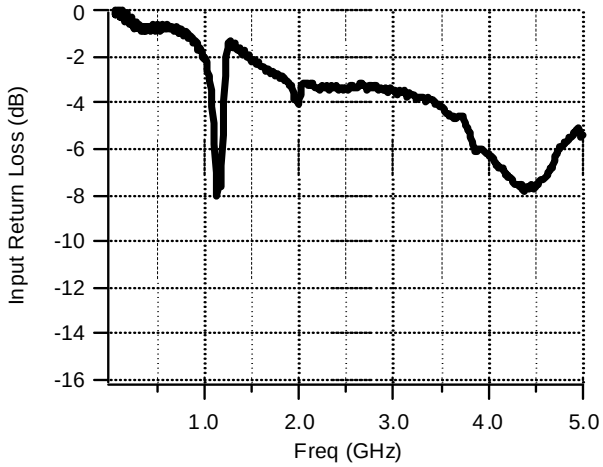
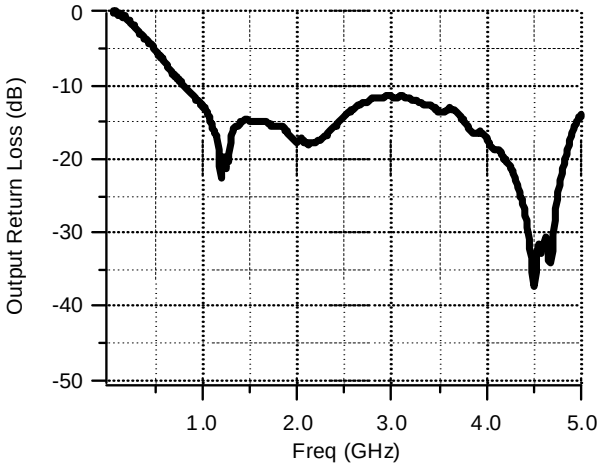
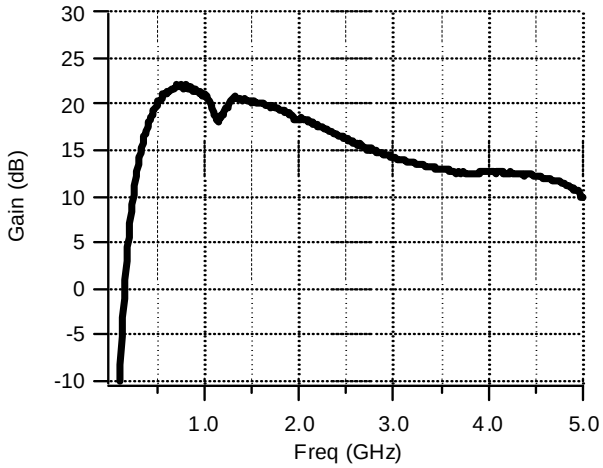
Typical Measured Evaluation Board Performance (Single-Ended Operation)

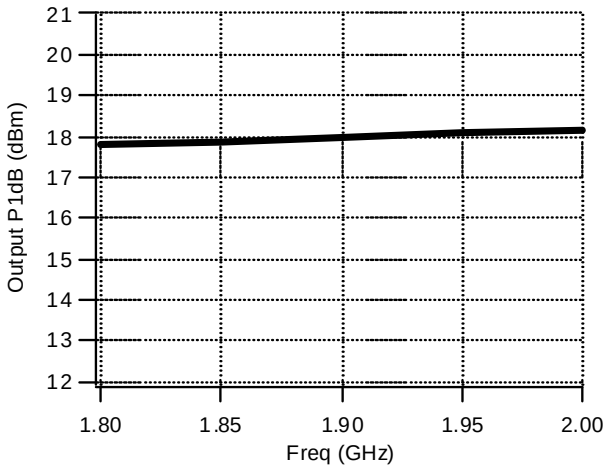
V_{DS}=3V, I_{DS}=40mA (per device), 50Ω environment and T_A=+22°C unless stated otherwise. All measurements shown are referenced to evaluation board connectors.

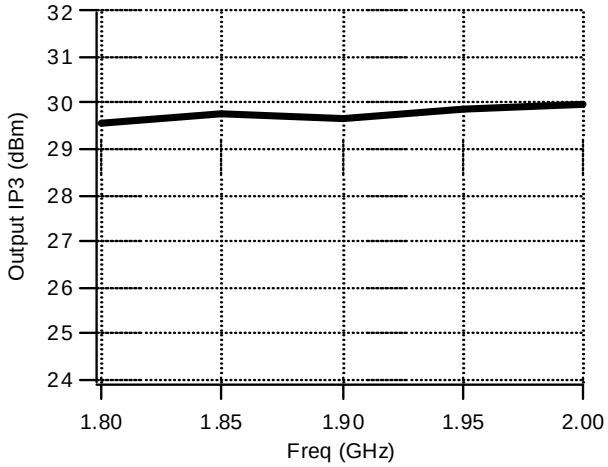




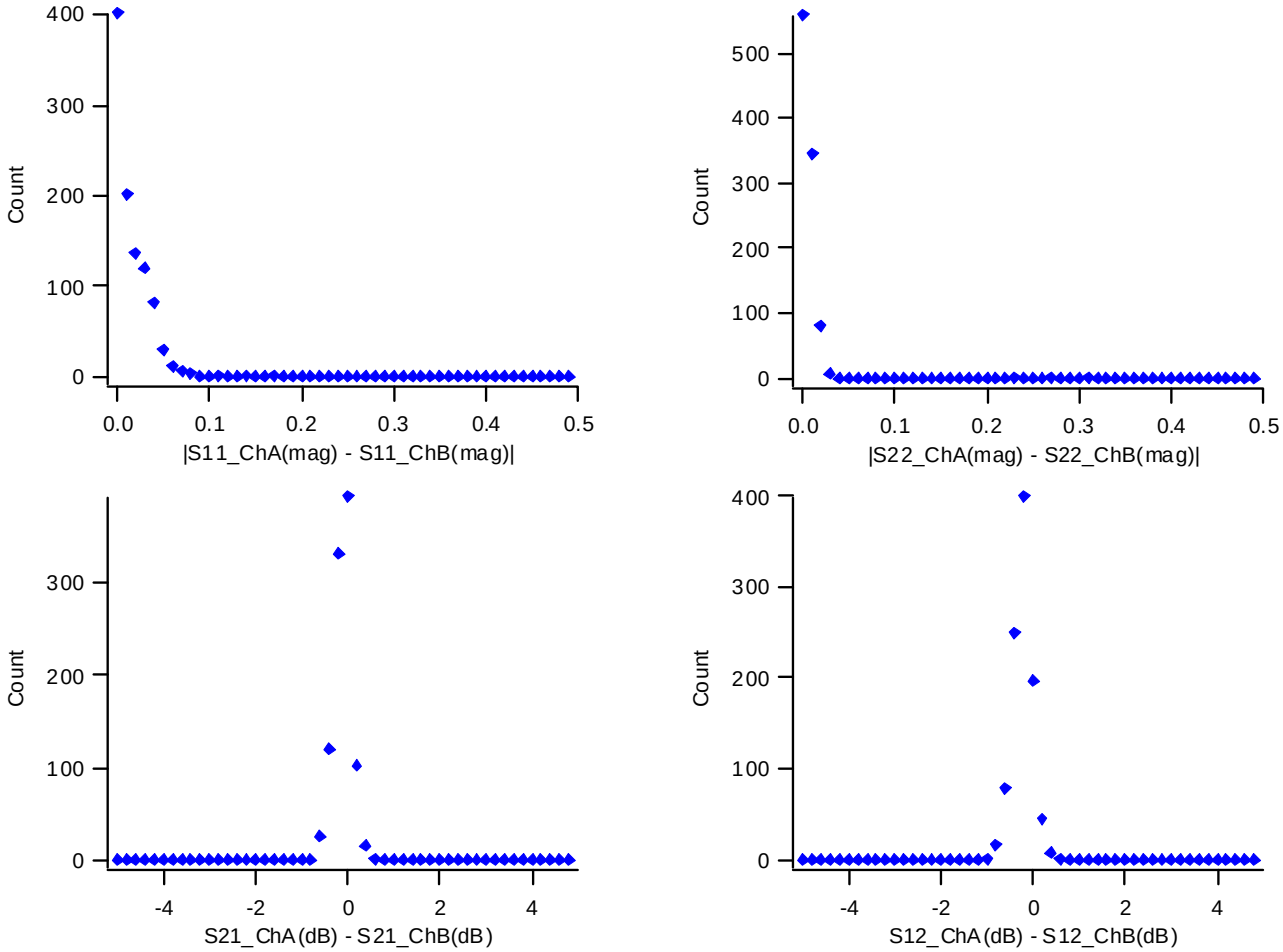








Typical Small Signal Magnitude Difference Within a Single Package



The histograms above represent the distribution of the asymmetry of RF parameters for the devices within a package. ChA and ChB are the two devices within the same package. The sample size for the histograms above is 1000 parts.

Parameter	Median	Standard Deviation	Test Limit	CPK
|S11 ChA (mag)-S11 ChB (mag)|	0.0001	0.027	0.1	1.3
|S22ChA (mag)-S22 ChB (mag)|	0.0001	0.019	0.1	1.7
S21 ChA (dB)-S21 ChB (dB)	0.006	0.408	±0.75	0.68
S12 ChA (dB)-S12 ChB (dB)	-0.128	0.205	±0.75	1.43

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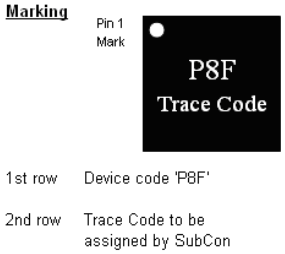
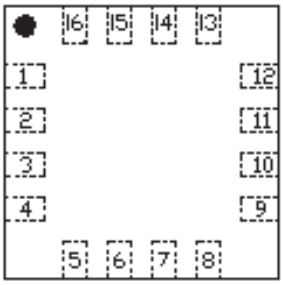
Part Identification



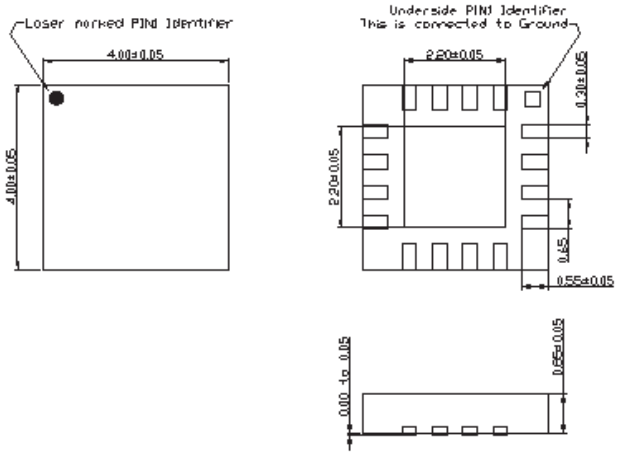
Pad Layout



Terminal	Function
1-4, 6, 15	Source 1
5	RFin 1/Gate 1
7, 9-12, 14	Source 2
8	RFin 2/Gate 2
13	RFout 2/Drain 2
16	RFout 1/Drain 1

Note: Dimensions in millimeters. Center paddle and pin 1 identifier are grounded.

Package Drawing



Tape and Reel

Tape and reel information on this material is in accordance with EIA-481-1 except where exceptions are identified.

Preferred Assembly Instructions

This package is compatible with both lead-free and leaded solder reflow processes as defined within IPC/J-STD-020C. The maximum package temperature should not exceed 260°C.

Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263..

MSL Rating

The device has an MSL rating of Level 1. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC, J-STD-020C, moisture/reflow sensitivity classification for non-hermetic solid state.

Application Notes and Design Data

Application Notes and design data including S-parameters are available from http://www.rfmd.com.

Reliability

An MTTF of 4.2 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Description	Ordering Code
Packaged pHEMT	FPM2750QFN
Evaluation Board (1.85GHz)	FPM2750QFNPCK

Delivery Quantity	Ordering Code
Reel of 1000	FPM2750QFN
Reel of 100	FPM2750QFNSR
Bag of 25	FPM27500QFNSQ
Bag of 5	FPM27500QFNSB

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