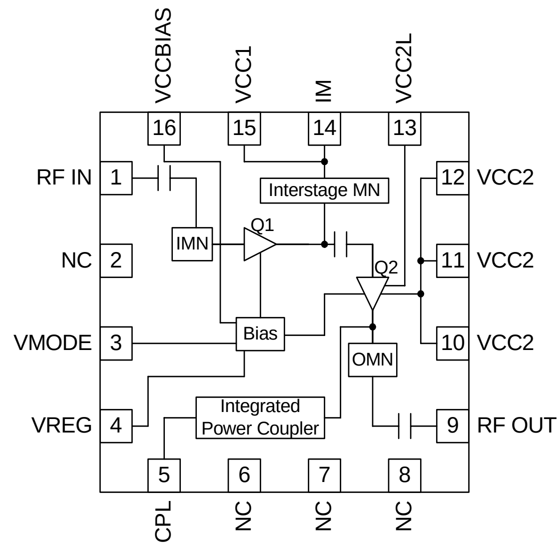
RF3267

3V W-CDMA LINEAR PA MODULE

RoHS Compliant & Pb-Free Product
Package Style: QFN, 16-Pin, 3x3x0.9mm



Functional Block Diagram

Features

- +28dBm Linear Output Power, ULRMC12.2 (26.5dBm, HSDPA)
- +28dB Linear Gain at +28dBm
- Digital Controlled HPM/LPM
- HSDPA Capable
- Low Quiescent Current (LPM <20mA)
- 21% Linear Efficiency@19dBm (LPM)
- Integrated Coupler

Applications

- 3V W-CDMA Handsets
- UMTS Band 1 Handsets
- Multi-Mode W-CDMA 3G Handsets
- UMTS Band 1 Datacards

Product Description

The RF3267 is a high-power, high-efficiency, linear PA module designed for use as the final RF amplifier in 3V, 50Ω W-CDMA handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1920MHz to 1980MHz band. The RF3267 has a digital control pin which, when enabled, will allow the amplifier to operate up to 19dBm output power with reduced current consumption. In the Low Power Mode, the current consumption may be reduced by more than 50% that of a standard power amplifier. The RF3267 also has an integrated directional coupler that would eliminate the use of an external coupler at the output. The RF3267 is fully HSDPA-capable and is assembled in a 16-pin, 3mmx3mm, QFN package.

Ordering Information

RF3267	3V W-CDMA Linear PA Module
RF3267PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltages, V_{CC} (No RF)	7.0	V
Supply Voltage in Standby Mode	7.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage,VCC (with RF) P_{INMAX}=5dBm, P_{OUT}=29dBm, VSWR=5:1	4.3	V
Supply Voltage, VCCBIAS	7.0	V
Control Voltage, VMODE	3.5	V
Control Voltage, V_{REG}	3.5	V
RF - Input Power	+6	dBm
RF - Output Power	+30	dBm
Output Load VSWR (Ruggedness)	10:1	
Operating Ambient Temperature	-30 to +85	°C
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power Mode (V_{MODE} Low)					T_C=+25°C, V_{CC}=3.4V, V_{MODE}=0V, V_{REG}=2.85V, Mod.=W-CDMA ULRMC 12.2, P_{OUT}=+28dBm, unless otherwise specified.
Operating Frequency Range	1920		1980	MHz	
Maximum Linear Output	28			dBm	
Maximum Linear Output (HSDPA)	26.5			dBm	HSDPA Modulation. See Condition A, Table 1.
Power Gain	26	28	32	dB	
Gain Delta versus Frequency	0	0.5	1	dB	
ACLR1 @ ±5MHz		-40	-36	dBc	
ACLR1 @ ±5MHz, HSDPA		-40	-36	dBc	P_{OUT}=+26.5dBm. See Condition A, Table 1.
ACLR2 @ ±10MHz		-54	-48	dBc	
ACLR2 @ ±10MHz, HSDPA		-52	-48	dBc	P_{OUT}=+26.5dBm. See Condition A, Table 1.
EVM	1	2.5	4	%	
Linear Efficiency	37	40	47	%	
I_{CC} (I_{CC}, I_{CC}_Bias)	400	463	515	mA	
Input VSWR		2.1:1			
Harmonic Output (2fo)			-15	dBm	f=2fo, RBW=1MHz
Harmonic Output (3fo)			-25	dBm	f=3fo, RBW=1MHz

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power Mode (V_{MODE} Low), cont'd					
Noise Power					
GPS		-104		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, RX=1570MHz to 1580MHz
GSM		-110		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, RX=875MHz to 960MHz
DCS		-92		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, RX=1805MHz to 1880MHz
W-CDMA		-95		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, RX=2110MHz to 2170MHz, TX/RX Offset=130MHz
W-CDMA		-98		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, RX=2110MHz to 2170MHz, TX/RX Offset=190MHz
Bluetooth		-103		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, RX=2400MHz to 2480MHz
PHS		-57		dBm/30KHz	$-50 \le P_{OUT} \le P_{OUT,MAX}$, TX=1932.3MHz to 1980MHz, RX=1893.5MHz to 1919.6MHz
Stability			-60	dBc	$3.1 \le V_{CC} \le 4.3V$, $-50 \le P_{OUT} \le P_{OUT,MAX}$, RBW=1MHz, Load VSWR=6:1, All Phase Angles
Reverse Intermodulation Product					
5MHz Offset			-31	dBc	IM product, interferer at -40dBc CW @ 5MHz offset
10MHz Offset			-41	dBc	IM product, interferer at -40dBc CW @ 10MHz offset
Phase Jump			25	°	V_{MODE} switched from 0V to 2.8V, P_{OUT}=+19dBm

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Low Power Mode (V_{MODE} High)					T_C=+25°C, V_{CC}=3.4V, V_{MODE}=2.8V, V_{REG}=2.85V, Mod.=W-CDMA ULRMC 12.2, P_{OUT}=19dBm, unless otherwise specified.
Operating Frequency Range	1920		1980	MHz	
Maximum Linear Output	+19			dBm	
Maximum Linear Output (HSDPA)	+18			dBm	HSDPA Modulation. See Condition A, Table 2.
Power Gain	17	20	25	dB	
Gain Delta versus Frequency	0	0.5	1	dB	
ACLR1 @ ±5MHz		-42	-36	dBc	
ACLR1 @ ±5MHz, HSDPA		-40	-36	dBc	P_{OUT}=+18dBm. See Condition A, Table 2.
ACLR2 @ ±10MHz		-54	-48	dBc	
ACLR2 @ ±10MHz, HSDPA		-52	-48	dBc	P_{OUT}=+18dBm. See Condition A, Table 2.
EVM	1	2.5	4.0	%	
Input VSWR		1.3:1			
Linear Efficiency	17	21	27	%	
I_{CC} (I_{CC}, I_{CC}_Bias)	86	108	142	mA	
Harmonic Output (2fo)			-15	dBm	P_{OUT}=+19dBm, f=2fo, RBW=1MHz
Harmonic Output (3fo)			-25	dBm	P_{OUT}=+19dBm, f=3fo, RBW=1MHz
Stability			-60	dBc	3.1≤V_{CC}≤4.3V, -50≤P_{OUT}≤$P_{OUT(MAX)}$, RBW=1MHz, Load VSWR=6:1, All Phase Angles
Reverse Intermodulation Product					
5MHz Offset			-31	dBc	IM product, interferer at -40dBc CW @ 5MHz offset
10MHz Offset			-41	dBc	IM product, interferer at -40dBc CW @ 10MHz offset
Phase Jump			25	°	V_{MODE} switched from 2.8V to 0V, P_{OUT}=+19dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Power Supply Voltage (V_{CC1}/V_{CC2})	3.1	3.4	4.3	V	
Power Supply Voltage (V_{CCBIAS})	1.7	3.4	4.3	V	
V_{REG} "Low" Voltage	0		0.5	V	PA shutdown
V_{REG} "High" Voltage	2.75	2.85	2.95	V	PA enabled
V_{REG} Current		4.00	4.50	mA	
High Power Idle Current ($I_{CC1}/I_{CC2}/I_{CC\_BIAS}$)	60	75	105	mA	$V_{CC1}/V_{CCBIAS}/V_{CC2}$=3.4V, V_{MODE}=0.0V, P_{OUT}=0W, V_{REG}=2.85V, T=+25°C
Low Power Idle Current ($I_{CC1}/I_{CC2}/I_{CC\_BIAS}$)	14	18	30	mA	$V_{CC1}/V_{CCBIAS}/V_{CC2}$=3.4V, V_{MODE}=2.8V, P_{OUT}=0W, V_{REG}=2.85V, T=+25°C
Leakage Current ($I_{CC1}/I_{CC2}/I_{CC\_BIAS}$)		0.2	5	µA	$V_{CC1}/V_{CCBIAS}/V_{CC2}$=4.3V, no RF applied, V_{MODE}=0.0V, V_{REG}=0.0V, T=+25°C
V_{MODE} "Low" Voltage	0.0		0.5	V	Voltage range for High power mode.
V_{MODE} "High" Voltage	2.0		3.0	V	Voltage range for Low power mode.
V_{MODE} Current		500	600	µA	
RF Turn-On/Off Time			6	uS	
DC Turn-On/Off Time			10	uS	
Coupled Output Power (High and Low Power Modes)					T_C=+25°C, V_{CC}=3.4V, V_{MODE}=2.8V and 0V, V_{REG}=2.85V, Z_{LOAD}=50Ω, Mod.=W-CDMAULRMC12.2, unless otherwise specified.
Operating Frequency Range	1920		1980	MHz	
Coupling Factor		19.5		dB	P_{OUT}=28dBm, ULRMC 12.2kbps

Condition Table 1

A) Max Linear Output (P_{OUTMAX_1}) reduction at normal and high voltage (V_{CC} > 3.4V).

As a reference, the following setup shall be used for HSDPA test with reduced output power.

Parameter	Conditions	Level
Output Power ($P_{OUT\_MAX\_1}$) for different ratio of β_c to β_d for all values of β_{hs}	A) $1/15 \leq \beta_c/\beta_d \leq 12/15$	+26.5dBm
	B) $13/15 \leq \beta_c/\beta_d \leq 15/8$	+25.5dBm
	C) $15/7 \leq \beta_c/\beta_d \leq 15/0$	+24.5dBm

Condition Table 2

A) Max Linear Output (P_{OUTMAX_1}) reduction at normal and high voltage (V_{CC} > 3.4V).

As a reference, the following setup shall be used for HSDPA test with reduced output power.

Parameter	Conditions	Level
Output Power ($P_{OUT\_MAX\_1}$) for different ratio of β_c to β_d for all values of β_{hs}	A) $1/15 \leq \beta_c/\beta_d \leq 12/15$	+18dBm
	B) $13/15 \leq \beta_c/\beta_d \leq 15/8$	+17dBm
	C) $15/7 \leq \beta_c/\beta_d \leq 15/0$	+16dBm

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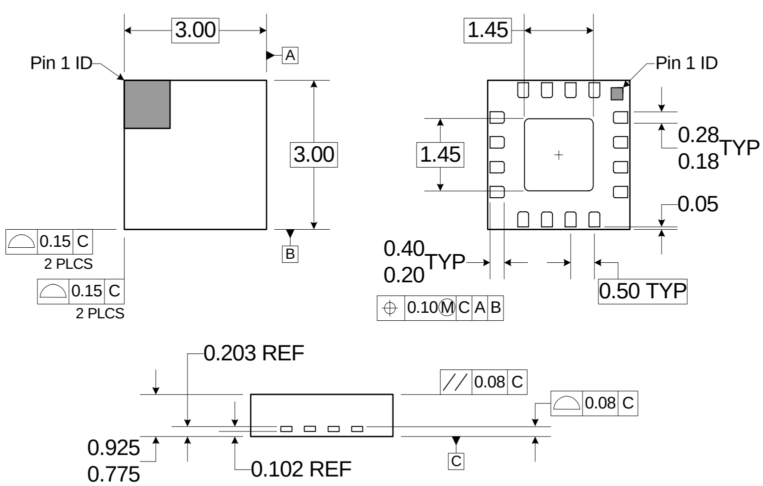
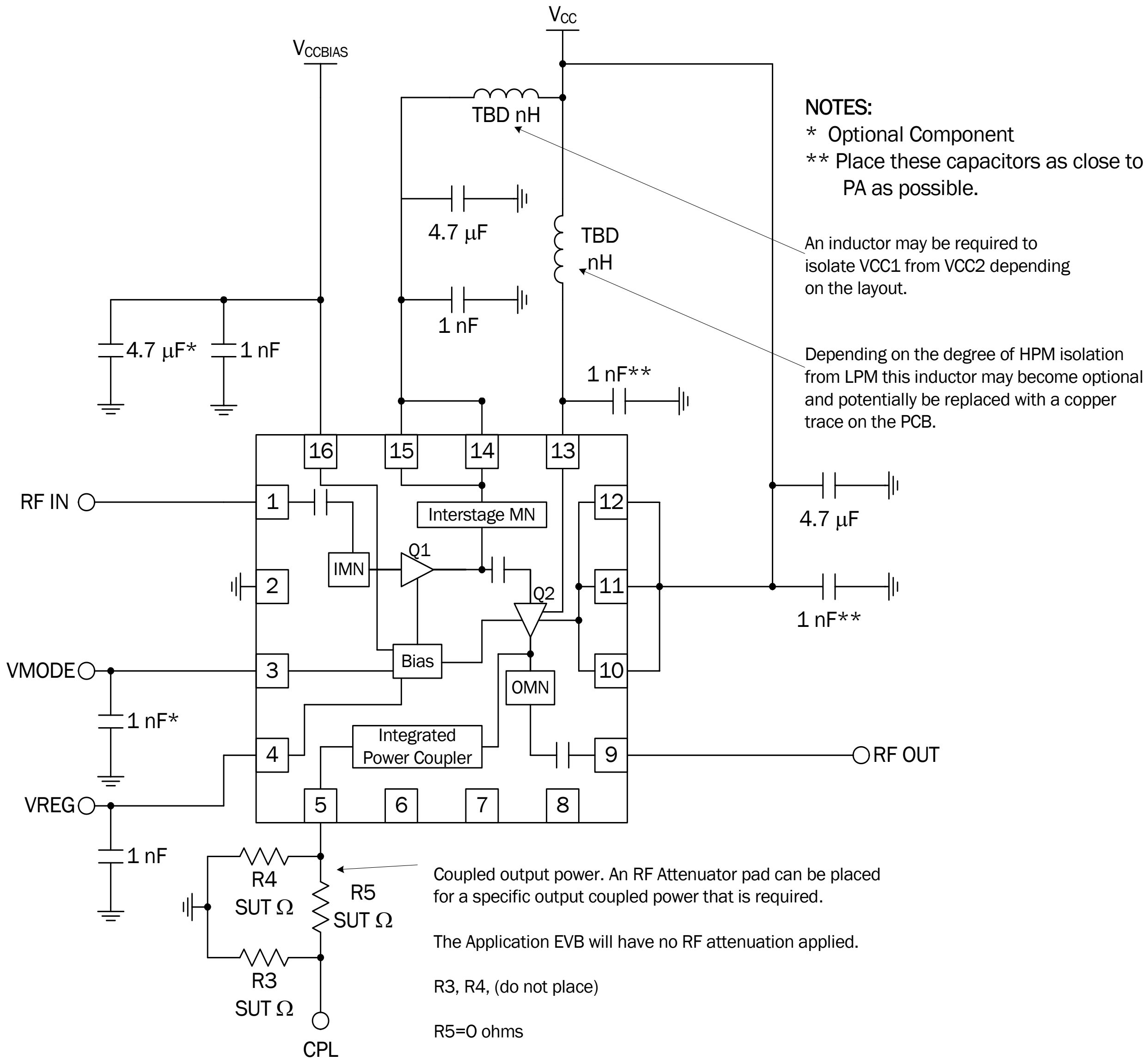
Pin	Function	Description
1	RF IN	AC-coupled RF input internally matched to 50Ω.
2	NC	This pin must remain floating.
3	VMODE	Digital control voltage input for switching the PA from low power mode to high power mode and vice versa. A "low" on this pin operates the PA in the specified high power mode. A "high" on this pin operates the PA in the specified low power mode.
4	VREG	Regulated voltage input required for operation of PA bias circuitry. This pin also functions as the PA enable/disable control.
5	CPL	This is the coupled power output. A RF attenuator can be placed on the customer's phone board if RF power needs to be reduced prior to input of the transceiver or baseband hardware.
6	NC	This pin must remain floating.
7	NC	This pin must remain floating.
8	NC	This pin must remain floating.
9	RF OUT	AC-coupled RF output internally matched to 50Ω.
10	VCC2	Power supply input for the collector voltage on Q2 RF output amplification stage. A low frequency decoupling capacitor (4.7 μF) is required on this line. The voltage on this pin may be controlled by a DC converter.
11	VCC2	Same as pin 10.
12	VCC2	Same as pin 10.
13	VCC2L	Power supply input for the collector voltage on LPM Q2 RF output amplification stage. A low frequency decoupling capacitor (4.7 μF) is required on this line. The voltage on this pin may be controlled by a DC-DC converter.
14	IM	Interstage matching.
15	VCC1	Power supply input for the collector voltage on Q1 RF output amplification stage. A low frequency decoupling capacitor (4.7 μF) is required on this line. The voltage on this pin may be controlled by a DC-DC converter. Pin 15 is connected internally to pin 14, and should be connected together on the PCB.
16	VCCBIAS	Power supply input for the DC bias circuitry. The voltage on this pin must be 3.1 V or greater for specified operation. Low frequency decoupling capacitors (4.7 μF and 1 nF) are recommended on this line.
Pkg Base	GND	Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

Package Drawing



Shaded areas represent pin 1. *Dimensions in mm.*

Preliminary Application Schematic



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 μinch to 8 μinch gold over 180 μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

A = 0.64 x 0.28 (mm) Typ.
B = 0.28 x 0.64 (mm) Typ.
C = 0.78 x 0.64 (mm)
D = 0.64 x 1.28 (mm)
E = 1.50 (mm) Sq.

Dimensions in mm.

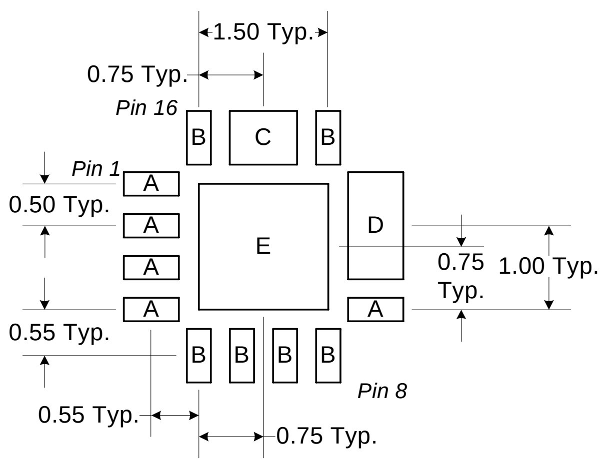


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2 mil to 3 mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

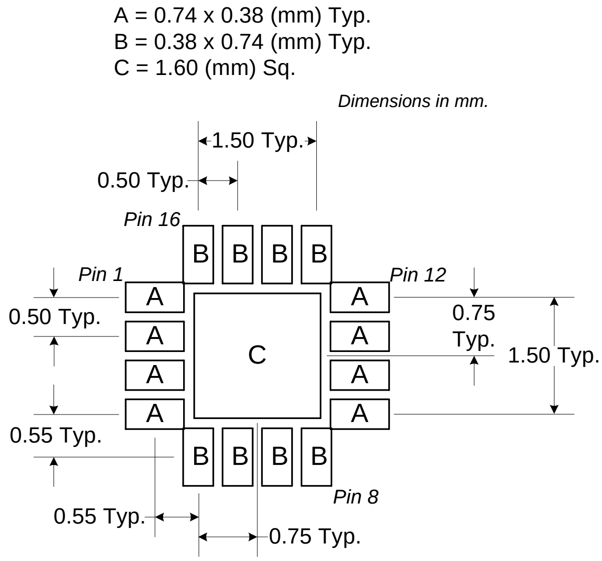


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203 mm to 0.330 mm finished hole size on a 0.5 mm to 1.2 mm grid pattern with 0.025 mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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Tape and Reel Information

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330 mm (13 inches) in diameter or 178 mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

The following table provides useful information for carrier tape and reels used for shipping the devices described in this document.

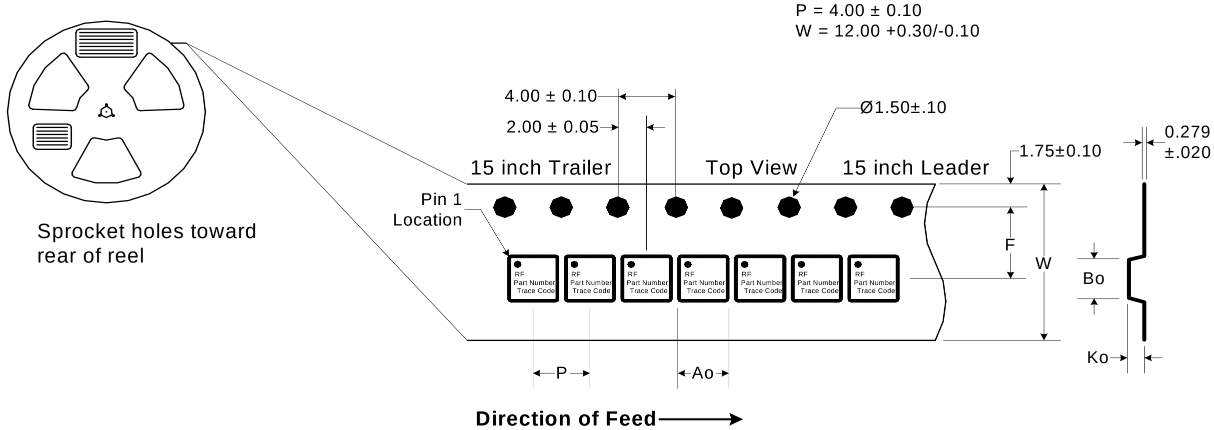
RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF3267TR7	7 (178)	2.4 (61)	12	4	Single	2500

QFN (Carrier Tape Drawing with Part Orientation)

Notes:

1. All dimensions are in millimeters (mm).
2. Unless otherwise specified, all dimension tolerances per EIA-481.

Ao = 3.18 ± 0.10
Bo = 3.18 ± 0.10
F = 5.50 ± 0.05
Ko = 1.02 ± 0.10
P = 4.00 ± 0.10
W = 12.00 +0.30/-0.10



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