rfmd.com

RF5633

SINGLE 5.0V, 3.3 TO 3.8GHZ LINEAR POWER AMPLIFIER

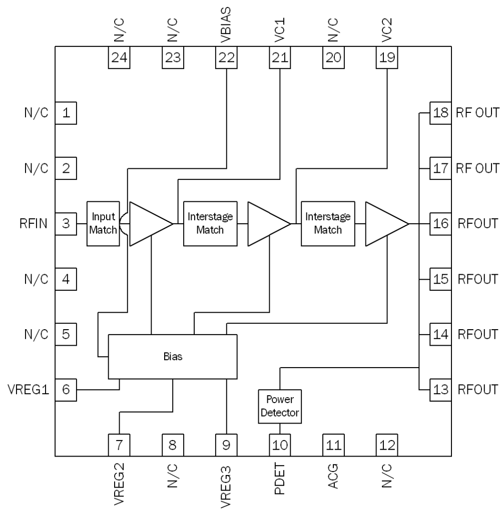
Package Style: QFN, 24-Pin, 4mmx4mmx0.9mm

Features

- High Gain; 34dB
- Supports Low Gain Mode
- 2.5% EVM WiMAX +28dBm, 5.0V
- Integrated Power Detector
- Multiple Frequency Ranges

Applications

- WiMAX Customer Premises Equipment
- WiMAX Access Points
- IEEE 802.16 WiMAX Systems



Functional Block Diagram

Product Description

The RF5633 is a linear power amplifier IC designed specifically for WiMAX final or driver stage applications. The device is manufactured on an advanced InGaP Heterojunction Bipolar Transistor (HBT) process, and is provided in a leadless chip carrier with a backside ground. The RF5633 is designed to maintain linearity over a wide range of temperatures and power outputs. The external match offers tunability for output power over multiple bands. RF5633 features internal input and interstage match, power down mode, and power detector.

Ordering Information

RF5633SQ	Standard 25 piece bag
RF5633SR	Standard 100 piece reel
RF5633TR13	Standard 2500 piece reel
RF5633LPCK-410	3.4GHz to 3.6GHz WiMAX Evaluation PCBA with 5 loose pcs
RF5633HPCK-410	3.6GHz to 3.8GHz WiMAX Evaluation PCBA with 5 loose pcs

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage, RF Applied	-0.5 to +5.25	V_{DC}
Supply Voltage, no RF Applied	-0.5 to +6.0V	V_{DC}
DC Supply Current	2000	mA
Input RF Power with 50Ω Load	+15	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	MSL2	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
IEEE802.16e, 5.0V					Nominal Condition T=25 °C, V_{CC}=5.0V, V_{REG} 1, 2, and 3=5.0V, Frequency=3.4GHz to 3.6GHz, using a standard IEEE802.16e 16QAM waveform at 37% duty cycle unless otherwise noted.
Compliance					IEEE802.16e
Frequency	3.4		3.6	GHz	
Output Power	26.5	28		dBm	With IEEE802.16e, 16 QAM standard waveform at <2.5% EVM
EVM		2.5	3	%	802.16e increase in EVM over EVM floor; RF P_{OUT}=+28dBm, Over temperature -40°C to +85°C
Stability	0		34	dBm	PA should be stable when P_{OUT} is measured from 0 to 34dBm
Gain	32.5	34.5	36.5	dB	P_{OUT}=28dBm
Low Gain Mode - Gain reduction		24		dB	Drop in gain versus high gain mode, by setting V_{REG2}=0V
Gain flatness, high gain mode and low gain mode			3	dB	Peak-Peak over any 200MHz bandwidth.
Power Detect Voltage	0.2		1.8	V	P_{OUT}=10 to 30dBm.
Noise Figure		5		dB	
Current					
Operating		1000	1300	mA	RF P_{OUT}=+28dBm, Over Temperature -40°C to +85°C
Quiescent		600	800	mA	RF=OFF, V_{CC}=+5V, V_{REG}=5V, Over Temperature -40°C to +85°C
I_{REG}		6	10	mA	RF P_{OUT}=+28dBm V_{CC}=+5V, V_{REG}=5V, Over Temperature -40°C to +85°C
Shutdown		5	30	uA	RF=OFF, V_{CC}=+5V, V_{REG}=0V, Over Temperature -40°C to +85°C
Power Supply		5	5.25	V	
V_{REG1}, V_{REG2}, V_{REG3} Input Voltage	4.85	5	5.15	V	
Turn-on time from setting of V_{REG}		400	1500	nsec	Output stable to within 90% of final gain
Input Return Loss		-15	-10	dB	
Output Return Loss		-10	-7	dB	
Stable into Output VSWR			4:1		No spurs above -47dBm
No damage into Output VSWR			10:1		+5dBm P_{IN}

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
IEEE802.16e, 5.0V					Nominal Condition T=25 °C, V_{CC}=5.0V, V_{REG} 1, 2, and 3=5.0V, Frequency=3.6GHz to 3.8GHz, using a standard IEEE802.16e 16QAM 10MHz BW waveform at 37% duty cycle unless otherwise noted.
Compliance					IEEE802.16e
Frequency	3.6		3.8	GHz	
Output Power	25.5	27		dBm	With IEEE802.16e, 16QAM standard waveform at <2.5% EVM
EVM		2.5	3	%	802.16e increase in EVM over EVM floor; RF P_{OUT}=+27dBm
Stability	0		34	dBm	PA should be stable when P_{OUT} is measured from 0 to 34dBm
Gain	32.5	34.5	36.5		P_{OUT}=27dBm
Gain Variation over Temperature			±2	dB	
Low Gain Mode - Gain reduction		22		dB	Drop in gain versus high gain mode, by setting V_{REG2}=0V
Gain flatness, high gain mode and low gain mode			3	dB	Peak-Peak over any 200MHz bandwidth.
Power Detect Voltage	0.2		1.8	V	P_{OUT}=10 to 30dBm.
Noise Figure		5		dB	
Current					
Operating		1000	1350	mA	RF P_{OUT}=+27dBm, Over Temperature -40°C to +85°C
Quiescent		600	800	mA	RF=OFF, V_{CC}=+5V, V_{REG}=5V, Over Temperature -40°C to +85°C
I_{REG}		6	10	mA	RF P_{OUT}=+27dBm V_{CC}=+5V, V_{REG}=5V, Over Temperature -40°C to +85°C
Shutdown		5	30	uA	RF=OFF, V_{CC}=+5V, V_{REG}=0V, Over Temperature -40°C to +85°C
Power Supply		5	5.25	V	
V_{REG1}, V_{REG2}, V_{REG3} Input Voltage	4.85	5	5.15	V	
Turn-on time from setting of V_{REG}		400	1500	nsec	Output stable to within 90% of final gain
Input Return Loss		-15	-10	dB	
Output Return Loss		-10	-7	dB	
Stable into Output VSWR			4:1		No spurs above -47dBm
No damage into Output VSWR			10:1		+5dBm P_{IN}
ESD					
Human Body Model	500			V	
Charge Device Model	1000			V	

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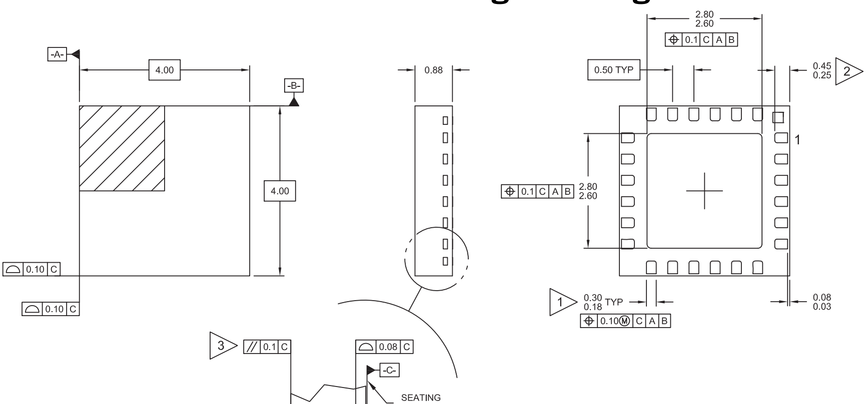
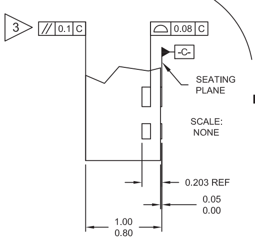
Pin	Function	Description
3	RFIN	RF input. This pin is matched to 50Ω and in DC-blocked internally.
6	VREG1	First stage input bias voltage. This pin requires a regulated supply to maintain nominal bias current.
7	VREG2	Second stage input bias voltage. This pin requires a regulated supply to maintain nominal bias current.
9	VREG3	Third stage input bias voltage. This pin requires a regulated supply to maintain nominal bias current.
10	PDET	Power detector provides an output voltage proportional to the RF level VCC3/RF OUT.
11	ACG	AC ground requires capacitor to ground.
13-18	VCC3/RFOUT	RF output and bias for third stage. Output is externally matched to 50Ω and needs a DC-block.
19	VC2	Second stage supply voltage.
21	VC1	First stage supply voltage.
22	VBIAS	Supply voltage for the bias reference and control circuits. May be connected with VCC1, VCC2, VCC3 as long as appropriate isolation is provided.
1, 2, 4, 5, 8, 12, 20, 23, 24	N/C	No internal connection. May be connected to ground.
Pkg Base	GND	Ground connection. The back side of the package should be connected to the ground plane through as short a connection as possible, e.g., PCB vias under the device.

Package Drawing





PKG-05-1000 REV (-)

NOTES:

1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
2. DIMENSION REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
4. RADIUS ON TERMINALS IS OPTIONAL.

PCB Design Requirements

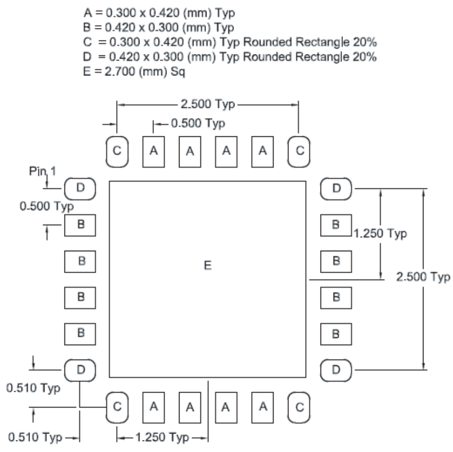
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 μinch to 8 μinch gold over 180 μinch nickel.

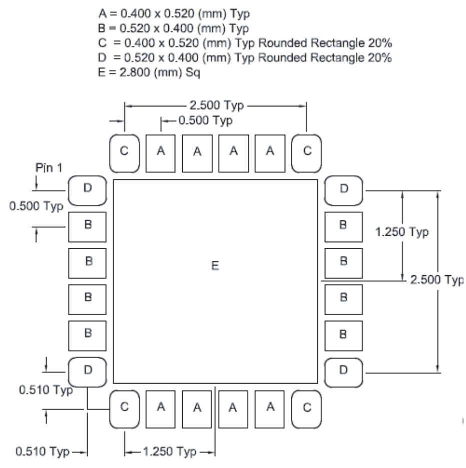
PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

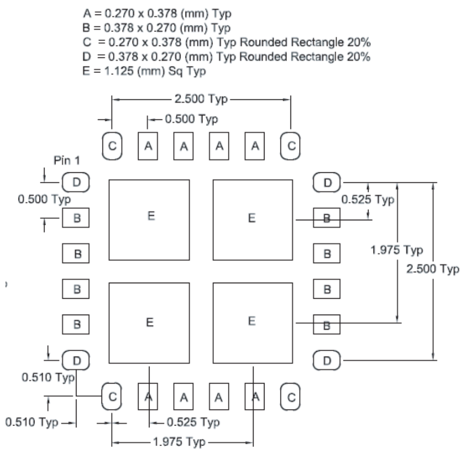
PCB Metal Land and Solder Mask Pattern



PCB METAL LAND PATTERN



PCB SOLDER MASK PATTERN

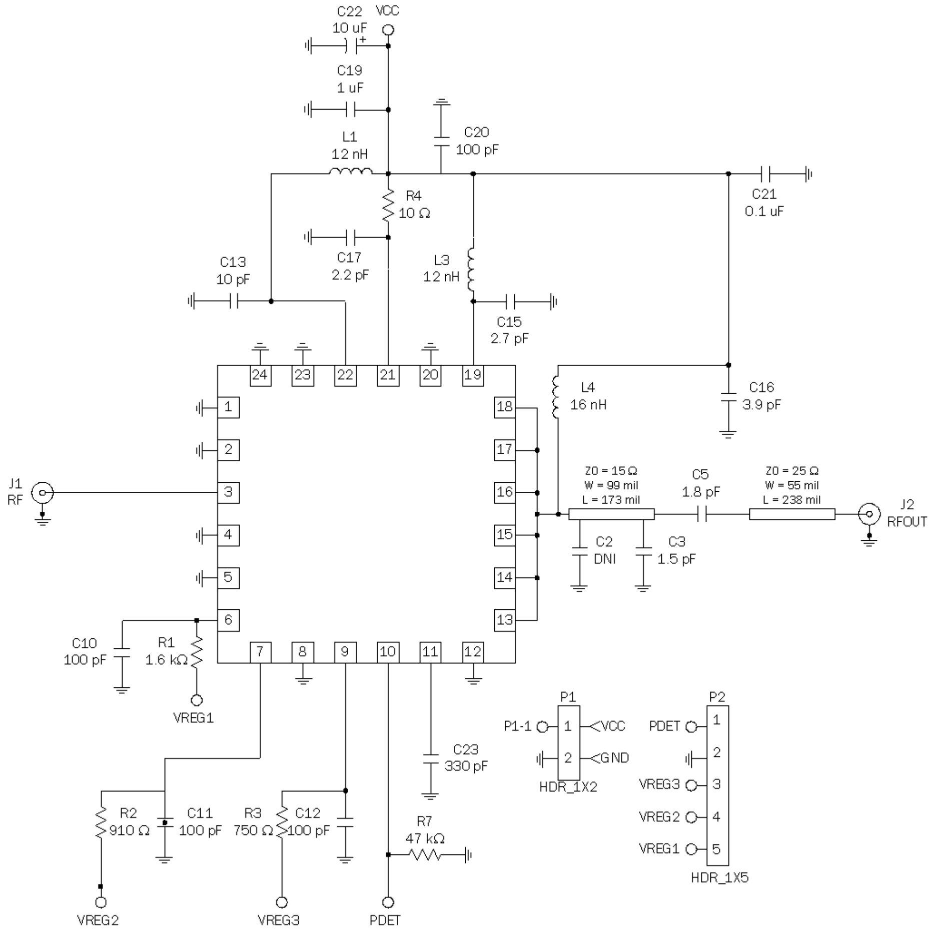


PCB STENCIL PATTERN

Note: Themal vias for center slub "E" should be incorporated into the PCB design. The number and size of thermal vias will depend on the application. Example of the number and size of vias can be found on the RFMD evaluation board layout.

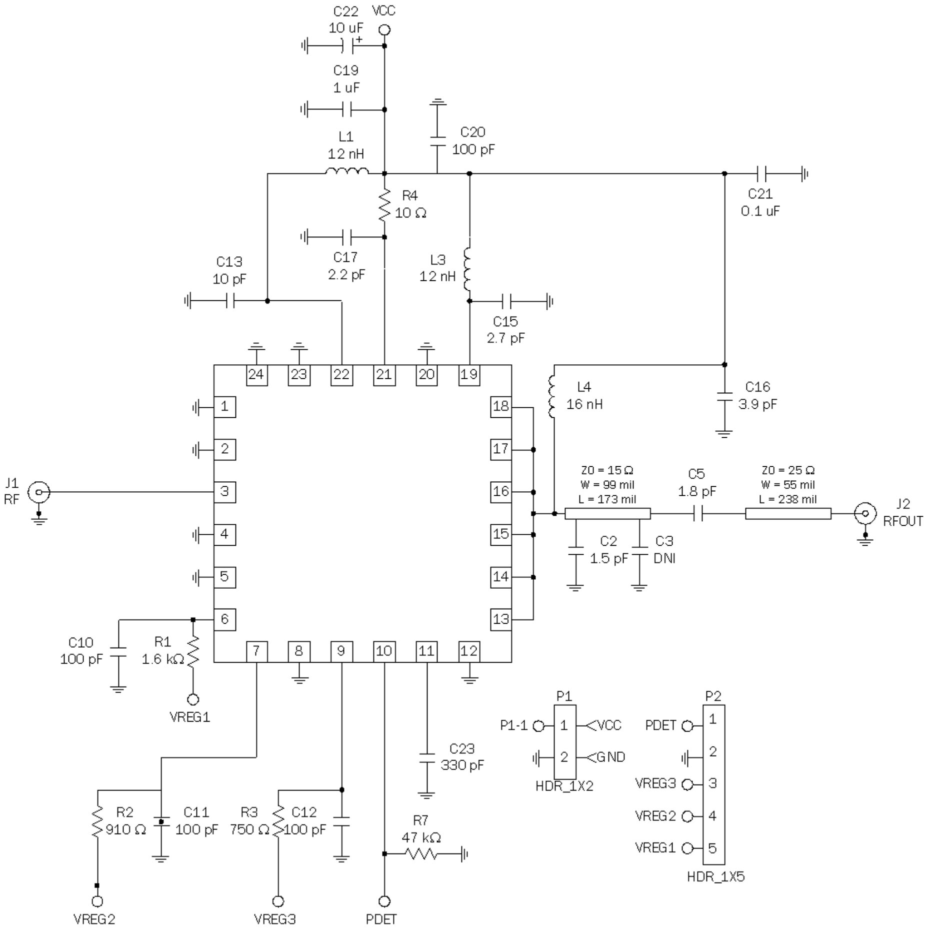
Evaluation Board Schematic

3.4GHz to 3.6GHz Operation



Evaluation Board Schematic

3.6GHz to 3.8GHz Operation



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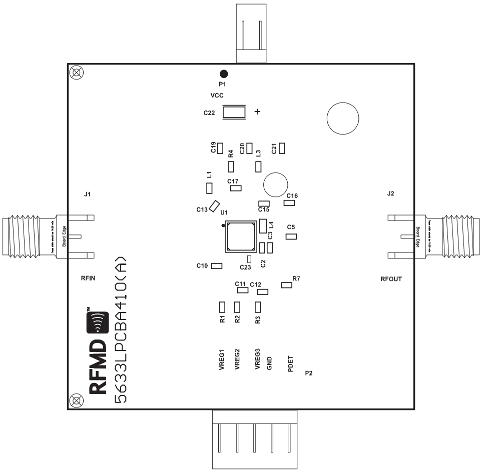
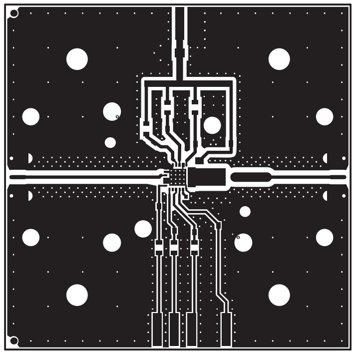
Evaluation Board Layout

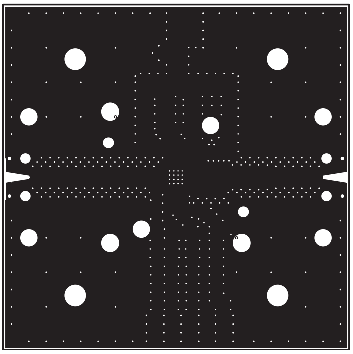
3.4GHz to 3.6GHz Operation



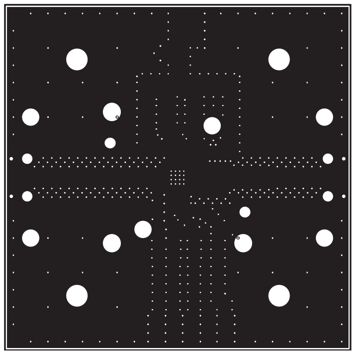
Assembly



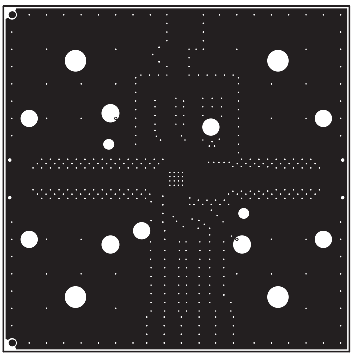
Top



In1



In2



Back

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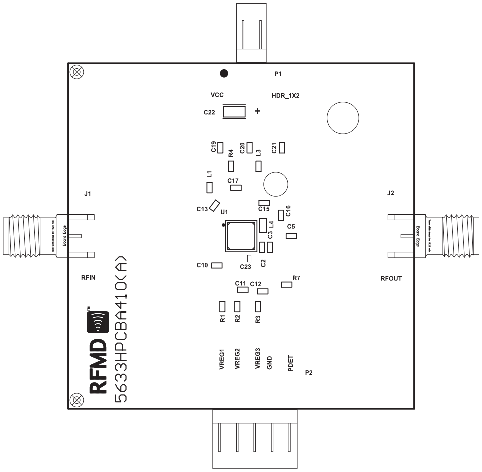
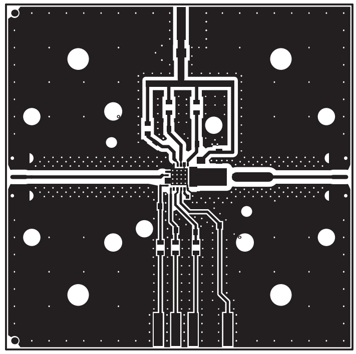
Evaluation Board Layout

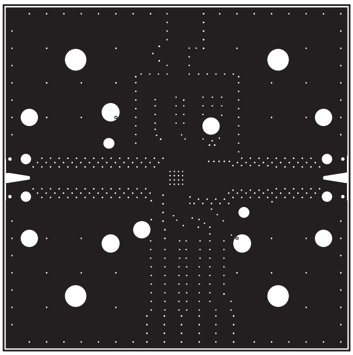
3.6GHz to 3.8GHz Operation



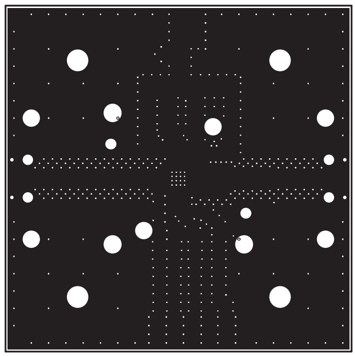
Assembly



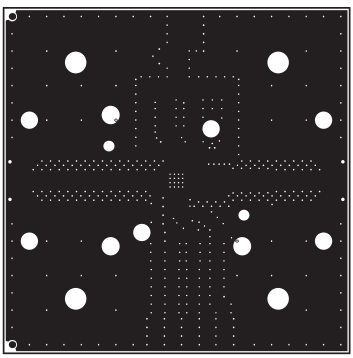
Top



In1

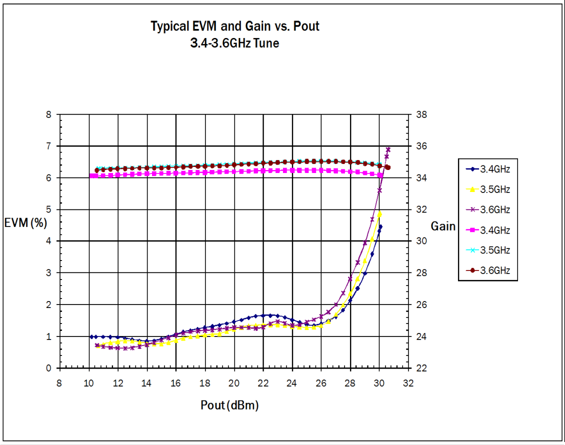


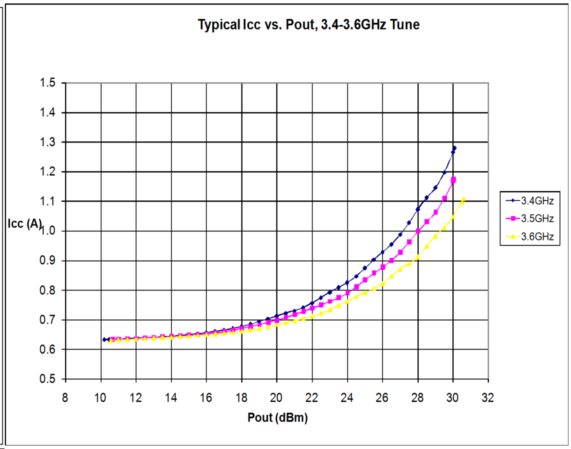
In2

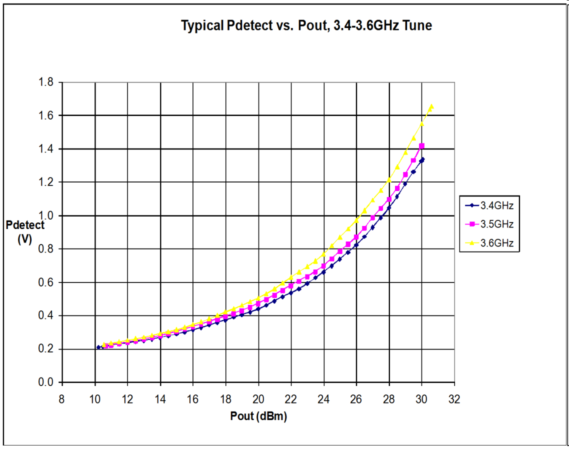


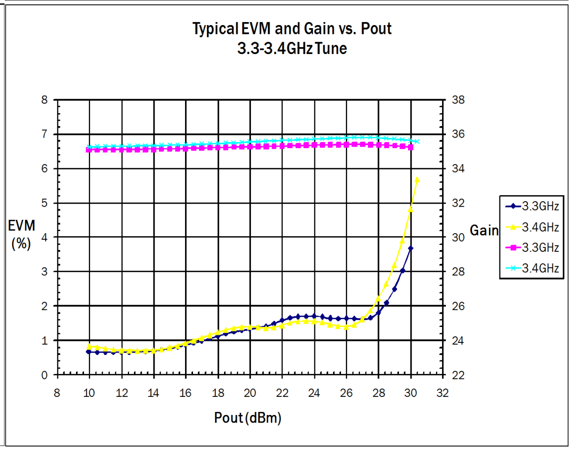
Back

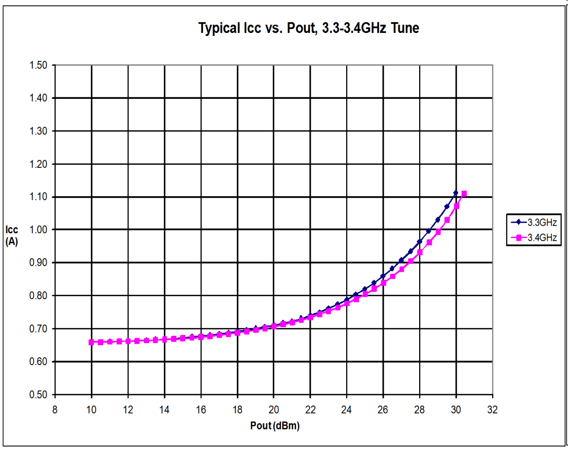
CC=5.0V and VREG1, 2, and 3=5.0V

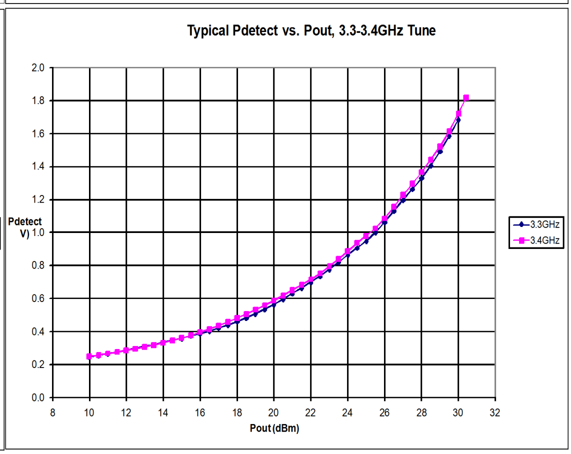












V_{CC}=5.0V and VREG1, 2, and 3=5.0V