# RF6590

## POWER MANAGEMENT IC

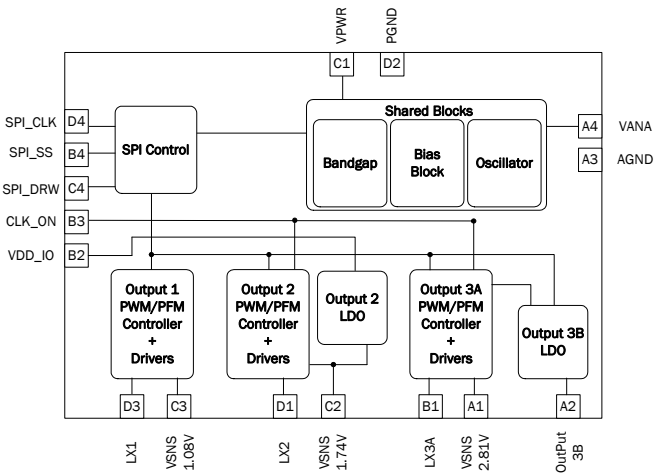
Package: 16-Bump WLCSP, 4x4 Array, 1.73mmx1.73mm


## Features

- 3 High Efficiency DC to DC Buck Converters
- 2 Low Noise LDOs
- Wide Voltage Range (2.5V to 5.1V)
- 2.8MHz PWM Switching Frequency
- Low Quiescent Current
- Auto PFM/PWM Controller
- Programmable Via SPI
- Small, Wafer-Level Chip-Scale Package
- Over-current (OC) Protection

## Applications

- Transceiver Power Management
- LTE, 2G/3G Multi-Mode, Multi-Band Handsets
- Quad-Band GSM/EDGE Handsets
- Multi-Band UMTS Handsets




Functional Block Diagram

## Product Description

The RF6590 is a power management IC designed for use in transceiver applications, consisting of three low-voltage, high-efficiency, low-ripple DC to DC buck converters and two low-noise LDOs. Using the RF6590 in handset applications can reduce transceiver battery current by up to 50%. Each DC to DC converter has a PWM and a PFM controller to enhance efficiency at light load current conditions. Over-current protection is employed to protect the device during a fault mode.

### Ordering Information

| | |
|---|---|
| RF6590 | Power Management IC |
| RF6590PCBA-41X | Fully Assembled Evaluation Board |

### Optimum Technology Matching® Applied

| | | | |
|---|---|---|---|
| ☐ GaAs HBT | ☐ SiGe BiCMOS | ☐ GaAs pHEMT | ☐ GaN HEMT |
| ☐ GaAs MESFET | ☐ Si BiCMOS | ☑ Si CMOS | ☐ RF MEMS |
| ☐ InGaP HBT | ☐ SiGe HBT | ☐ Si BJT | ☐ LDMOS |





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## Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Battery Voltage | -0.30 to +6.00 | V |
| Short Circuit at Output | No damage | |
| Storage Temperature | -65 to +125 | °C |
| Operating Temperature | -30 to +85 | °C |
| Moisture Sensitivity | MSL1 | Per J-STD-020 |

**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).



| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Overall** | | | | | All Nominal Test Conditions Unless Otherwise Stated, ($V_{BATT}$=3.8V, Temp.=25°C.) |
| Battery Voltage ($V_{BAT}$) | 2.90 | 3.80 | 5.10 | V | |
| Reduced Performance 1 ($V_{BAT}$) | 2.70 | | 2.90 | V | IC must remain functional. Output 3A and 3B are allowed to fall below specified tolerance range. Ripple and noise requirements do not need to be fulfilled |
| Reduced Performance 2 ($V_{BAT}$) | 2.50 | | 2.70 | V | Only in >SLEEP< and >CLOCK< (Output 3B is off), IC must remain functional, Output 3A is allowed to fall down to 2.49V at a load current of 5mA, Ripple and noise requirements not fulfilled |
| **General** | | | | | |
| OFF | | | | | |
| Total Leakage Current | | 3 | 10 | µA | VDD_IO=0, CLK_ON=0; Output 1, 2, 3A, and 3B OFF, No Load |
| Power Mode >SLEEP< | | | | | |
| Total Loss Current | | 18 | 25 | µA | VDD_IO=1, CLK_ON=0; Output 1, 3A, and 3B OFF, Output 2 in >SLEEP<, No Load |
| Power Mode >CLOCK< | | | | | |
| Total Loss Current | | 440 | 500 | µA | VDD_IO=1, CLK_ON=1; Output 1 and 3B OFF, Output 2 and 3A in >CLOCK<, No Load |
| Power Mode >TRX< | | | | | |
| Total Loss Current | | 770 | 850 | µA | VDD_IO=1, CLK_ON=1, via SPI; Output 1, 2, 3A, and 3B in Nominal Operation, >TRX<, No Load |





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| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Hardware Control Lines** | | | | | |
| VDD_IO High Level | 1.15 | 1.2 | 1.25 | V | Logic HIGH state depends on the operating voltage of the baseband or transceiver unit that drives VDD_IO, CLK_ON, and three SPI logic lines. |
| | 1.17 | 1.8 | 1.85 | V | |
| CLK_ON Low Level Threshold | | | 0.3*VDD_IO | V | |
| CLK_ON High Level Threshold | 0.7*VDD_IO | | | V | |
| Note: Basic loss currents above are understood to be independent from Output current. | | | | | |
| **SPI (Serial Peripheral Interface)** | | | | | |
| Logic Levels | | | | | |
| Input Low Level | | | 0.55 | V | SPI_CLK, SPI_SS, SPI_DRW |
| Input High Level | 1.2 | | | V | SPI_CLK, SPI_SS, SPI_DRW |
| Output Low Level | | | 0.35 | V | SPI_DRW |
| Output High Level | 1.5 | | | V | SPI_DRW |
| Multi-Device SPI Requirements | | | | | |
| Input Capacitance | | | 6.0 | pF | SPI_CLK, SPI_SS, SPI_DRW |
| Output Load Capacitance (Driven by PMU) | 36.0 | | | pF | SPI_DRW |
| Communication Speed | | | | | |
| Nominal Clock Rate | 6.5 | | 26.0 | MHz | SPI_CLK |
| Clock Frequency | 0.1 | | | | |
| Clock Duty Cycle | 45 | 50 | 55 | % | |
| Data Setup Time | 13.2 | | | ns | in read mode |
| Data Hold Time | 13.2 | | | ns | in read mode |
| Data Setup Time | 4 | | | ns | in read mode |
| Data Hold Time | 15.8 | | | ns | in read mode |
| **Output 1** | | | | | |
| Power Mode >TRX< (upon SPI programming): | | | | | |
| Nominal Output Voltage | 1.044 | 1.080 | 1.116 | V | Including ripple |
| Load Current | | 40 | 100 | mA | |
| Efficiency at 1mA Load Current | 75 | 83 | | % | Auto Mode |
| Efficiency ≥5mA Load Current | 76 | 83 | | % | Auto Mode |
| Efficiency ≥20mA Load Current | 78 | 87 | | % | Auto Mode |
| **Output 2** | | | | | |
| Power Mode >SLEEP< (VDD_IO=1, CLK_ON=0): | | | | | |
| Nominal Output Voltage | 1.700 | 1.800 | 1.920 | V | |
| Load Current | | 0.02 | 5.00 | mA | |
| Power Mode >CLOCK< (VDD_IO=1, CLK_ON=1): | | | | | |
| Nominal Output Voltage | 1.683 | 1.740 | 1.797 | V | Including Ripple |
| Load Current | | | 50 | mA | |
| Efficiency at 1mA Load Current | 81 | 87 | | % | |
| Efficiency ≥5mA Load Current | 83 | 88 | | % | |



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| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Output 2, cont.** | | | | | |
| Power Mode >TRX< (upon SPI programming): | | | | | |
| Nominal Output Voltage | 1.683 | 1.740 | 1.797 | V | |
| Output Voltage Tolerance in PFM Mode | 1.683 | 1.740 | 1.797 | V | Including Ripple |
| Output Voltage Tolerance in PWM Mode | 1.702 | 1.740 | 1.778 | V | Including ripple |
| Load Current | | 90 | 170 | mA | |
| Efficiency at 1mA Load Current | 81 | 87 | | % | Auto Mode |
| Efficiency ≥5mA Load Current | 78 | 88 | | % | Auto Mode |
| Efficiency ≥20mA Load Current | 78 | 91 | | % | Auto Mode |
| **Output 3A** | | | | | |
| Power Mode >CLOCK< (VDD_IO=1, CLK_ON=1): | | | | | |
| Nominal Output Voltage | 2.712 | 2.810 | 2.903 | V | Including Ripple |
| Load Current | | | 15 | mA | |
| Efficiency at 1mA Load Current | 90 | 91 | | % | |
| Efficiency ≥5mA Load Current | 90 | 93 | | % | |
| Power Mode >TRX< (Upon SPI Programming): | | | | | |
| Nominal Output Voltage | 2.712 | 2.810 | 2.903 | V | Including Ripple |
| Load Current | | 80 | 160 | mA | (including supply current for Output 3B) |
| Efficiency at 1mA Load Current | 87 | 91 | | % | Auto Mode |
| Efficiency ≥5mA Load Current | 87 | 93 | | % | Auto Mode |
| **Output 3B** | | | | | |
| Power Mode >TRX< (upon SPI Programming): | | | | | |
| Nominal Output Voltage | -40 | Output 3A-200 | +40 | mV | Follows Output 3A with fixed 200mV drop, $V_{OUT}$ DAC set to 2.81V |
| Load Current | | | 90 | mA | |

## Operational Notes

### Truth Table

| (fm BB) | (fm XCVR) | | Control | DC to DC | DC to DC | LDO | DC to DC | LDO |
|---|---|---|---|---|---|---|---|---|
| **VDD_IO** | **CLK_ON** | **Mode** | **SPI** | **Output 1** | **Output 2** | **Output 2** | **Output 3A** | **Output 3B** |
| Low | Low | OFF | Off | Off | Off | Off | Off | Off |
| High | Low | SLEEP | Off | Off | Off | 1.8V (<5mA) | Off | Off |
| High | High | CLK | Off | Off | 1.74V Forced PFM <50mA | Off | 2.81V Forced PFM <15mA | Off |
| High | High | TRX* | On | 1.08V Auto PWM/PFM (<100mA) | 1.74V Auto PWM/PFM <170mA | Off | 2.81V Auto PWM/PFM <70mA | 2.61V<90mA Powered from Out3A |

*Programmed via SPI Interface

### Typical Power on Sequence

1. Apply VBATT
2. Apply VDD_IO
3. Apply CLK_ON
4. Write to register to enable TRX mode

### Typical Power off Sequence

Power off sequence is in the opposite order of Power on Sequence.

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# RF6590 Operational Description

## Overview

The RF6590 power management IC is designed to work in a transceiver application with four modes of operation requiring up to four Output voltages in TRX mode (Output 1 and Output 3A are DC to DC converters, Output 2 is a parallel DC to DC converter/LDO, and Output 3B is an LDO). Mode-to-mode control is achieved with a combination of GPIO pins (VDD_IO and CLK_ON) and SPI. In addition, features such as the Output voltage can be adjusted through SPI programming.

## Operation by Mode

**Off Mode**

- GPIO: VDD_IO and CLK_ON = logic 0.
- SPI: None.

Description: In this mode of operation the RF6590 is completely shutdown (no Output voltages are generated). Only process leakage currents are drawn from the battery. Default states for Output 1, Output 3A and Output 3B are high impedance while for Output 2 it is pull-down.

**SLP Mode**

- GPIO: VDD_IO= logic 1 (1.2V or 1.8V), and CLK_ON = logic 0.
- SPI: None.

Description: In this mode of operation only the ultra low current Output 2 LDO is enabled. The Output voltage is nominally 1.80V and load current is less than 5mA. Max Output voltage settling time is 100µs.

**CLK Mode**

- GPIO: VDD_IO and CLK_ON = logic 1 (both 1.2V or 1.8V must be same voltage level).
- SPI: None.

Description: In this mode of operation, the Output 2 LDO is disabled and the Output 2 DC to DC converter is enabled in forced PFM mode. Nominal Output voltage for Output 2 in CLK mode is 1.74V and the max load current is 50mA. Output 3A DC to DC converter is enabled in this mode, also in forced PFM mode. Output 3A employs a soft-start feature to limit the in-rush current. No similar feature is employed on Output 2 since the external devices are already pre-charged in SLP mode. Output 3A nominal Output voltage is 2.81V and max load current is 15mA.

**TRX Mode**

- GPIO: VDD_IO and CLK_ON = logic 1 (both 1.2 V or 1.8 V must be same voltage level).
- SPI: Use to enable/disable all Output and program Output voltages.

Description: This mode of operation begins when the transceiver internal LDO on Output 2 is enabled and used to pre-charge the external capacitors on Output 1. Once pre-charge is complete, Output 1, 2, and 3A are enabled through the SPI port. Nominal Output voltage for Output 1 is 1.08V (100mA max), for Output 2 is 1.74V (170mA max), and for Output 3A is 2.81V (160mA max).

Since Output 1 is pre-charge the controller starts in forced PFM for ~10µs, giving the transceiver internal LDO time to shutdown. This is described as the override mode of operation for Output 1. Output 1 DC to DC converter will run (per SPI programmability) in auto PFM/PWM mode, based on load current. Once enabled through the SPI, Output 2 and Output 3A DC to DC converters will also transition from forced PFM mode to auto PFM/PWM control. Output 3B LDO (2.65V nominally, 90mA max) will be enabled through the SPI port only during TX mode (not RX). Note that the supply for the Output 3B LDO is the Output 3A DC to DC converter. As a result, the max load current of 90mA is included in the Output 3A max load current of 160mA. Output 3B also employs an override mode similar to Output 1. An internal transceiver LDO will pre-charge Output 3B prior to RF transmission, then Output 3B is enabled through the SPI port and finally then the internal transceiver LDO is shutdown. In order to minimize the effect of ripple noise on the transceiver during RF transmission the DC to DC converters can be transiently switched into forced PWM mode. After transmission is complete the controllers can resume auto PFM/PWM operation to realize the efficiency benefits.

**Shutdown Sequence**
Typical shutdown mode-to-mode sequencing for the RF6590 is in the reverse order as described above: TRX, CLK, SLP, and OFF. Although this is the recommended sequence, it is not harmful if it not followed explicitly.

## Fault Management

The RF6590 is over-current fault protected in all modes of operation. In CLK mode, with Output 2 and Output 3A DC to DC converters running in forced PFM mode, the converters are inherently over-current protected. In TRX mode, with the DC to DC converters running in auto PFM/PWM mode, the affected converter will automatically be disabled, the affiliated over-current bit is set and a parallel over-current LDO enabled in order to maintain the Output voltage. If the LDO cannot maintain the desired Output voltage, the affected Output is shutdown after ~20μs. The Output can be reset through the SPI port. If the fault persists the Output will shut down again.

## Other Operational Notes

- Logic HIGH state must be 1.2 volts OR 1.8 volts, depending on the operating voltage of the baseband or transceiver unit that drives VDD_IO, CLK_ON, and three SPI logic lines.
- SPI logic voltage should not exceed 1.8 volts (Output 2 supply) during operation.
- Do not exceed listed currents in CLK mode, otherwise the Output voltage will fall out of regulation.
- Register 0 must be restored by the controller, whenever the mode enters TRX mode. All registers should be considered volatile in OFF mode. The user needs to reprogram all registers after each power cycle (VDD_IO goes low).
- Output 3B current is sourced from Output 3A, so the combined load current should not exceed 160mA.
- In TRX mode, each DC to DC converter independently switches between PFM and PWM modes, depending on load current, unless the control register bit is set for forced PWM or forced PFM mode.
- SPI mode is only enabled after RF6590 is in CLK state (after a 10μs waiting period). The chip transitions to TRX mode when the OUTxTRX bits are set from 0 to 1. These are 4MSB in register 0. [Reg 0, Ctrl (15:12)]
- Supply source for all Output is the VPWR pin and references to the PGND pin. See Application Notes from RFMD on suggested layout patterns to minimize current loops and stray noise coupling.
- VANA and reference AGND provide the current to operate internal control circuits.



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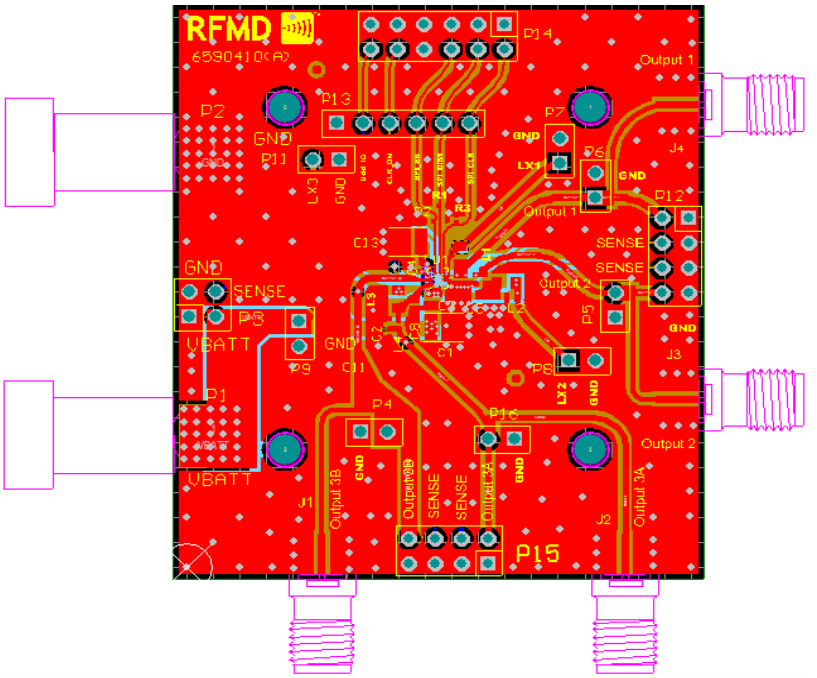
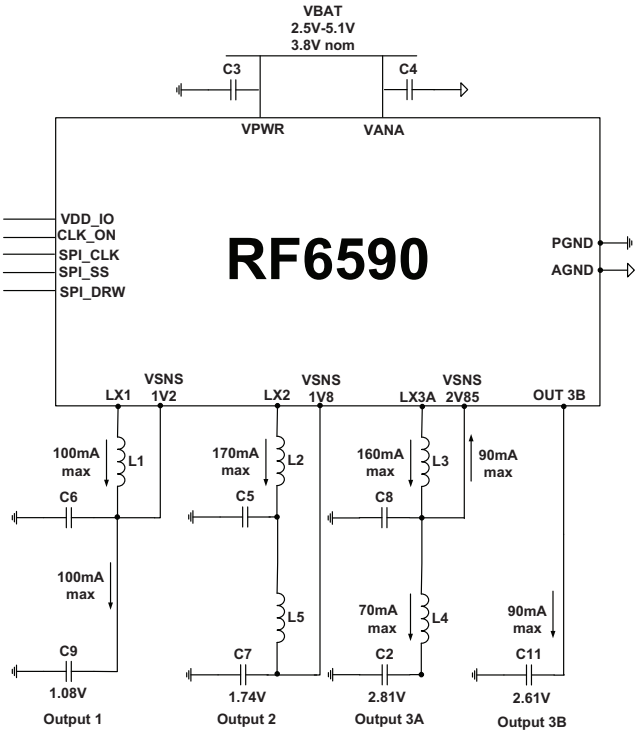
## Evaluation Board Layout

Board Thickness 0.042, Board Material FR-4



## Application Schematic




## Recommended BOM

| Designator | Case Size | Quantity | Value |
|---|---|---|---|
| C3 | 0603 | 1 | 4.7µF |
| C4 | 0402 | 1 | 1.0µF |
| L1 | 2.0x1.25x1.0 | 1 | 4.7µH |
| C6 | 0402 | 1 | 2.2µF |
| C9 | 0402 | 1 | 1.0µF |
| L2 | 2.0x1.25x1.0 | 1 | 4.7µH |
| C5 | 0603 | 1 | 4.7µF |
| L5 | 0402 | 1 | 15nH |
| C7 | 0402 | 1 | 4.7µF |
| L3 | 2.0x1.25x1.0 | 1 | 4.7µH |
| C8 | 0603 | 1 | 4.7µF |
| L4 | 0402 | 1 | 15nH |
| C2 | 0402 | 1 | 1.0µF |
| C11 | 0402 | 1 | 4.7µF |



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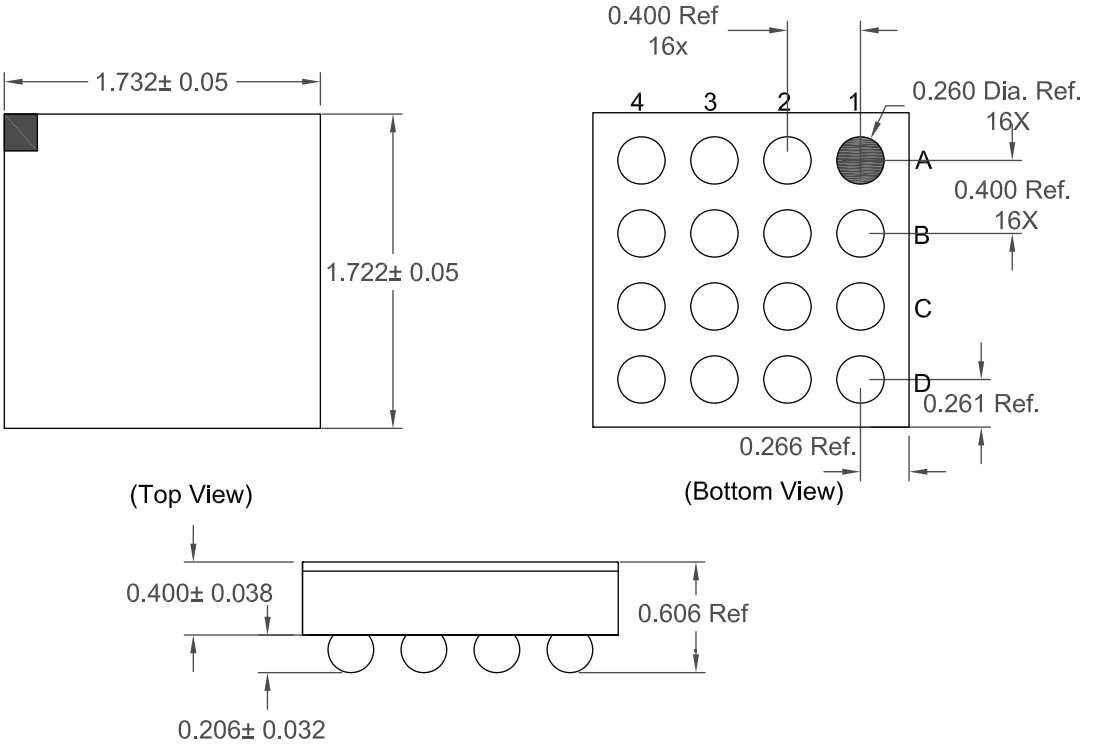
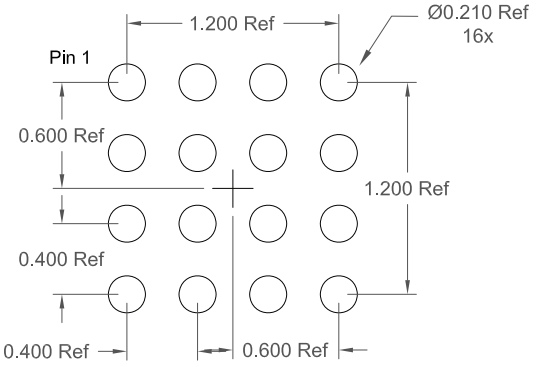
## Package Drawing

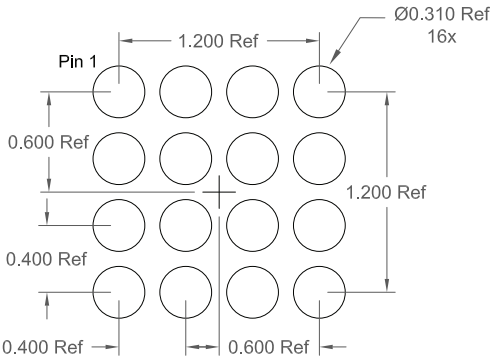



Notes:
1. Shaded area represents Pin 1 location.
2. All bumps are attached in the package with 0.21mm diameter UBM.

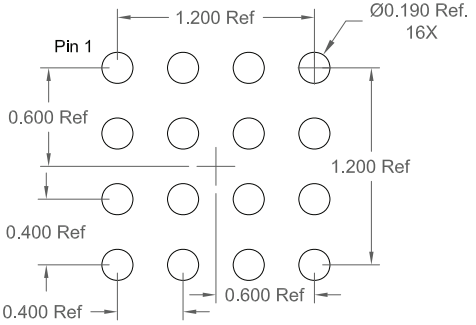
## Metal, Solder, Stencil Pattern




PCB METAL LAND PATTERN




PCB SOLDER MASK PATTERN




PCB STENCIL PATTERN



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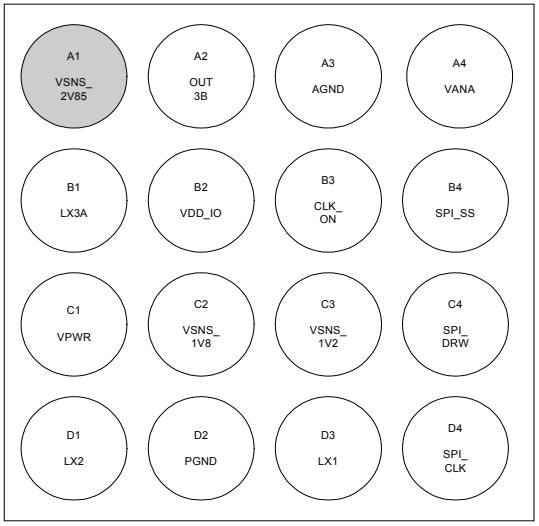
## Pin Description

| Pin | Function | Description |
|---|---|---|
| A1 | VSNS_2V85 | Feedback node from DC to DC Converter Output 3A (2.81 V). |
| A2 | OUT 3B | 2.61 V LDO. |
| A3 | AGND | Analog Ground. |
| A4 | VANA | Power supply used for analog circuitry. |
| B1 | LX3A | DC to DC Converter Output 3A. Connect to the filter inductor as recommended on application schematic. |
| B2 | VDD_IO | Along with CLK_ON pin, determines mode of operation. See Truth Table. |
| B3 | CLK_ON | Along with VDD_IO pin, determines mode of operation. See Truth Table. |
| B4 | SPI_SS | Serial Interface enable signal. |
| C1 | VPWR | Power Supply Voltage. |
| C2 | VSNS_1V8 | Feedback node from DC to DC Converter Output 2 (1.74 V). |
| C3 | VSNS_1V2 | Feedback node from DC to DC Converter Output 1 (1.08 V). |
| C4 | SPI_DRW | Serial Interface data signal for read and write access. |
| D1 | LX2 | DC to DC Converter Output 2. Connect to the filter inductor as recommended on application schematic. |
| D2 | PGND | Power Ground. |
| D3 | LX1 | DC to DC Converter Output 1. Connect to the filter inductor as recommended on application schematic. |
| D4 | SPI_CLK | Serial Interface clock input. |

## Pin Out




Top View