RFHA1101

4.3W GaN ON SiC POWER AMPLIFIER DIE-ON-CARRIER

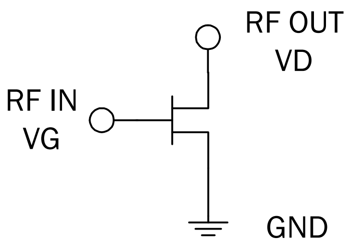
Package: Die

Features

- Broadband Operation DC to 10GHz [1]
- Advanced GaN HEMT Technology
- Small Signal Gain=21.4dB at 2.14GHz
- 28V Typical Performance
  - Output Power 4.3W at P3dB
  - Drain Efficiency 60% at P3dB
- Dimensions
  - GaN die: 0.448 x 0.825 x 0.1mm
  - GaN die on Heat Sink: 1.25 x 1.25 x 0.3mm
- Active Area Periphery: 2.22mm

Applications

- Commercial Wireless Infrastructure
- Cellular and WiMAX Infrastructure
- Civilian and Military Radar
- General Purpose Broadband Amplifiers
- Public Mobile Radios
- Industrial, Scientific and Medical



Functional Block Diagram

Product Description

The RFHA1101 is a 28V, 4.3W, GaN on SiC high power discrete amplifier die-on-carrier designed for commercial wireless infrastructure, cellular and WiMAX infrastructure, industrial/scientific/medical, and general purpose broadband amplifier applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, the RFHA1101 is able to achieve high efficiency and flat gain over a broad frequency range in a single amplifier design with proper heat sinking and assembly. The RFHA1101 is an unmatched 0.5μm gate, GaN transistor die suitable for many applications with >36dBm 3dB-compressed power, >60% 3dB-compressed drain efficiency, and >21dB small signal gain at 2GHz.

Ordering Information

RFHA1101 4.3W GaN on SiC Power Amplifier Die-on-Carrier

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☑ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

1. Based on 10dB power gain extrapolated from f_{MAX}

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	155	V
Gate Voltage (V_G)	-6 to +2	V
Gate Current (I_G)	2.2	mA
Operational Voltage	28	V
Storage Temperature Range	-55 to +100	°C
Operating Junction Temperature (T_J)	200	°C
MTTF (T_J < 200°C, 95% Confidence Limits)*	1.8×10^7	Hours
Thermal Resistance, R_{TH} (Junction to case)** measured at TC=85°C, DC bias only.	12.5	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table below.

* MTTF - median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.

** User will need to define this specification in the final application and ensure bias conditions satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH}$ J-C and $T_C = T_{CASE}$ to maintain maximum operating junction temperature and MTTF

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		28		V	
Gate Voltage (V_{GSQ})		-0.96		V	V_D=28V, I_D=44mA
Drain Bias Current		44		mA	
Frequency of Operation	DC		10	GHz	Based on 10dB power gain, calculated from f_{MAX}
DC Functional Test					
V_G (on) - Forward Bias Diode Gate Voltage	0.4	0.95	1.2	V	I_G=2.22mA, V_D=0V
BV (off) - Drain Breakdown Voltage	100	>150		V	V_G=-4V, I_D=2.22mA
V_{PO} - Threshold Voltage	-1.9	-1.48	-1.1	V	V_D=20V, I_D=2mA
Die Capacitance from on-wafer CV measurements					
C_{RSS}		60		f_F	V_D=28V, I_D=44mA
C_{ISS}		5460		f_F	V_D=28V, I_D=44mA
C_{OSS}		895		f_F	V_D=28V, I_D=44mA
RF Small Signal Figures of Merit					On-wafer test
F_T		10		GHz	V_D=28V, I_D=170mA
F_{MAX} (based on G_{TU})		32		GHz	V_D=28V, I_D=170mA
F_T		7		GHz	V_D=28V, I_D=44mA
F_{MAX} (based on G_{TU})		27		GHz	V_D=28V, I_D=44mA
RF Typical Load Pull Performance					On-wafer tests [1,2,3,4]
Gain		21.4		dB	V_{DQ}=28V, I_{DQ}=44mA, CW, f=2140MHz, trade match[1]
Gain		19.4		dB	V_{DQ}=28V, I_{DQ}=44mA, CW, f=2700MHz, trade match[3]
Output Power at P3dB		36.3		dBm	V_{DQ}=28V, I_{DQ}=44mA, CW, f=2140MHz
Output Power at P3dB		35.8		dBm	V_{DQ}=28V, I_{DQ}=44mA, CW, f=2700MHz
Drain Efficiency at P3dB		60		%	V_{DQ}=28V, I_{DQ}=44mA, CW, f=2140MHz
Drain Efficiency at P3dB		60		%	V_{DQ}=28V, I_{DQ}=44mA, CW, f=2700MHz

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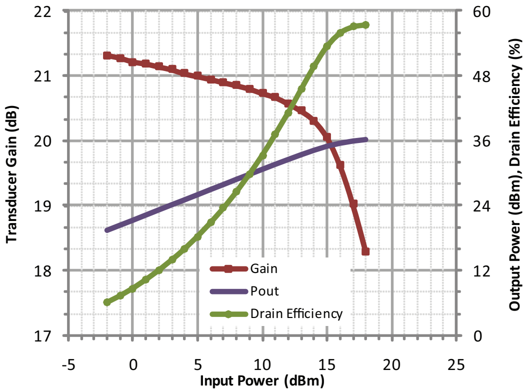
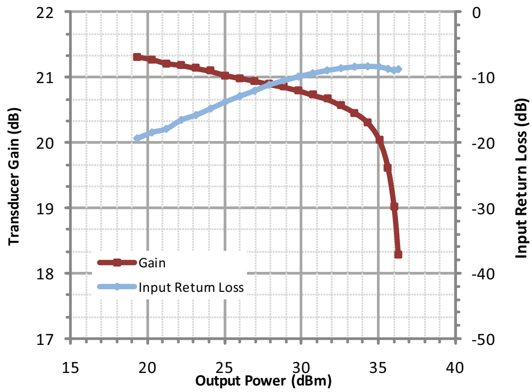
[1]Typical Performance at 2.14GHz when matched to a match point located midway between points of maximum gain and maximum efficiency

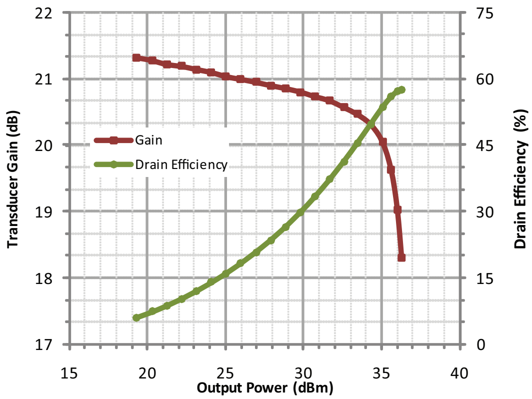
Gain/P_{OUT}/Efficiency vs. Input Power



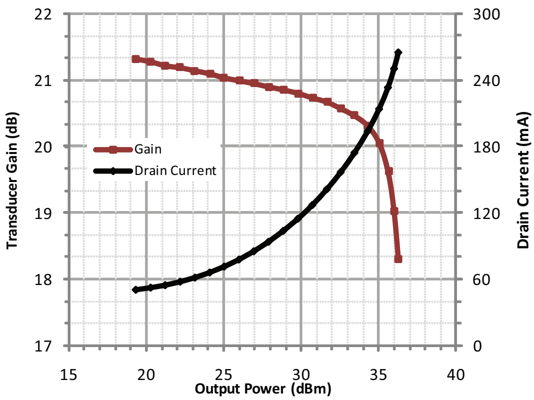
Gain/Input Return Loss vs. Output Power



Gain/Efficiency vs. Output Power



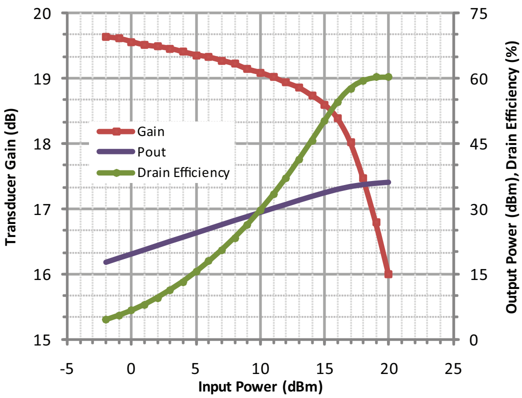
Gain/Drain Current vs. Output Power



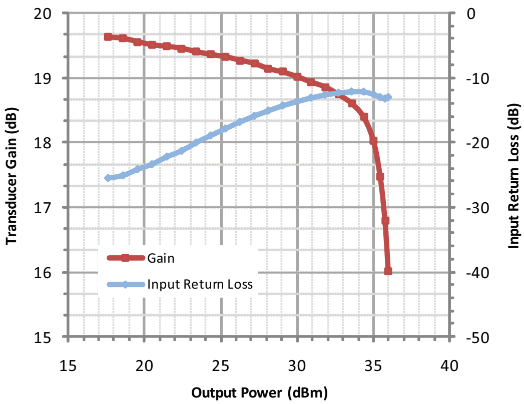
[2] Test Conditions: CW Operation, f=2140MHz, V_{DSQ}=28V, I_{DQ}=44.4mA, $T_{AMBIENT}$=25°C, measured with probes on-wafer, in Maury Microwave Load Pull Test System.

[3]Typical Performance at 2.7GHz when matched to a match point located midway between points of maximum gain and maximum efficiency

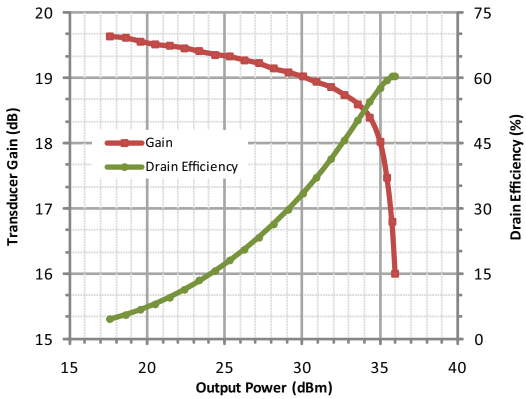
Gain/P_{OUT}/Efficiency vs. Input Power



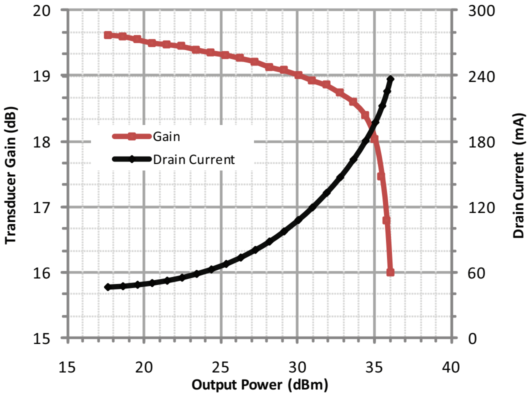
Gain/Input Return Loss vs. Output Power



Gain/Efficiency vs. Output Power



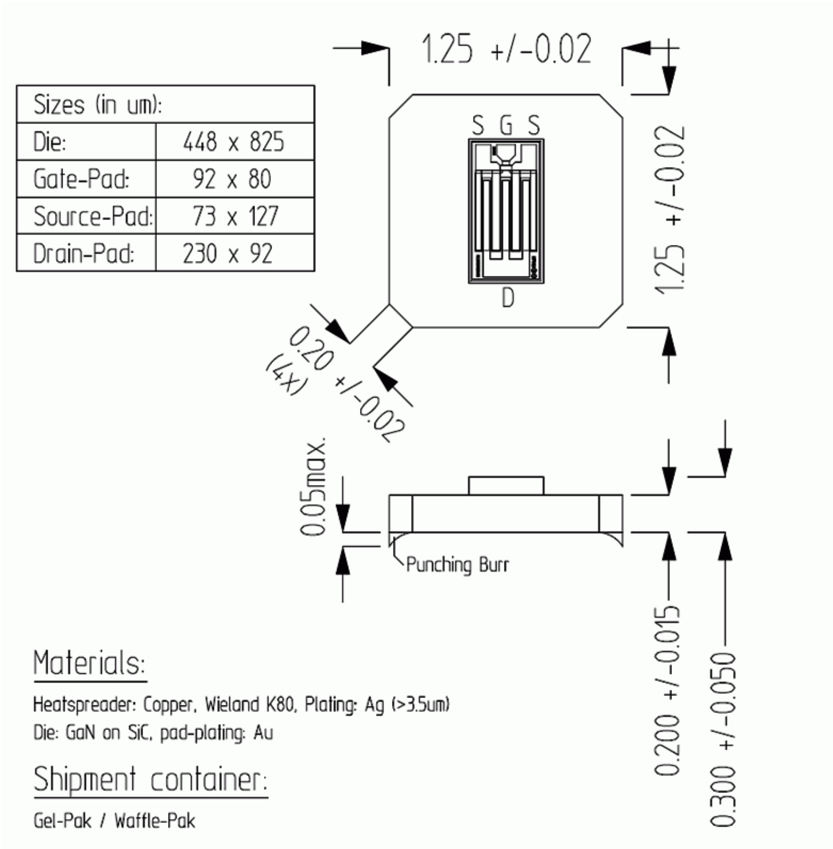
Gain/Drain Current vs. Output Power



[4] Test Conditions: CW Operation, f=2700 MHz, V_{DSQ}=28V, I_{DQ}=44.4mA, $T_{AMBIENT}$=25°C, measured with probes on-wafer, in Maury Microwave Load Pull Test System.

Package Drawing

(All dimensions in mm)



Bias Instruction for RFHA1101 Die

ESD Sensitive Material. Please use proper ESD precautions when handling devices die. Die must be mounted with minimal die attach voids for proper thermal dissipation. This device is a depletion mode HEMT and must have gate voltage applied for pinched off prior to applying drain voltage.

1. Mount device on carrier or package with minimal die attach voiding and applying proper heat removal techniques.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -4V to VG.
4. Apply 28V to VD.
5. Increase VG until drain current reaches desired bias point.
6. Apply RF input.

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Assembly Notes

Die Storage

- Individual bare die should be held in appropriately sized ESD waffle trays or ESD GEL packs.
- Die should be stored in CDA/N2 cabinets and in a controlled temperature and humidity environment.

Die Handling

- Die should only be picked using an automated or semi-automated pick system and an appropriate pick tool.
- Pick parameters will need to be carefully defined so as not to cause damage to either the top or bottom die surface.
- GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.
- RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

CAUTION: The use of inappropriate or worn-out ejector needle and improper ejection parameter settings can cause die backside tool marks or micro-cracks that can eventually lead to die cracking.

Die Attach

There are two commonly applied die attach processes: adhesive die attach and eutectic die attach. Both processes use special equipment and tooling to mount the die.

Eutectic Attach

- 80/20 AμSn preform, 0.5mil to 1mil thickness, made from virgin melt gold.
- Pulsed heat or die scrub attach process using automatic or semi-automatic equipment.
- Attach process carried out in an inert atmosphere.
- Custom die pick collets are required that match the outline of the die and the specific process employed using either pulsed, fixed heat, or scrub.
- Maximum temperature during die attach should be no greater than 320°C and for less than 30 seconds.
- Key parameters that need to be considered include: die placement force, die scrub profile, and heat profile.
- Minimal amount of voiding is desired to ensure maximum heat transfer to the carrier and no voids should be present under the active area of the die.
- Voiding can be measured using X-ray or Acoustic microscopy.
- The acceptable level of voiding should be determined using thermal modeling analysis.

Adhesive Attach

- High thermal silver filled epoxy is dispensed in a controlled manner and die is placed using as appropriate collet. Assembled parts are cured at temperatures between 150°C and 180°C.
- Always refer to epoxy manufacturer's data sheet.
- Industry recognized standards for epoxy die attach are clearly defined within MIL-883.

Early Life Screen Conditions

RFMD recommends an Early Life Screen Test that subjects this die to TJ=250°C (junction temperature) for at least 1 hour prior to field deployment.

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Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = - 8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$
$$C_{OSS} = C_{GD} + C_{DS}$$
$$C_{RSS} = C_{GD}$$

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