

Die: 3.1mmx1.45mmx0.102mm



Product Description

RFMD's SDA-1000 is a directly coupled (DC) GaAs microwave monolithic integrated circuit (MMIC) distributed driver amplifier die designed to support a wide array of high frequency commercial, military, and space applications. They are ideal for wideband amplifier gain blocks, broadband test equipment (ATE), military, and aerospace applications.

Features

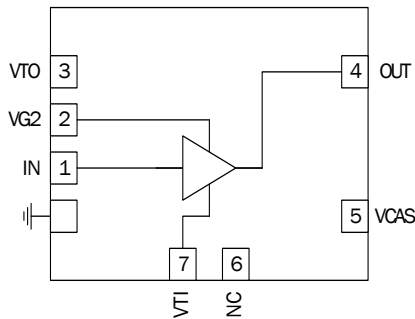
- DC to 20GHz Operation
- +26dBm P_{3dB}
- Gain = 14dB Typical
- Noise Figure = 4dB
- Output Voltage to 8V_{PP}
- 300mA Total Current

Applications

- Military
- Aerospace
- Broadband ATE
- Instrumentation

Optimum Technology Matching® Applied

- GaAs HBT
- GaAs MESFET
- InGaP HBT
- SiGe BiCMOS
- Si BiCMOS
- SiGe HBT
- GaAs pHEMT
- Si CMOS
- Si BJT
- GaN HEMT
- InP HBT
- RF MEMS
- LDMOS



Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					T _A = +25 °C, V _{DD} = +8V _{DC} , VG2 at +3.5V _{DC} , I _{DD} = 300mA
Operating Frequency	0		20	GHz	
Gain	13.8	14.5		dB	10GHz
Maximim Output Voltage		8		V _{P-P}	
IP3 at 10GHz		36		dBm	P _{OUT} ≅ 0dBm
P1dB at 10GHz		25		dBm	
P _{3dB} at 10GHz		26.5		dBm	
Noise Figure at Mid-Band		4		dB	
Input Return Loss		13		dB	
Output Return Loss		15			
Supply Current		300		mA	
Supply Voltage		8		V _{DC}	

*Adjust VTI between -1.5V_{DC} to +0.2V_{DC} to achieve I_{DD} = 300mA typical., VG2 = 3.5V_{DC} typ.

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Bias Voltage (V_{DD})	+9.0	V_{DC}
Gate Bias Voltage (V_{TI})	-2 to 0	V_{DC}
Gate Bias Voltage (V_{G2})	$(V_{DD}-8.0) V_{DC}$ to V_{DD}	V
RF Input Power ($V_{DD}=+8.0V_{DC}$)	20	dBm
Operating Channel Temperature (T_J)	+175	$^{\circ}C$
Continuous Power Dissipation ($T=+85^{\circ}C$)	3.5	W
Thermal Resistance (Pad to Die Bottom)	25	$^{\circ}C/W$
Storage Temperature	-40 to +150	$^{\circ}C$
Operating Temperature	-40 to +85	$^{\circ}C$
ESD JESD22-A114 Human Body Model (HBM)	Class 0 (All Pads)	



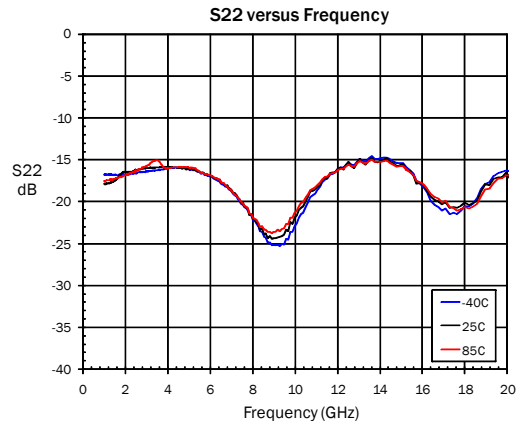
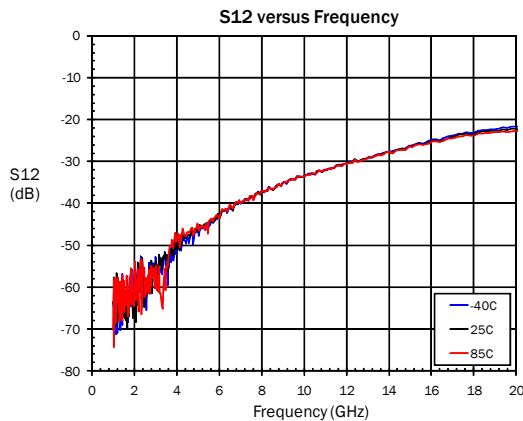
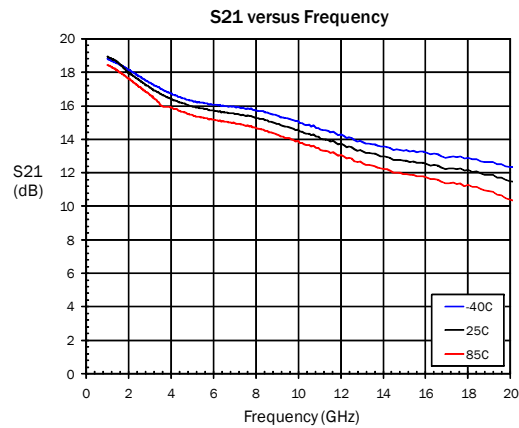
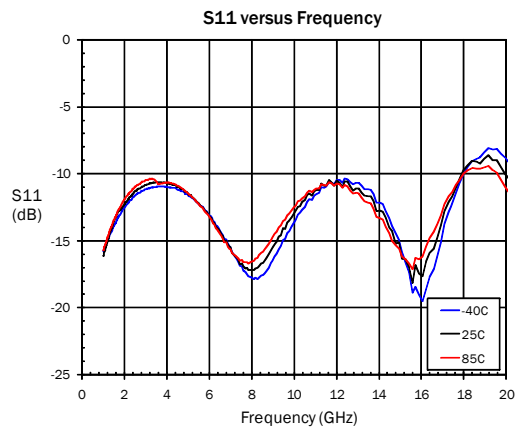
Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

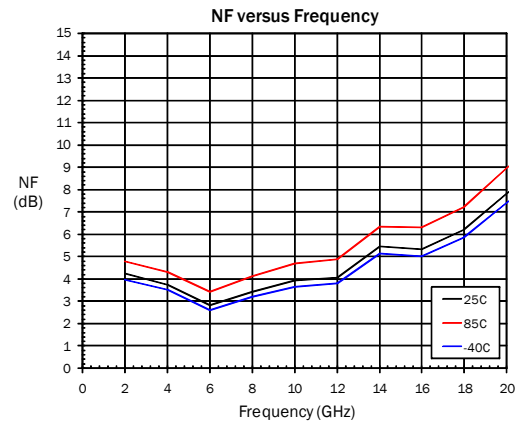
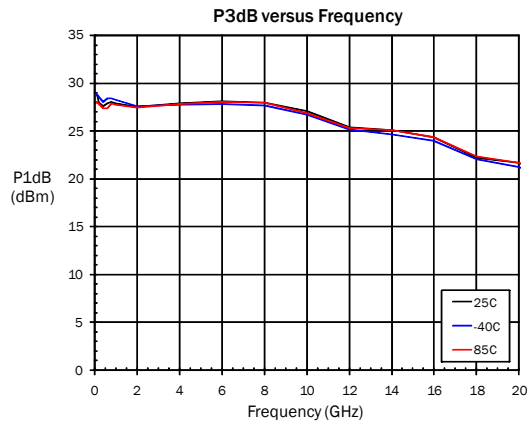
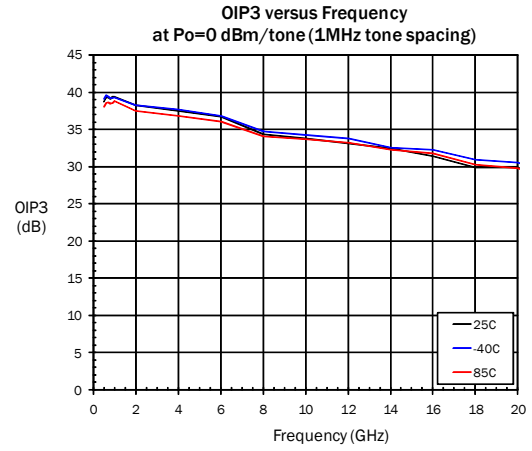
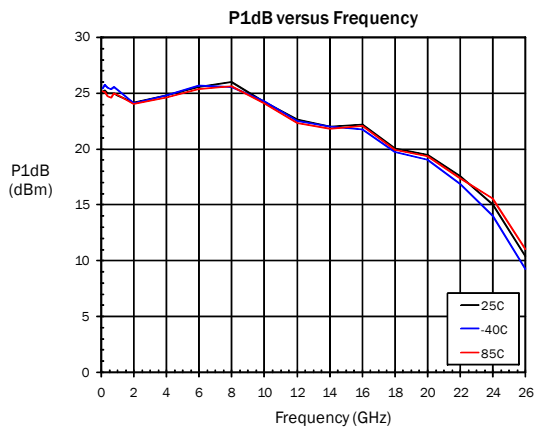
RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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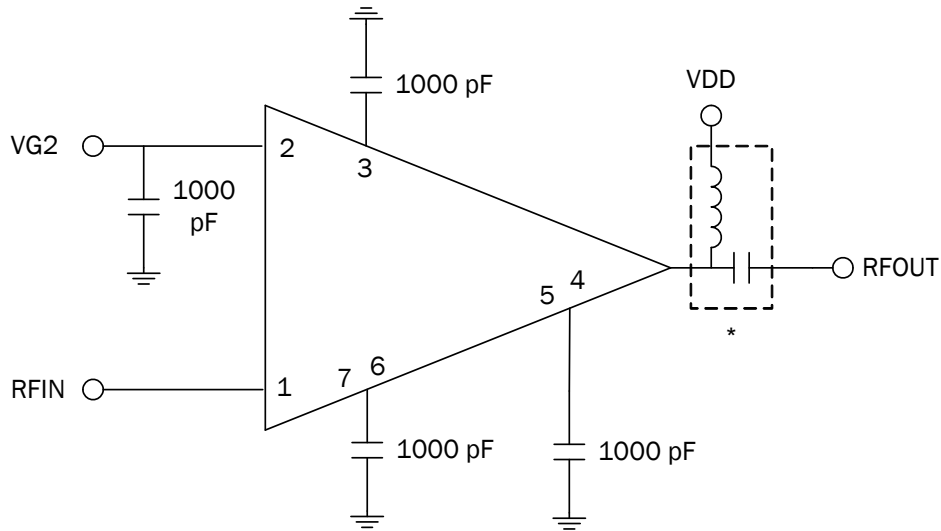
Typical Electrical Performance



Typical Performance (Circuit Board Data with Bias Tees) $V_S=5V$, $I_D=51mA$, $R_{BIAS}=33\Omega$



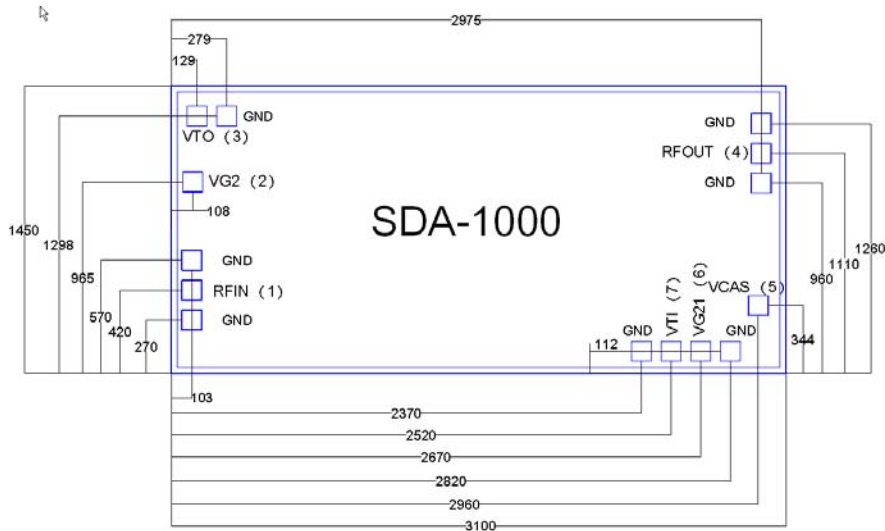
Application Circuit



*Note: Drain Bias (VDD) must be applied through a broadband bias tee or external bias network

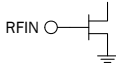
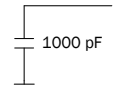
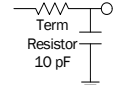
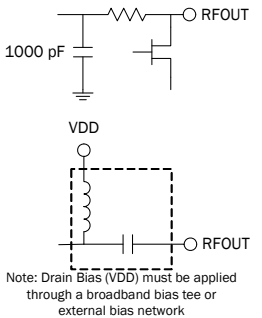
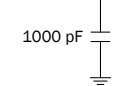
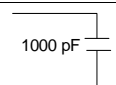
Package Drawing

Refer to drawing posted at www.rfmd.com for tolerances.

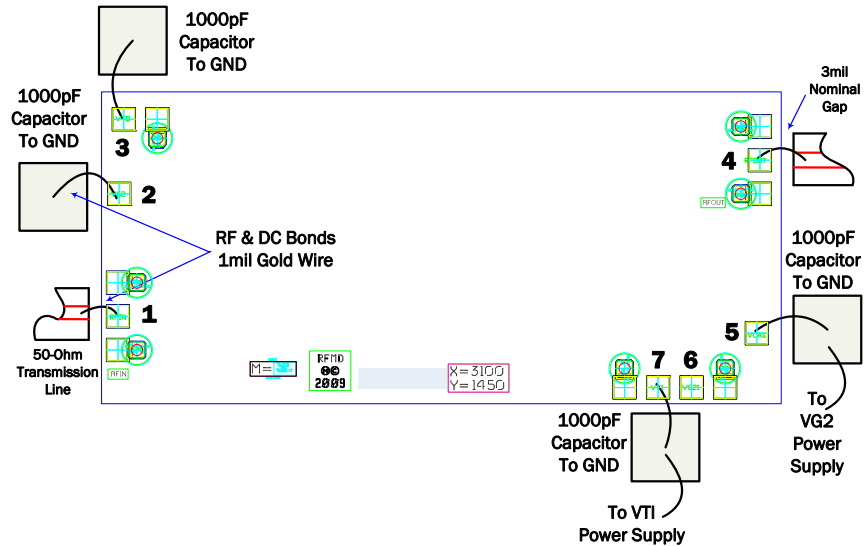


Notes:

1. All dimensions in microns
2. No connection required for ground bond pads
3. Die thickness is 0.102mm (4 MIL)
4. Typical bond pad is 0.100mm square
5. Backside metallization: gold
6. Backside metal is ground
7. Bond pad metallization: gold

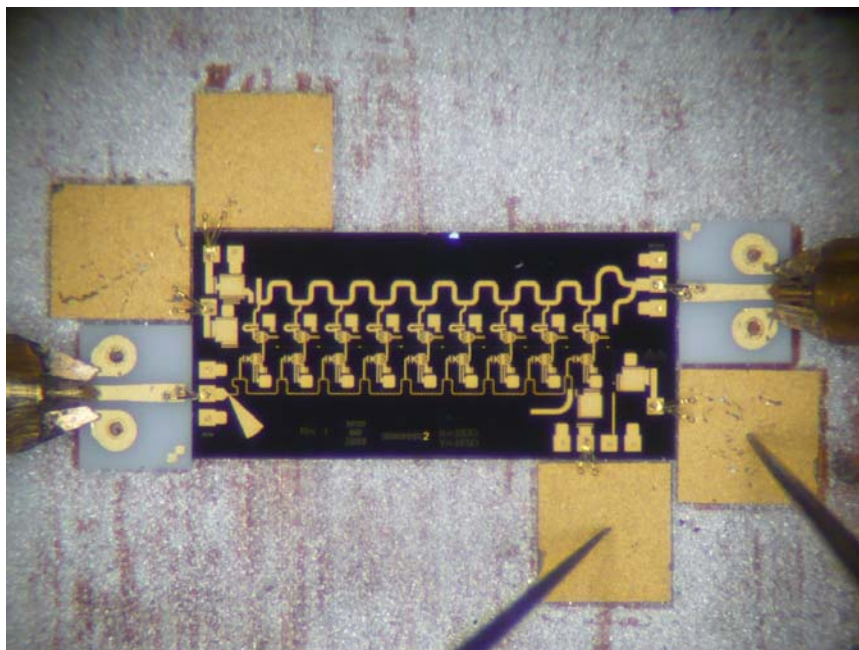
Pin	Function	Description	Interface Schematic
1	RFIN	RF Input. This pad is DC coupled and matched to 50Ω from DC to 20GHz. 50Ω microstrip transmission line on 0.127 mm (5mil) thick alumina thin film substrate is recommended for RF input and output.	
2	VG2	VG2 is an optional pad. It may be used to bias the cascode gate of the amplifier. If this port is used, a 1000 pF bypass capacitor with the shortest wirebond length possible is recommended to prevent low frequency gain ripple.	
3	VTO	The output drain termination pad. This pad requires a suggested 1000pF bypass capacitor with the shortest wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	
4	RFOUT and VDD	RF Output. 50Ω microstrip transmission line on 0.127 mm (5mil) thick alumina thin film substrate is recommended for RF input and output. Connect the DC bias (V_{DD}) network to provide drain current (I_{DD}).	
5	VCAS	Provides VG2 gate voltage to the cascode amplifier. The value is $\sim (V_{CC}/2 - \text{absolute value of } V_{TI})$.	
6	VG21	Not connected.	
7	VTI	Input gate voltage, used to bias the amplifier. The value is between $-1.5V_{DC}$ (device is pinched OFF) to $+0.2V_{DC}$ (fully ON). This pad requires a bypass capacitor to ground with the shortest possible wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	
Die	GND	Ground connection. Connect die bottom directly to ground plane for best performance. NOTE: The die should be connected directly to the ground plane with conductive epoxy.	

Assembly Diagram



Measurement Technique

All specifications and typical performances reported in this document were measured in the following manner. Data was taken using a temperature controlled probe station utilizing 150 μ m pitch GSG probes. The interface between the probes and integrated circuit was made with a coplanar to microstrip ceramic test interface. The test interface was then wire bonded to the die as shown in the figure below using 1mil diameter bondwires. The spacing between the test interface and the die was 200 μ m, and the bond wire loop height was 100 μ m. The thickness of the test interface is 125 μ m (5mil). The calibration of the test fixture included the probes and test interfaces, so that the measurement reference plane was at the point of bond wire attachment. Therefore, all data represents the integrated circuit and accompanying bond wires.



Ordering Information

Part Number	Description	Delivery Method	Die/GelPak
SDA1000	GaAs Distributed Amplifier, 20GHz, 3.10mmx1.45mm Die	GelPak	10 pcs or More
SDA1000SB	GaAs Distributed Amplifier, 20GHz, 3.10mmx1.45mm Die	GelPak	2 pcs

SDA-1000

