256Mb B-die UtRAM

(16Mb x16) Synchronous Burst Uni-Transistor CMOS RAM (1.7V ~ 1.95V)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- Preliminary datasheet.	Jan. 12, 2010	Preliminary	J.Y.Bae
0.5	- Corrected errata. - Revised General description. - Deleted Hardware /RESET. - t_{SKEW} : 15 -> 10[ns] - Revised Power Up Sequence timing. - Revised DC and operating characteristics. 1. Deleted I_{SPB} - Revised Mode Register Set. - Deleted MRS TIMING WAVEFORM ($\overline{PS}$ Pin). - Deleted PAR (Partial Array Refresh) mode.	Feb. 16, 2010	Preliminary	J.Y.Bae
0.6	- Changed tCSM from 2.5us to 1.7us. - Deleted $\overline{PS}$ pin.	Feb. 25, 2010	Preliminary	J.Y.Bae
1.0	- Final datasheet.	Apr. 16, 2010	Final	J.Y.Bae

Table Of Contents

256Mb B-die UtRAM

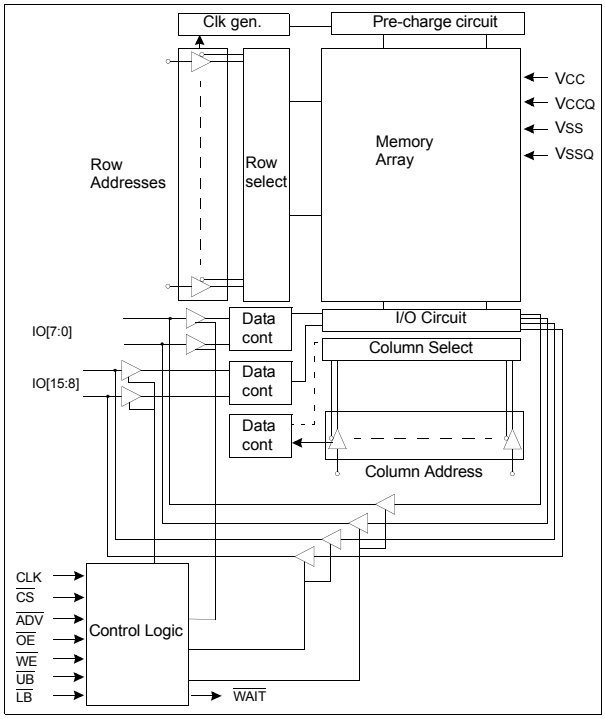
16M x 16 bit Synchronous Burst Uni-Transistor CMOS RAM

1.0 GENERAL DESCRIPTION

The world is moving into the mobile multi-media era and therefore the mobile handsets need bigger & faster memory capacity to handle the multi-media data. SAMSUNG's UtRAM products are designed to meet all the request from the various customers who want to cope with the fast growing mobile market. UtRAM is the perfect solution for the mobile market with its low cost, high density and high performance feature. K1B5616BFB is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous operation (asynchronous page read and asynchronous write) and the fully synchronous operation (synchronous burst read and synchronous burst write). These two operation modes are defined through the mode register setting. The device also supports the special feature for the standby power saving. That is internal TCSR (Temperature Compensated Self Refresh). The optimization of output drive strength is possible through the mode register setting to adjust for the different data loadings. Through this drive strength optimization, the device can minimize the noise generated on the data bus during read operation.

2.0 FEATURES

- Process technology: CMOS
- Organization: 16M x 16 bit
- Power supply voltage: 1.7V~1.95V
- Three state outputs
- Supports MRS (Mode Register Set)
  - Software set up
- Supports power saving modes
  - Internal TCSR (Temperature Compensated Self Refresh)
- Supports driver strength optimization
- K1B5616BFB supports
  - Asynchronous read / Asynchronous write
  - Synchronous burst read / Synchronous burst write
- Synchronous burst operation
  - Max. clock frequency : 108MHz
  - Fixed and Variable read latency
  - 4 / 8 / 16 / 32 and Continuous burst
  - Wrap / No-wrap
  - Latency : 4(Variable) @ 108MHz
    4(Variable) @ 104MHz
    3(Variable) @ 80MHz
    2(Variable) @ 66MHz
  - Burst stop
  - Burst read suspend
  - Burst write data masking



3.0 PRODUCT FAMILY

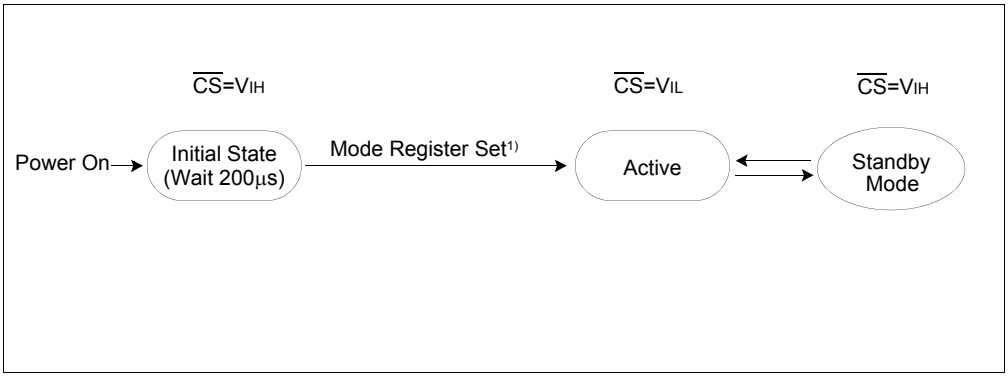
Product Family	Operating Mode[1)]	Operating Temp.	Vcc Range	Speed	Current Consumption	
					Standby (I_{SB1}, Max.)	Operating (I_{CC2P}, Max.)
K1B5616BFB-I	Mode 1 Mode 3	Industrial(-25~85°C)	1.7~1.95V	108MHz	TBD < 85°C TBD < 40°C	TBD

NOTE :
1) Mode1 : Asynchronous read / Asynchronous write
Mode3 : Synchronous burst read / Synchronous burst write

4.0 TERMINOLOGY DESCRIPTION

Name	Function	Type	Description
CLK	Clock	Input	Synchronizes the memory to the system operating frequency during synchronous operations. Commands are referenced to CLK.
$\overline{\text{ADV}}$	Address Valid	Input	Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of $\overline{\text{ADV}}$ during asynchronous READ and WRITE operations.
$\overline{\text{CS}}$	Chip Select	Input	$\overline{\text{CS}}$ low enables the chip to be active $\overline{\text{CS}}$ high disables the chip and puts it into standby mode.
$\overline{\text{OE}}$	Output Enable	Input	Enables the output buffers when LOW. when $\overline{\text{OE}}$ is HIGH, the output buffers are disabled.
$\overline{\text{WE}}$	Write Enable	Input	$\overline{\text{WE}}$ low enables the chip to start writing the data
$\overline{\text{LB}}$	Lower Byte (I/O0~7)	Input	$\overline{\text{UB}}$ ($\overline{\text{LB}}$) low enables upper byte (lower byte) to allow data Input/output from I/O buffers.
$\overline{\text{UB}}$	Upper Byte (I/O8~15)	Input	
A0~A23	Address0 ~ Address 23	Input	Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles.
I/O0~I/O15	Data Inputs / Outputs	Input/Output	Depending on $\overline{\text{UB}}$ or $\overline{\text{LB}}$ status, word(16-bit, $\overline{\text{UB}}$ & $\overline{\text{LB}}$ low) data, upper byte(8-bit, $\overline{\text{UB}}$ low & $\overline{\text{LB}}$ high) data or lower byte(8-bit, $\overline{\text{LB}}$ low & $\overline{\text{UB}}$ high) data is loaded
VCC	Voltage Source	Power	Device Power supply. Power supply for device core operation.
VCCQ	I/O Voltage Source	Power	I/O Power supply. Power supply for input/output buffers.
VSS	Ground Source	GND	Ground for device operation
VSSQ	I/O Ground Source	GND	Ground for Input/Output buffers
$\overline{\text{WAIT}}$	Valid Data Indicator	Output	The $\overline{\text{WAIT}}$ signal is output signal indicating the status of the data on the bus whether or not it is valid. $\overline{\text{WAIT}}$ is asserted when a burst crosses a word-line boundary. $\overline{\text{WAIT}}$ is asserted and should be ignored during asynchronous and page mode operations.

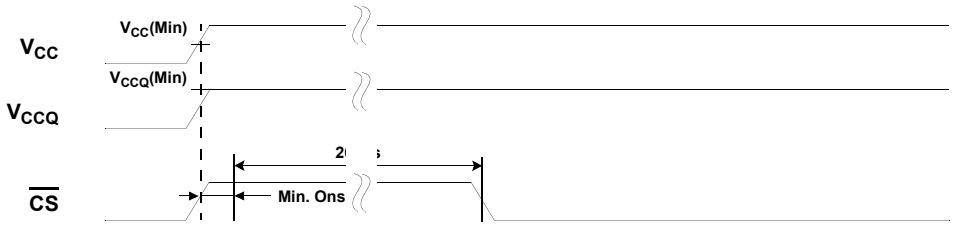
5.0 MODE STATE MACHINE



NOTE :
1) Refer to MRS(Mode Register Set)

6.0 POWER UP SEQUENCE

After V_{CC} and V_{CCQ} reach minimum operating voltage (1.7V), drive $\overline{CS}$ High first. Before V_{CC} and V_{CCQ} reach minimum voltage (1.7V) drive $\overline{PS}$ High. Then the device gets into the Power Up mode. Wait for minimum 200μs to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.
Mode1 (Asynchronous read/ Asynchronous write) is set up after power up, but this mode is not always guaranteed.



7.0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Power supply voltage relative to Vss	V_{CC}, V_{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-55 to +150	°C
Operating Temperature	T_A	-25 to 85	°C

NOTE :
1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

8.0 RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V_{CC}	1.7	1.8	1.95	V
Power supply voltage(I/O)	V_{CCQ}	1.7	1.8	1.95	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	0.8 x V_{CCQ}	-	V_{CCQ}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

NOTE :
1) T_A=-25 to 85°C, otherwise specified.
2) Overshoot: V_{CCQ} +1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3) Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

9.0 CAPACITANCE (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	6	pF

10.0 DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CCQ}		-2	-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=V_{SS} to V_{CCQ}		-5	-	5	μA
Average Operating Current(Async) [7]	I_{CC2}	Cycle time=min t_{RC}/min t_{WC}, I_{IO}=0mA[4], 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	35	mA
	I_{CC2P}	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA[4], 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	25	mA
Average Operating Current(Sync) [7]	I_{CC3}	Burst Length 4, Latency 5, 80MHz, I_{IO}=0mA[4], Address transition 1 time, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	35	mA
Output Low Voltage	V_{OL}	I_{OL}=0.1mA		-	-	0.2	V
Output High Voltage	V_{OH}	I_{OH}=-0.1mA		1.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1]	$\overline{CS}$≥V_{CCQ}-0.2V, $\overline{PS}$≥V_{CCQ}-0.2V, Other inputs=V_{SS} or V_{CCQ} (Toggle is not allowed)[5]	< 40°C	-	-	200	μA
			< 85°C	-	-	350	μA

NOTE :
1) I_{SB1} is measured after 60ms after $\overline{CS}$ high. CLK should be fixed at high or at Low.
2) Full Array Partial Refresh Current(I_{SBP}) is same as Standby Current(I_{SB1}).
3) Internal TCSR (Temperature Compensated Self Refresh) is used to optimize refresh cycle.
4) I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.
5) V_{IN}=0V; all inputs should not be toggle.
6) Clock should not be inserted between ADV low and WE low during Write operation.
7) When testing, this current is measured using Read and Write timing which portion is 50:50.

11.0 MRS (MODE REGISTER SET)

The mode registers store the values for the various modes to make UtRAM suitable for a various applications through MRS. There are two ways to perform MRS. One is $\overline{PS}$ pin MRS and the other is Software MRS. The mode registers have lots of fields and each field consists of several options. Refer to the Table below for detailed Mode Register Setting. A19~A23 addresses Should be "0" in Mode Register Setting.

11.1 MRS CODE

MRS code consists of 12 categories and several options in each category. BL, WC, Latency, Wrap, WP, MS and IL are related to bus operation and DS is related to device output impedance.

[Table 1] Mode Register Setting according to field of function

Address	A18	A17~A16	A15~A14	A13	A12	A11~A9	A8	A7~A5	A3	A2	A1~A0
Function	IL	DS	MS	WP	Wrap	Latency	WC	BL			

Initial Latency		Driver Strength			Mode Select		
A18	IL	A17	A16	DS	A15	A14	MS[1]
0	Fixed	0	0	Full Drive	0	0	Mode 1(Async. 4 Page Read / Async. Write)
1	Variable	0	1	1/2 Drive	1	0	Mode 3(Sync. Burst Read / Sync. Burst Write)
		1	0	1/4 Drive			

$\overline{WAIT}$ Polarity		Wrap		Latency Count				$\overline{Wait}$ Configuration		Burst Length			
A13	WP[1]	A12	Wrap	A11	A10	A9	Latency	A8	WC	A7	A6	A5	BL
0	Low Enable	0	Wrap	1	0	0	2	0	One clock prior	0	1	0	4 word
1	High Enable	1	No-Wrap	0	0	0	3	1	At data	0	1	1	8 word
				0	0	1	4			1	0	0	16 word
				0	1	0	5			1	0	1	32 word
				0	1	1	Reserve			1	1	1	Continuous[2]
				1	0	1	7						
				1	1	0	Reserve						
				1	1	1	Reserve						

NOTE :
- A4, A19 ~ A23 should be '0'
- The default modes are set automatically after power up.
  * Default modes: Async. Read and Async. Write / PAR disable, 1/2 Drive Strength

- Mode Change Rules.
  Mode1 to Mode3 : 1 dummy write(to any address with any data) is necessary before setting Mode3
  * Dummy write: Dummy write timing is just the same with normal write timing. It is necessary because 'Late write' is applied to Asynchronous write as in Mode1.
  * Late write: The data that is latched in previous write cycle is written in the address that is also latched in previous write cycle when Write starts. And current data and address are latched when Write ends. ($\overline{WE}$ high or $\overline{CS}$ high, whichever comes first)

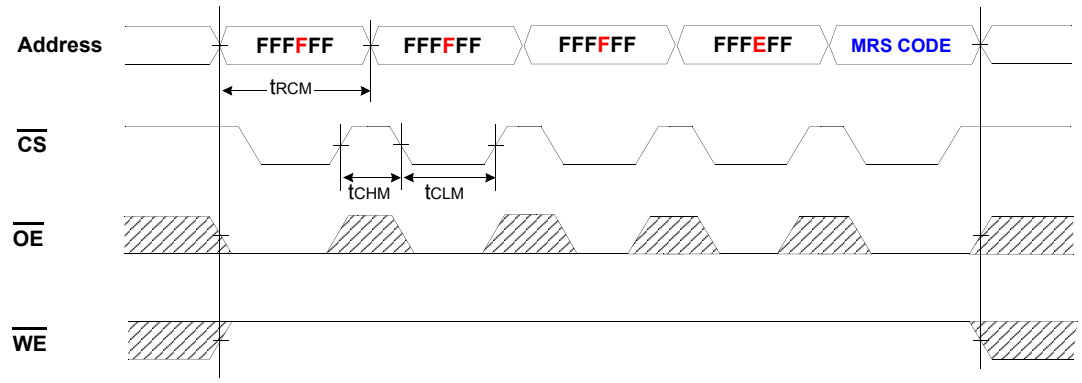
  Mode3 to Mode1 : 1 dummy write is necessary before setting Mode1
  * Dummy write: The data and the address should be the same with those which are used during Mode1 to Mode3 transition.

1) WP[0]; The data is available when $\overline{WAIT}$ signal is High. All the timings in this spec are illustrated based on this mode.
   WP[1]; The data is available when $\overline{WAIT}$ signal is Low.
2) Refresh command will be denied during continuous operation. $\overline{CS}$ low should not be longer than t_{CSM}(max 1.7us)
   The continous mode [A7:A6:A5 =111] must be set with No-Wrap mode [A12=1].

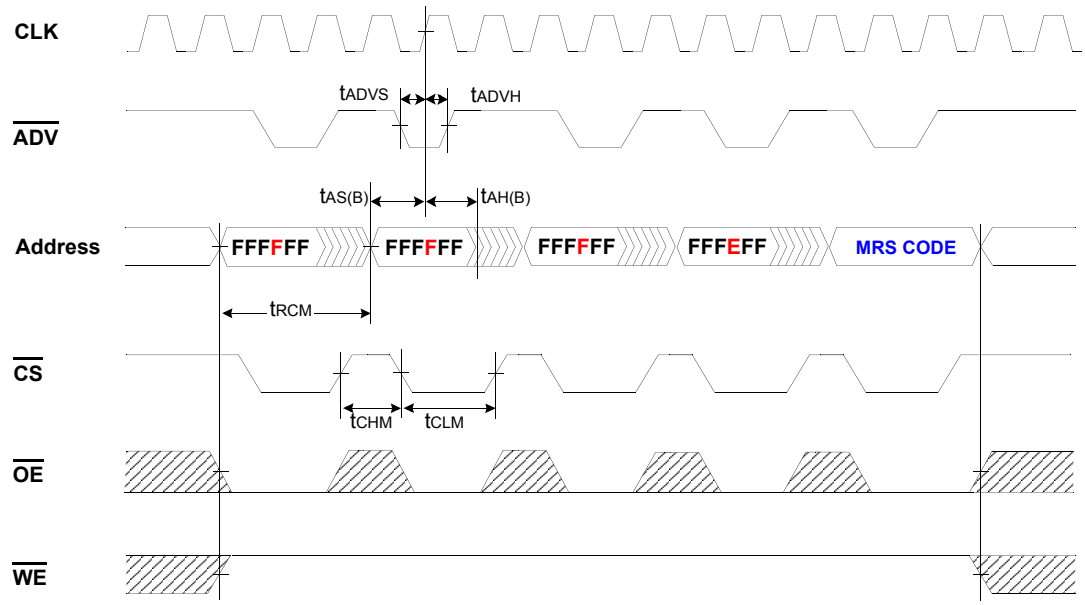
11.2 MRS TIMING WAVEFORM (SOFTWARE)

Software MRS timing consists of 5 Read cycles. 5 Read cycles should be operated in a row. Each cycle is normal Read cycle. $\overline{CS}$ pin should be toggling between cycles. 1st, 2nd and 3rd cycle should be FFFFFF(h), 4th cycle should be FFFEFF(h) and 5th cycle should be MRS code

Asynch. Mode Clock, $\overline{ADV}$, $\overline{UB}$ and $\overline{LB}$ = Don't care, $\overline{WAIT}$=High-Z



Synch. Mode $\overline{UB}$ and $\overline{LB}$ = Don't care



NOTE :
1) Above timing and address condition should not be used in the normal operation. The above condition should be used only for the mode register setting purpose.

[Table 2] AC CHARACTERISTICS

Parameter List	Symbol	Min	Max	Units	Parameter List	Symbol	Min	Max	Units
$\overline{ADV}$ setup time to clock	t_{ADVS}	3	-	ns	Read cycle time	t_{RCM}	70	-	ns
$\overline{ADV}$ hold time from clock	t_{ADVH}	2	-	ns	$\overline{CS}$ high time	t_{CHM}	10	-	ns
Address setup time to clock	$t_{AS(B)}$	3	-	ns	$\overline{CS}$ low time	t_{CLM}	60	-	ns
Address hold time from clock	$t_{AH(B)}$	2	-	ns					

11.3 Burst Length [A7~A5] & Wrap [A12]

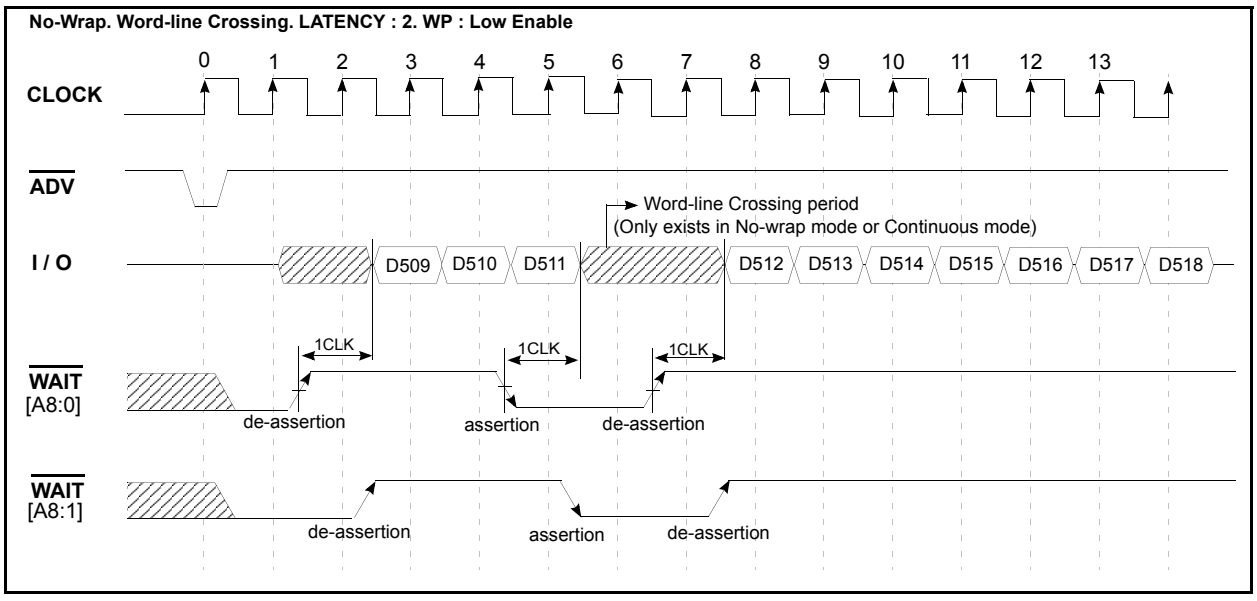
The device supports 4 word, 8 word, 16 word, 32 word and Continuous burst read or write. and Wrap & No-Wrap are supported for Burst sequence.

Burst Address Sequence(Decimal)					
Mode	**Start**	**4 word**	**8 word**	**16 word**	**32 word**
WRAP	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31 - 0
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31 - 0 - 1
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31- 0 - 1 - 2
	~		~	~	~
	7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7 - 8 - 9 - 10- 11- 12 ~ 2 - 3 - 4 - 5 - 6
	~			~	~
	15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20 ~ 10- 11- 12- 13- 14
	~				~
	31				31- 0 - 1 - 2 - 3 - 4 ~ 25-26-27-28-29-30
No-WRAP	0	0-1-2-3	0- 1- 2- 3- 4- 5- 6 -7	0- 1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-4	1- 2- 3- 4- 5- 6- 7- 8	1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31-32
	2	2-3-4-5	2- 3- 4- 5- 6- 7- 8- 9	2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31-32-33
	3	3-4-5-6	3- 4- 5- 6- 7- 8- 9-10	3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17-18	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31-32-33-34
	~		~	~	~
	7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7 - 8 - 9 - 10-11-12 ~ 33-34-35-36-37-38
	~			~	~
	15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17-18-19-20 ~ 41-42-43-44-45-46
	~				~
	31				31-32-33-34-35-36 ~ 57-58-59-60-61-62

NOTE :
1) Continuous Burst mode needs to meet t_{CSM} (max. 1.7us) parameter.

11.4 $\overline{\text{WAIT}}$ Configuration [A8] & $\overline{\text{WAIT}}$ Polarity [A13]

The $\overline{\text{WAIT}}$ signal is output signal indicating the status of the data on the bus whether or not it is valid. $\overline{\text{WAIT}}$ configuration is to decide the timing when $\overline{\text{WAIT}}$ asserts or desserts. $\overline{\text{WAIT}}$ asserts (or desserts) one clock prior to the data when A8 is set to 0. ($\overline{\text{WAIT}}$ asserts (or desserts) at data clock when A8 is set to 1). $\overline{\text{WAIT}}$ polarity is to decide the $\overline{\text{WAIT}}$ signal level at which data is valid or invalid. Data is valid if $\overline{\text{WAIT}}$ signal is high when A13 is set to 0. (Data is valid if $\overline{\text{WAIT}}$ signal is low when A13 is set to 1). All the timing diagrams in this SPEC are illustrated based on following setup; [A13 : 0] and [A8 : 0]. Below timing shows $\overline{\text{WAIT}}$ signal's movement when word boundary crossing happens in No-wrap mode.

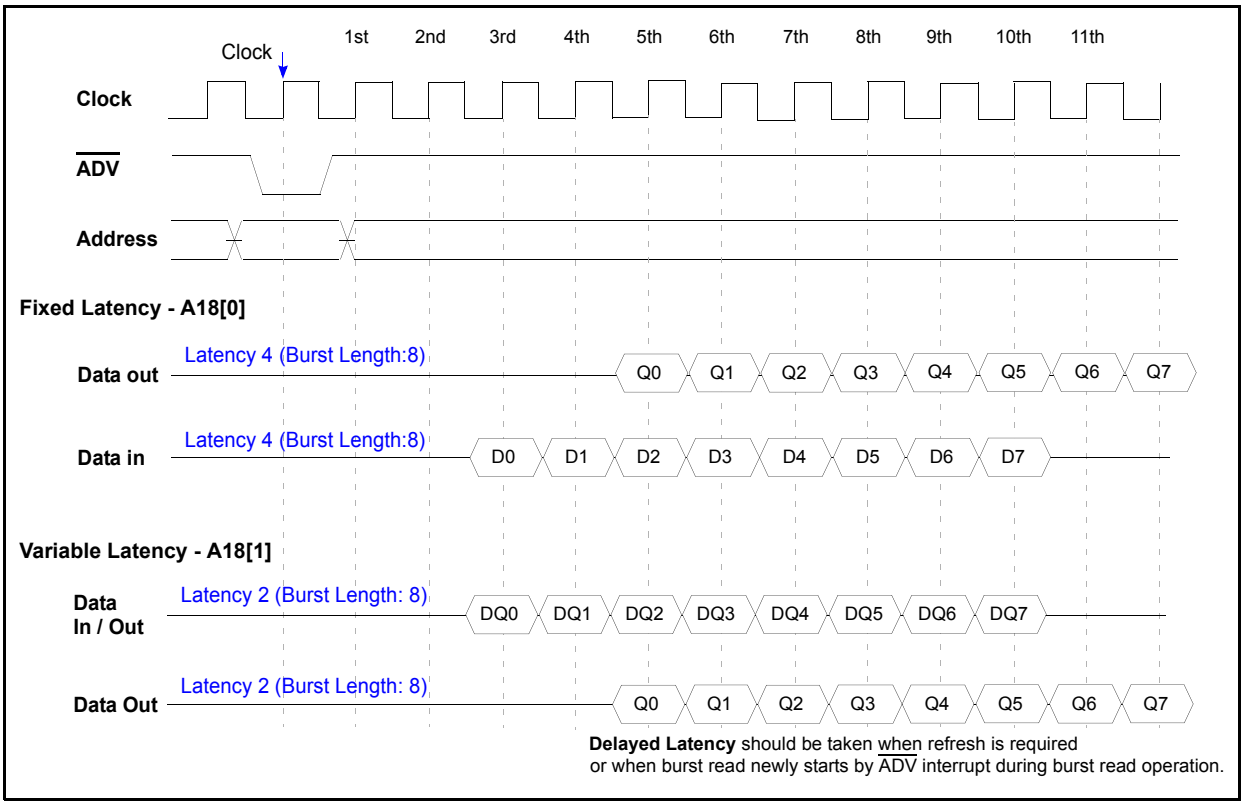


11.5 Latency [A11~A9]

The Latency stands for the number of clocks before the first data available from the burst command.

Item	Upto 66MHz		Upto 80MHz		Upto 104MHz		Upto 108MHz	
	Fixed	Variable	Fixed	Variable	Fixed	Variable	Fixed	Variable
Latency Set(A11:A10:A9)	4(0:0:1)	2(1:0:0)	5(0:1:0)	3(0:0:0)	7(1:0:1)	4(0:0:1)	7(1:0:1)	4(0:0:1)
Read Latency(min)	4	2 / 4[1)]	5	3 / 5[1)]	7	4 / 7[1)]	7	4 / 7[1)]
1st Read data fetch clock	5th	3rd / 5th[1)]	6th	4th / 6th[1)]	8th	5th / 8th[1)]	8th	5th / 8th[1)]
Write Latency(min)	2	2	3	3	4	4	4	4
1st Write data loading clock	3rd	3rd	4th	4th	5th	5th	5th	5th

NOTE:
1) **Delayed Latency** should be taken when refresh is required or when burst read newly starts by $\overline{ADV}$ interrupt during burst read operation.



11.6 Driver Strength [A17~A16]

The optimization of output driver strength is possible to adjust for the different data loadings. The device can minimize the noise generated on the data bus during read operation. The device supports full, 1/2 and 1/4 driver strength. The device's default mode is 1/2 driver strength.

Driver Strength	Full	1 / 2	1 / 4
Recommendation	CL 30 ~ 50pF	CL 15 ~ 30pF	CL 15pF or lower

12.0 OPEARTION MODE [A15~A14]

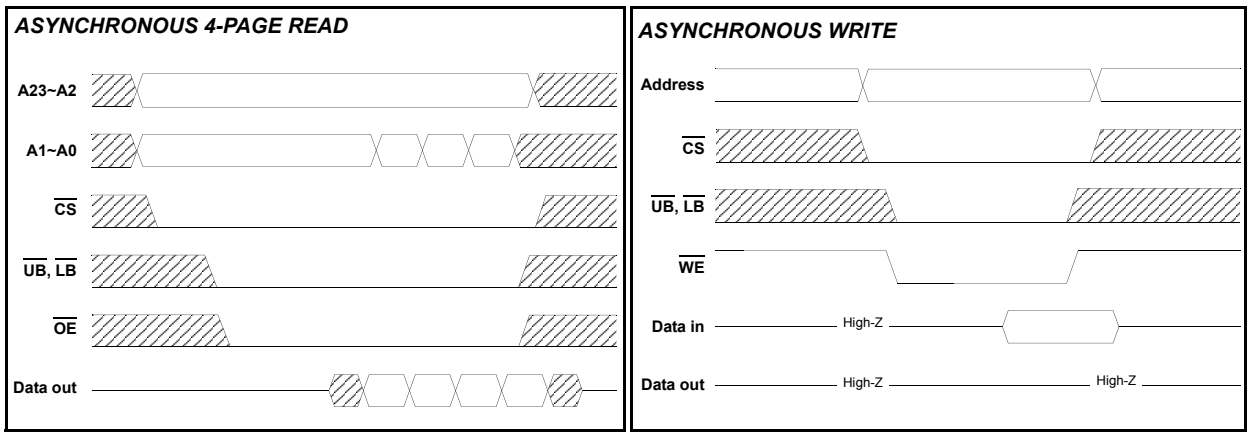
12.1 MODE1. ASYNCHRONOUS READ / ASYNCHRONOUS WRITE MODE

12.1.1. Asynchronous read operation

Asynchronous read operation starts when $\overline{CS}$, $\overline{OE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. First data come out after random access time(tAA) but second, third and fourth data come out after page access time(tPA) when using the page addresses (A0, A1). $\overline{PS}$ and $\overline{WE}$ should be de-asserted during read operation. Clock, $\overline{ADV}$ are don't care during read operation and $\overline{WAIT}$ is Hi-Z.

12.1.2. Asynchronous write operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. $\overline{PS}$ and should be de-asserted during write operation. Clock, $\overline{OE}$, $\overline{ADV}$ are don't care during write operation and $\overline{WAIT}$ signal is Hi-Z.



[Table 3] FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	Mode	Power
H	X1)	X1)	X1)	X1)	High-Z	High-Z	Deselected	Standby
H	X1)	X1)	X1)	X1)	High-Z	High-Z	Deselected	PAR
L	H	H	X1)	X1)	High-Z	High-Z	Output Disabled	Active
L	X1)	X1)	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	H	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	L	L	L	Din	Din	Word Write	Active

NOTE :
1) X means "Don't care". X should be low or high state.
2) In asynchronous mode, Clock and $\overline{ADV}$ are ignored. Clock and $\overline{ADV}$ should be low or high state.
3) /WAIT pin is High-Z in Asynchronous mode.

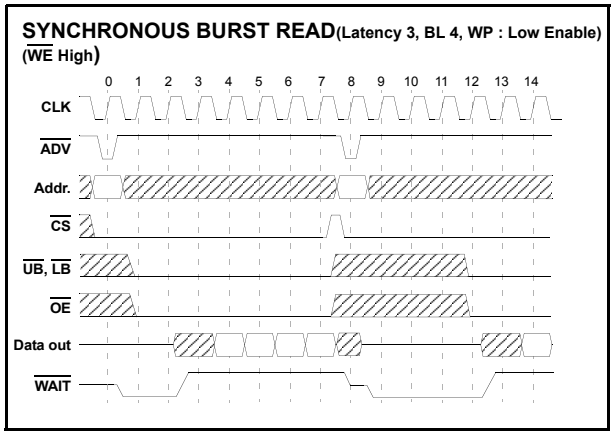
12.2 MODE3. SYNCHRONOUS BURST READ / SYNCHRONOUS BURST WRITE MODE

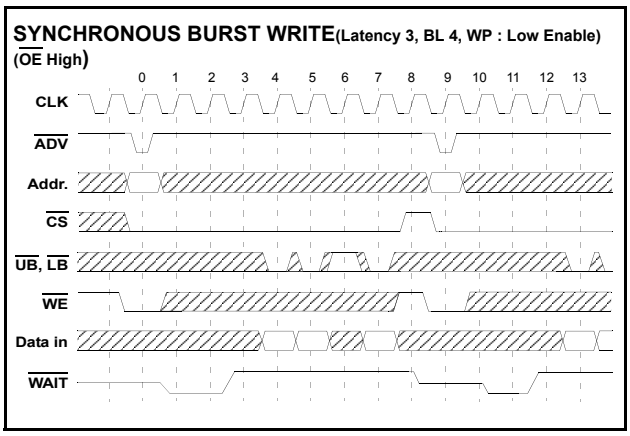
12.2.1. Synchronous Burst Read Operation

Burst Read command is implemented when $\overline{ADV}$ is detected low at clock rising edge. $\overline{WE}$ should be de-asserted during Burst read, Burst Read operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of Burst Read operation. Variable latency allows the UtRAM to be configured for minimum latency at high frequencies, but the controller must monitor $\overline{WAIT}$ to detect any conflict with refresh cycles.

12.2.2. Synchronous Burst Write Operation

Burst Write command is implemented when $\overline{ADV}$ & $\overline{WE}$ are detected low at clock rising edge. Burst Write operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of Burst Write operation.
Write operations always use fixed latency.





[Table 4] FUNCTIONAL DESCRIPTION

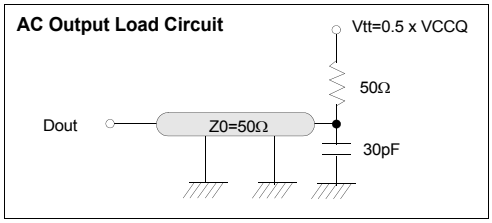
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	X1)	X1)	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	Standby
H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	PAR
L	H	H	X[1)]	X[1)]	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	X[1)]	X[1)]	H	H	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	X[1)]	H	X[1)]	X[1)]	High-Z	High-Z	⎍	⎍‾	Read Command	Active
L	L	H	L	H	Dout	High-Z	⎍	H	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	⎍	H	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	⎍	H	Word Read	Active
L	X[1)]	L	X[1)]	X[1)]	High-Z	High-Z	⎍	⎍‾	Write Command	Active
L	H	X[1)]	L	H	Din	High-Z	⎍	H	Lower Byte Write	Active
L	H	X[1)]	H	L	High-Z	Din	⎍	H	Upper Byte Write	Active
L	H	X[1)]	L	L	Din	Din	⎍	H	Word Write	Active
L	H	L	L	L	High-Z	High-Z	⎍	⎍‾	Mode Register Set	Active

NOTE :
1) X means "Don't care". X should be low or high state.
2) /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

13.0 MODE 1 AC OPERATING CONDITIONS (ASYNCH. READ / ASYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load: C_L=30pF
V_{CC}:1.7V~1.95V
T_A: -25°C~85°C



[Table 5] AC CHARACTERISTICS

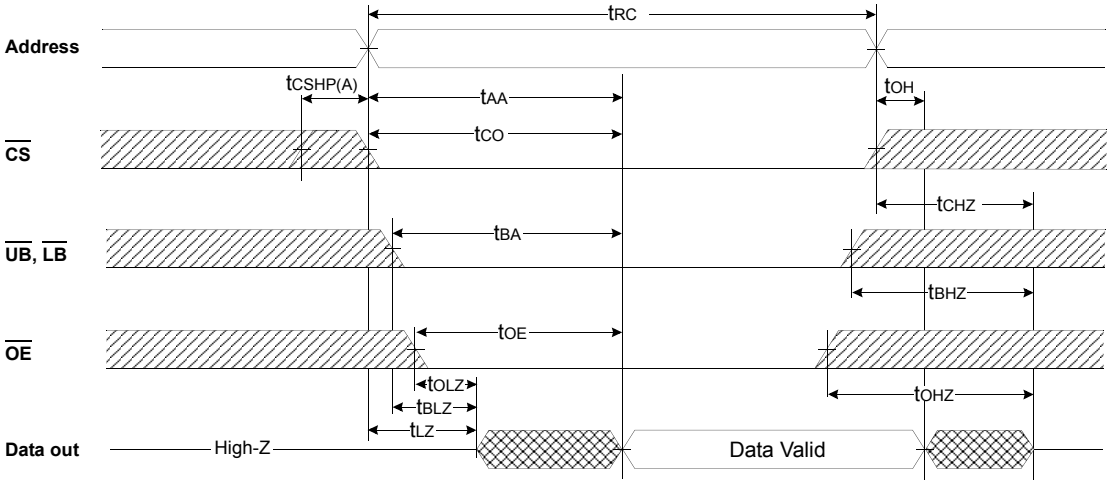
Parameter List		Symbol	Speed		Units
			Min	Max	
Common	$\overline{CS}$ High Pulse Width 1)	$t_{CSHP(A)}$	10	-	ns
Asynch. Read	Read Cycle Time	t_{RC}	70	-	ns
	Page Read Cycle Time	t_{PC}	20	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Page Access Time	t_{PA}	-	20	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	20	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	20	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	5	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{CHZ}	0	10	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	10	ns
	Output Disable to High-Z Output	t_{OHZ}	0	10	ns
	Output Hold	t_{OH}	5	-	ns
Asynch. Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time to Beginning of Write	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55	-	ns
	$\overline{WE}$ High Pulse Width	t_{WHP}	5	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Data to Write Time Overlap	t_{DW}	20	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	$\overline{UB}$, $\overline{LB}$ valid or mask setup time to beginning of write	t_{BSA}	0	-	ns
	$\overline{UB}$, $\overline{LB}$ valid or mask hold time to end of write	t_{BHA}	0	-	ns
Refresh	Maximum $\overline{CS}$ Low Pulse Width	t_{CSM}	-	1700	ns
	Address skew	t_{SKEW}	-	10	ns

NOTE :
1) A reresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition : $\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ must not remain LOW longer than t_{CSM} (1.7us)
2) The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5
3) The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.
4) A Invalid skew window is not allowed for longer than 15ns.

13.1 TIMING WAVEFORMS (ASYNCH. READ / ASYNCH. WRITE)

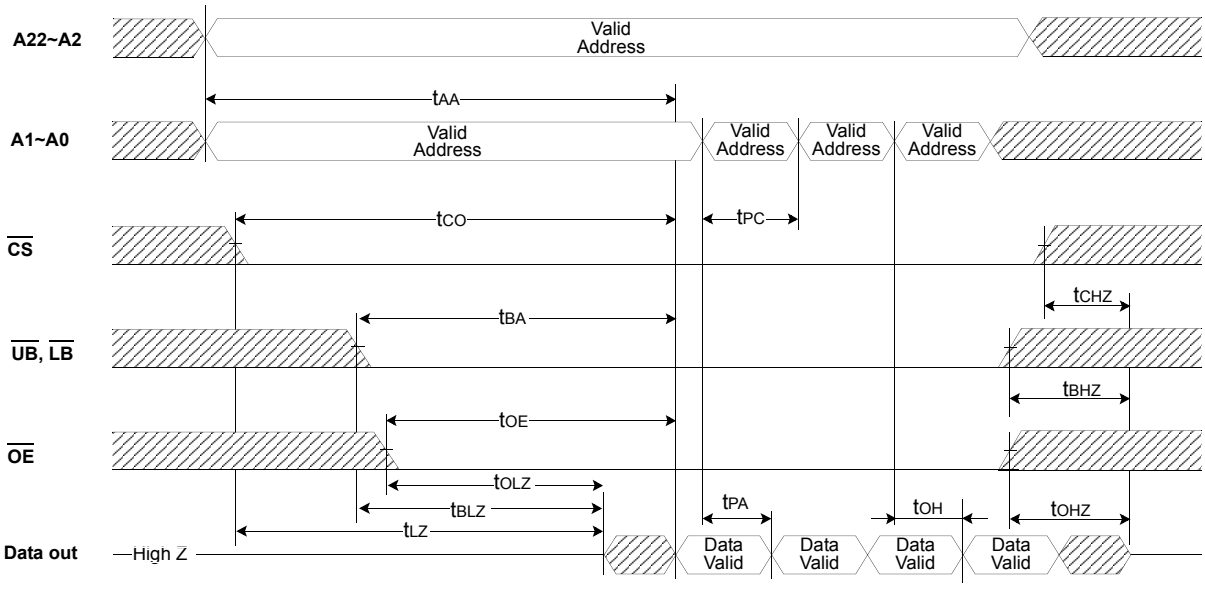
13.1.1. Asynch. READ

($\overline{WE}$=VIH, $\overline{WAIT}$=High-Z)



13.1.2. Asynch. PAGE READ

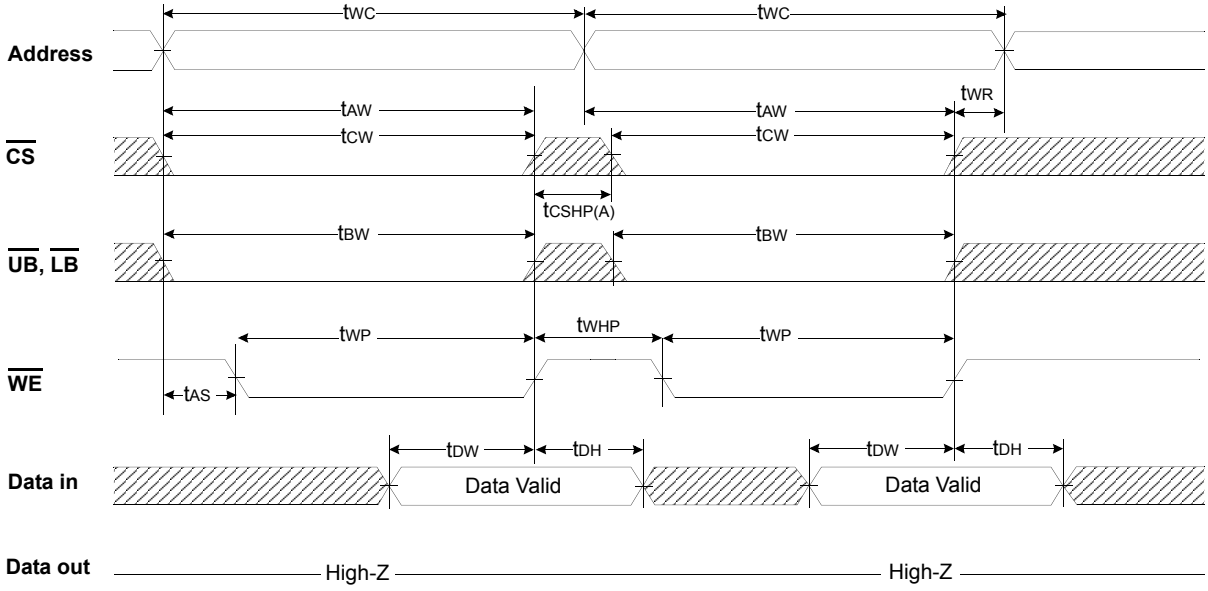
($\overline{WE}$=VIH, $\overline{WAIT}$=High-Z)



NOTE :
1) tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2) At any given temperature and voltage condition, tCHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3) In asynchronous read cycle, Clock and $\overline{ADV}$ signals are ignored.
4) If invalid address signals shorter than min. tRC are continuously repeated for over 1.7us, the device needs a normal read timing(tRC) or needs to sustain standby state for min. tRC at least once in every 1.7us.
5) A reresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
$\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ must not remain LOW longer than t_{CSM} (1.7us)
6) In asynchronous 4 page read cycle, Clock and $\overline{ADV}$ signals are ignored.

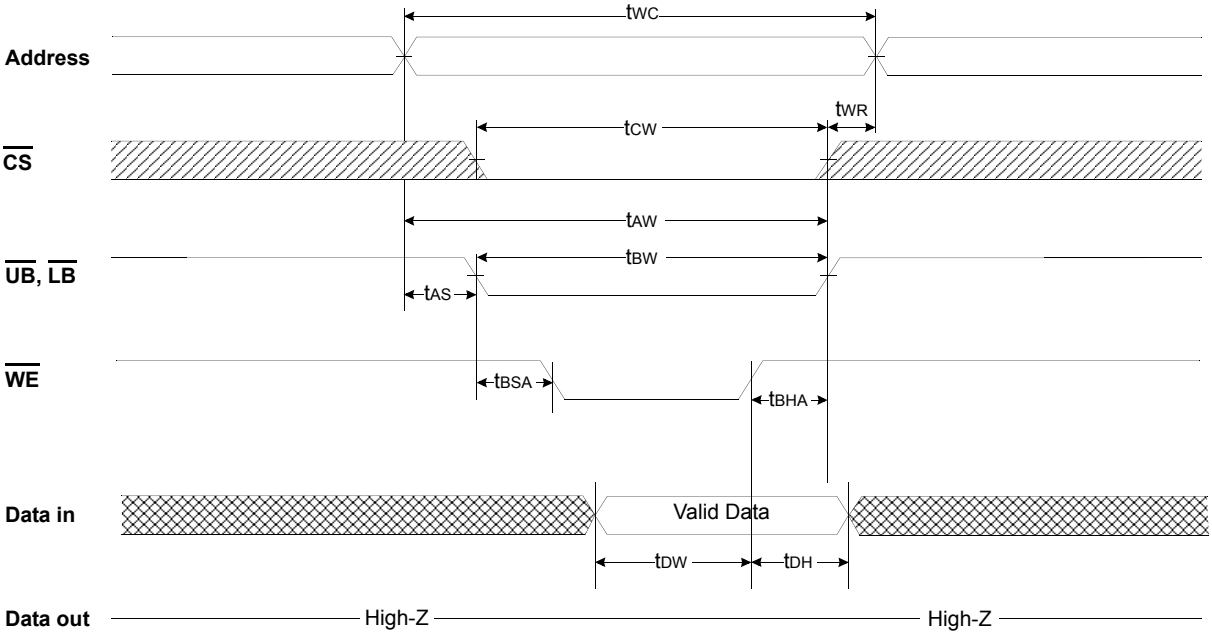
13.1.3. Asynch. WRITE (1)

($\overline{OE}$=VIH, $\overline{WAIT}$=High-Z, $\overline{WE}$ Controlled)



13.1.4. Asynch. Byte Write (2)

($\overline{OE}$=VIH, $\overline{WAIT}$=High-Z, $\overline{UB}$ & $\overline{LB}$ Controlled)

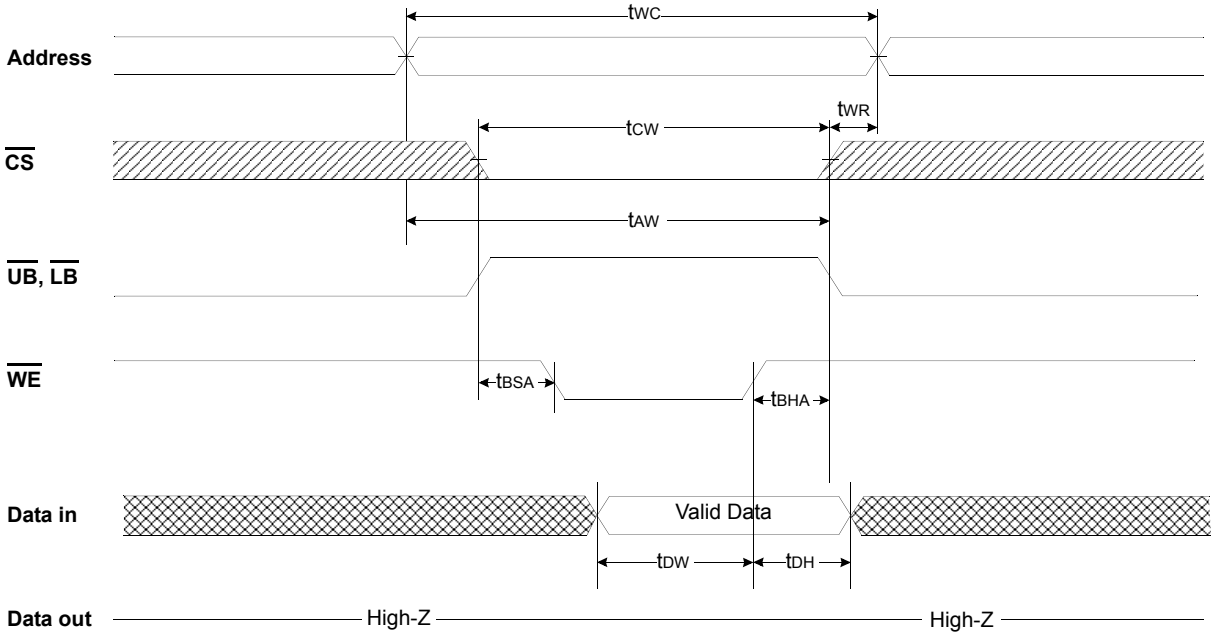


NOTE :

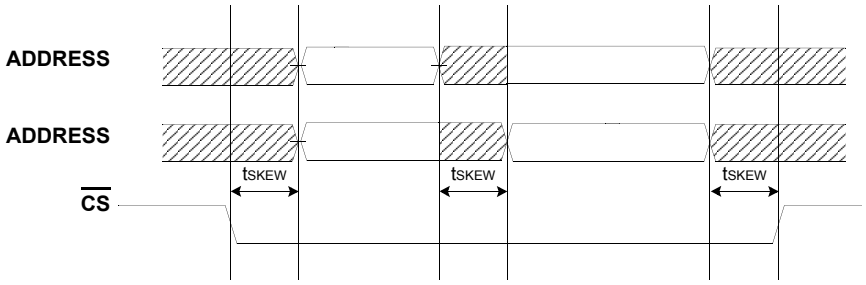
1) A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2) t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5) In asynchronous write cycle, Clock and $\overline{ADV}$ signals are ignored.
6) A reresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
$\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ must not remain LOW longer than t_{CSM} (1.7us)

13.1.5. Asynch. Write MASK (3)

(OE=VIH, WAIT=High-Z, UB & LB Controlled)

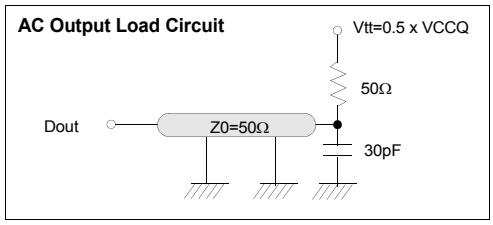


13.1.6. Address Skew for Asynchronous Operation



14.0 MODE 3 AC OPERATING CONDITIONS (SYNCH. READ / SYNCH. WRITE)

TEST CONDITIONS
(Test Load and Test Input/Output Reference)
Input pulse level: 0.2 to V_{CC}-0.2V
Input rising and falling time: 1ns
Input and output reference voltage: 0.5 x V_{CC}
Output load: C_L=30pF
V_{CC}:1.7V~1.95V
T_A: -25°C~85°C



[Table 6] AC CHARACTERISTICS

Parameter List		Symbol	66MHz		80MHz		104MHz		108MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Burst Operation (Common)	Clock Cycle Time	T	15	200	12.5	200	9.6	200	9.26	200	ns
	Maximum $\overline{CS}$ Low Pulse Width	t_{CSM}	-	1700	-	1700	-	1700	-	1700	ns
	Address Set-up Time to clock	$t_{AS(B)}$	3	-	3	-	3	-	3	-	ns
	Address Hold Time from clock	$t_{AH(B)}$	2	-	2	-	2	-	2	-	ns
	$\overline{ADV}$ Setup Time to clock	t_{ADVS}	3	-	3	-	3	-	3	-	ns
	$\overline{ADV}$ Hold Time from clock	t_{ADVH}	2	-	2	-	2	-	2	-	ns
	$\overline{CS}$ Setup Time to clock	$t_{CSS(B)}$	3	-	3	-	3	-	3	-	ns
	Burst STOP clock to New $\overline{ADV}$ Low	t_{BSADV}	0	-	0	-	0	-	0	-	ns
	$\overline{CS}$ Low Hold Time from Clock(Burst Stop)	t_{CSLH}	2	-	2	-	2	-	2	-	ns
	$\overline{CS}$ High Pulse Width[1)]	t_{CSHP}	5	-	5	-	5	-	5	-	ns
	$\overline{CS}$ Low to $\overline{WAIT}$ Low	t_{WL}	-	12	-	12	-	12	-	12	ns
	Clock to $\overline{WAIT}$ High	t_{WH}	-	11	-	9	-	7	-	7	ns
	$\overline{CS}$ High to $\overline{WAIT}$ High-Z	t_{WZ}	-	10	-	10	-	10	-	10	ns
Burst Read Operation	$\overline{UB}$, $\overline{LB}$ Low to End of Latency Clock	t_{BEL}	20	-	20	-	20	-	20	-	ns
	$\overline{OE}$ Low to End of Latency Clock	t_{OEL}	20	-	20	-	20	-	20	-	ns
	$\overline{UB}$, $\overline{LB}$ Low to Low-Z Output	t_{BLZ}	5	-	5	-	5	-	5	-	ns
	$\overline{OE}$ Low to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	5	-	ns
	Clock Rising to Data Output	t_{CD}	-	11	-	9	-	7	-	7	ns
	Output Hold from clock	$t_{OH(B)}$	2	-	2	-	2	-	2	-	ns
	ADV interrupt Clock to Output High-Z	t_{HZ}	-	10	-	10	-	10	-	10	ns
	$\overline{CS}$ High to Output High-Z	t_{CHZ}	-	10	-	10	-	10	-	10	ns
	$\overline{OE}$ High to Output High-Z	t_{OHZ}	-	10	-	10	-	10	-	10	ns
	$\overline{UB}$, $\overline{LB}$ High to Output High-Z	t_{BHZ}	-	10	-	10	-	10	-	10	ns

NOTE :
1) Refresh can not be implemented when t_{BSADV} is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 1.7us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for t_{BSADV} and $\overline{CS}$ must reimain High longer than 15ns (t_{CSHP} > 15ns).
2) The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5
3) The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

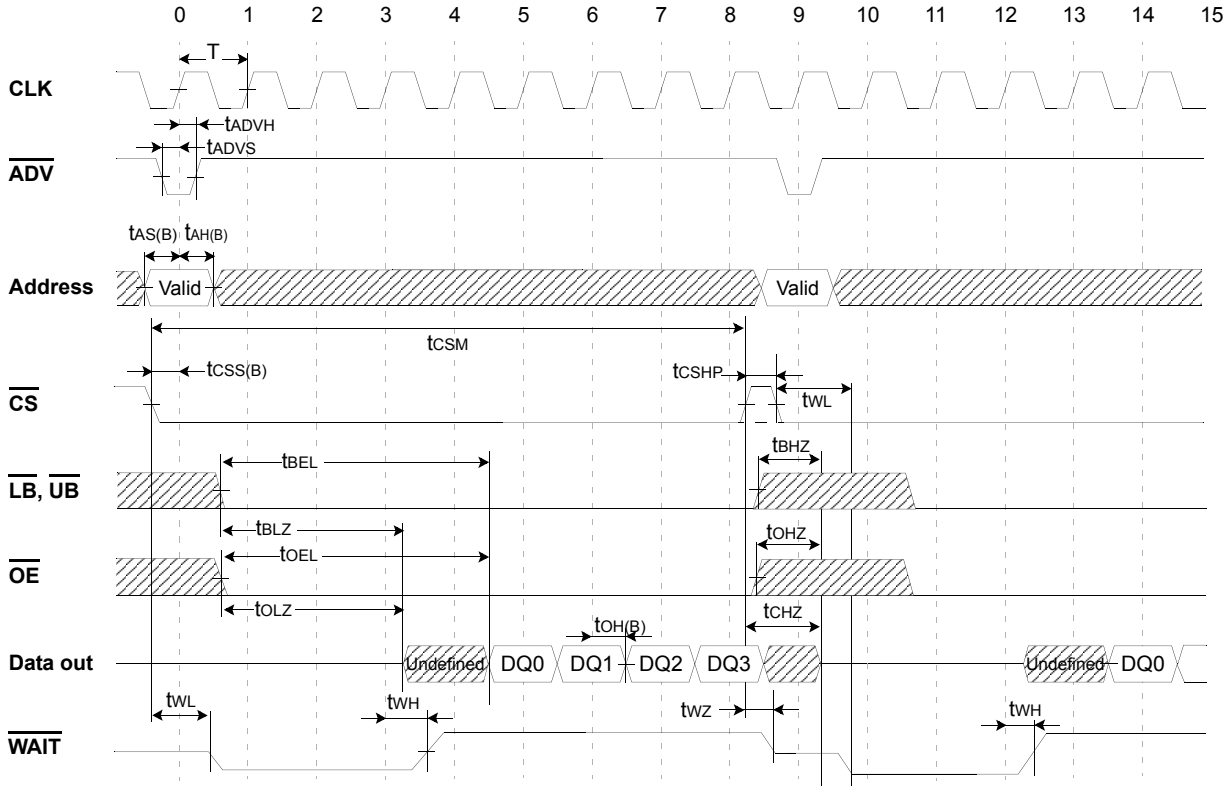
Burst Write Operation	WE Set-up Time to Clock	t_{WES}	3	-	3	-	3	-	ns
	$\overline{WE}$ Hold Time from Clock	t_{WEH}	2	-	2	-	2	-	ns
	$\overline{UB}$, $\overline{LB}$ Set-up Time to Clock	t_{BS}	3	-	3	-	3	-	ns
	Burst End clock to New $\overline{ADV}$ Low	t_{BEADV}	0	-	0	-	0	-	ns
	$\overline{UB}$, $\overline{LB}$ Hold Time from Clock	t_{BH}	2	-	2	-	2	-	ns
	Byte Masking Set-up Time to Clock	t_{BMS}	3	-	3	-	3	-	ns
	Byte Masking Hold Time from Clock	t_{BMH}	2	-	2	-	2	-	ns
	Write Data Set-up Time to Clock	t_{DS}	3	-	3	-	3	-	ns
	Write Data Hold Time from Clock	t_{DHC}	2	-	2	-	2	-	ns

NOTE :
1) Refresh can not be implemented when t_{BEADV} is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 1.7us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for t_{BEADV} and $\overline{CS}$ must reimain High longer than 15ns (t_{CSHP} > 15ns).

14.1 TIMING WAVEFORMS (SYNCH. READ / SYNCH. WRITE)

14.1.1. Burst READ - Fixed Latency

($\overline{WE}$=VIH, $\overline{WAIT}$=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



NOTE :
1) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2) Multiple clock risings are not allowed during low $\overline{ADV}$ period.
3) Burst operation should not be longer than (t_{CSM}) 1.7us and $\overline{CS}$ must remain High longer than 15ns to avoid refresh fail.

[Table 7] AC CHARACTERISTICS

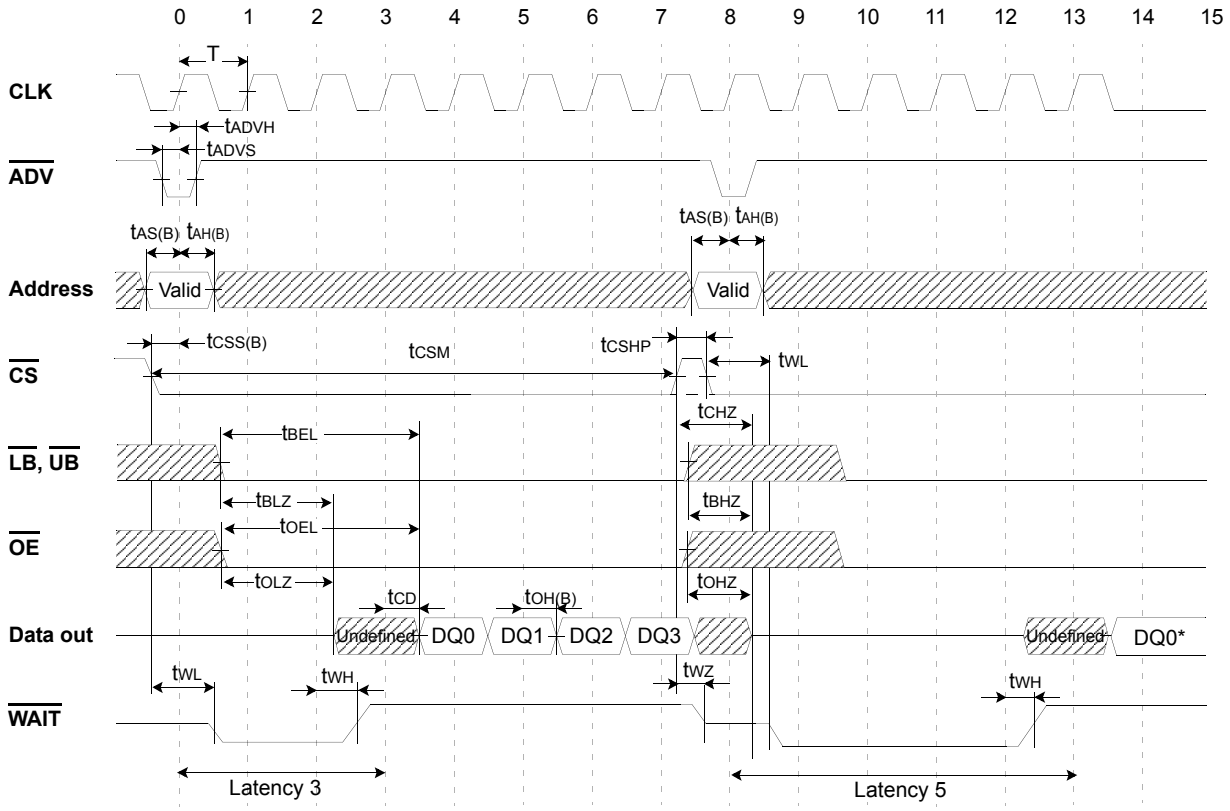
Symbol	66MHz		80MHz		104MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	9.26	200	ns
t_{CSM} 1)	-	1700	-	1700	-	1700	-	1700	ns
t_{ADVS}	3	-	3	-	3	-	3	-	ns
t_{ADVH}	2	-	2	-	2	-	2	-	ns
$t_{AS(B)}$	3	-	3	-	3	-	3	-	ns
$t_{AH(B)}$	2	-	2	-	2	-	2	-	ns
$t_{CSS(B)}$	3	-	3	-	3	-	3	-	ns
t_{CSHP} 1)	5	-	5	-	5	-	5	-	ns
t_{BEL}	20	-	20	-	20	-	20	-	ns
t_{OEL}	20	-	20	-	20	-	20	-	ns
t_{WZ}	-	10	-	10	-	10	-	10	ns

Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max	
t_{BLZ}	5	-	5	-	5	-	ns
t_{OLZ}	5	-	5	-	5	-	ns
t_{CHZ}	-	10	-	10	-	10	ns
t_{OHZ}	-	10	-	10	-	10	ns
t_{BHZ}	-	10	-	10	-	10	ns
t_{CD}	-	11	-	9	-	7	ns
$t_{OH(B)}$	2	-	2	-	2	-	ns
t_{WL}	-	12	-	12	-	12	ns
t_{WH}	-	11	-	9	-	7	ns

NOTE :
1) A refresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
$\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ Low time must not exceed t_{CSM} (1.7us).

14.1.2. Burst READ - Variable Latency

($\overline{WE}$=VIH, Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



NOTE :
1) Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3) Multiple clock risings are not allowed during low $\overline{ADV}$ period.
4) Burst operation should not be longer than (t_{CSM}) 1.7us and $\overline{CS}$ must remain High longer than 15ns to avoid refresh fail.

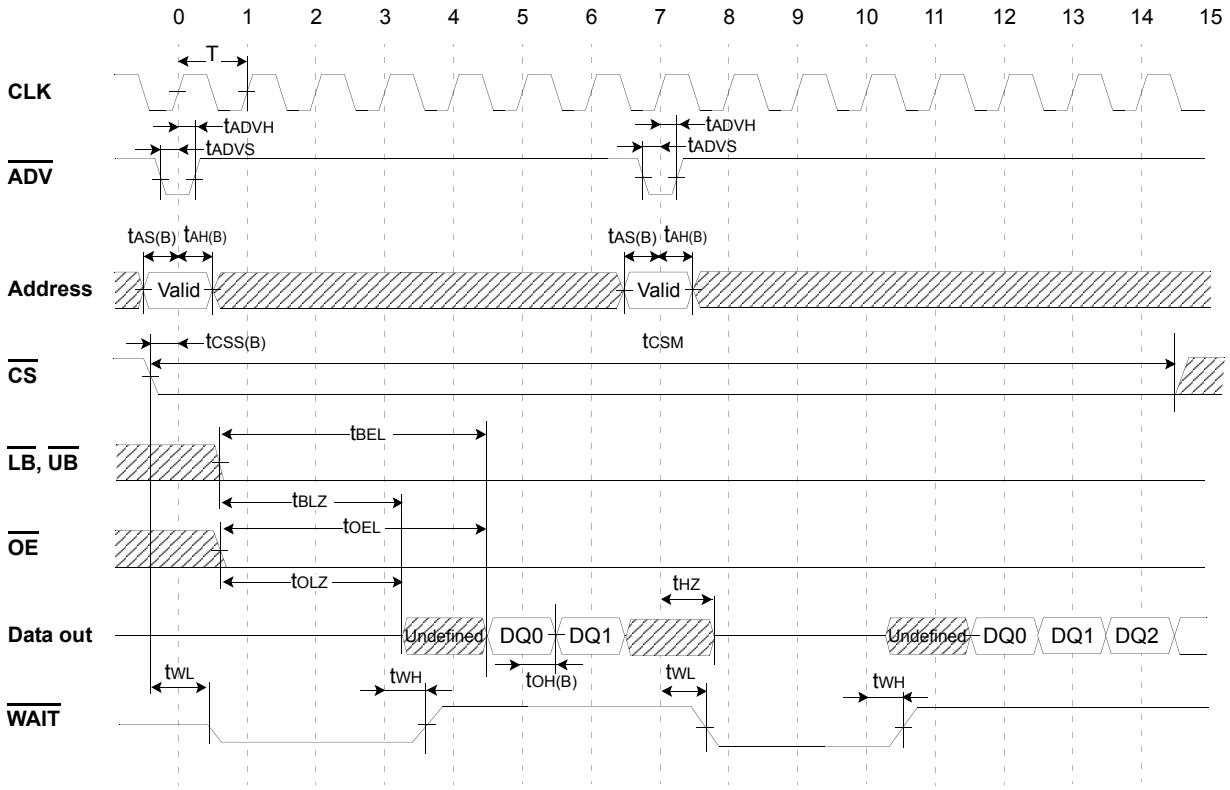
[Table 8] AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		108MHz		Units	Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	9.26	200	ns	t_{BLZ}	5	-	5	-	5	-	ns
t_{CSM} 1)	-	1700	-	1700	-	1700	-	1700	ns	t_{OLZ}	5	-	5	-	5	-	ns
t_{ADVS}	3	-	3	-	3	-	3	-	ns	t_{CHZ}	-	10	-	10	-	10	ns
t_{ADVH}	2	-	2	-	2	-	2	-	ns	t_{OHZ}	-	10	-	10	-	10	ns
$t_{AS(B)}$	3	-	3	-	3	-	3	-	ns	t_{BHZ}	-	10	-	10	-	10	ns
$t_{AH(B)}$	2	-	2	-	2	-	2	-	ns	t_{CD}	-	11	-	9	-	7	ns
$t_{CSS(B)}$	3	-	3	-	3	-	3	-	ns	$t_{OH(B)}$	2	-	2	-	2	-	ns
t_{CSHP} 1)	5	-	5	-	5	-	5	-	ns	t_{WL}	-	12	-	12	-	12	ns
t_{BEL}	20	-	20	-	20	-	20	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{OEL}	20	-	20	-	20	-	20	-	ns								
t_{WZ}	-	10	-	10	-	10	-	10	ns								

NOTE :
1) A refresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
$\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ Low time must not exceed t_{CSM} (1.7us).

14.1.3. Burst READ ($\overline{ADV}$ Interrupt) - Fixed Latency

($\overline{WE}$=VIH, $\overline{WAIT}$=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



NOTE :
1) Refresh is blocked during $\overline{ADV}$ Interrupt Read and continuous Burst Read by ADV interrupt should not be longer than t_{CSM} (1.7us)
2) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3) Multiple clock risings are not allowed during low $\overline{ADV}$ period.
4) Burst interrupt is allowable after the first data received by controller.

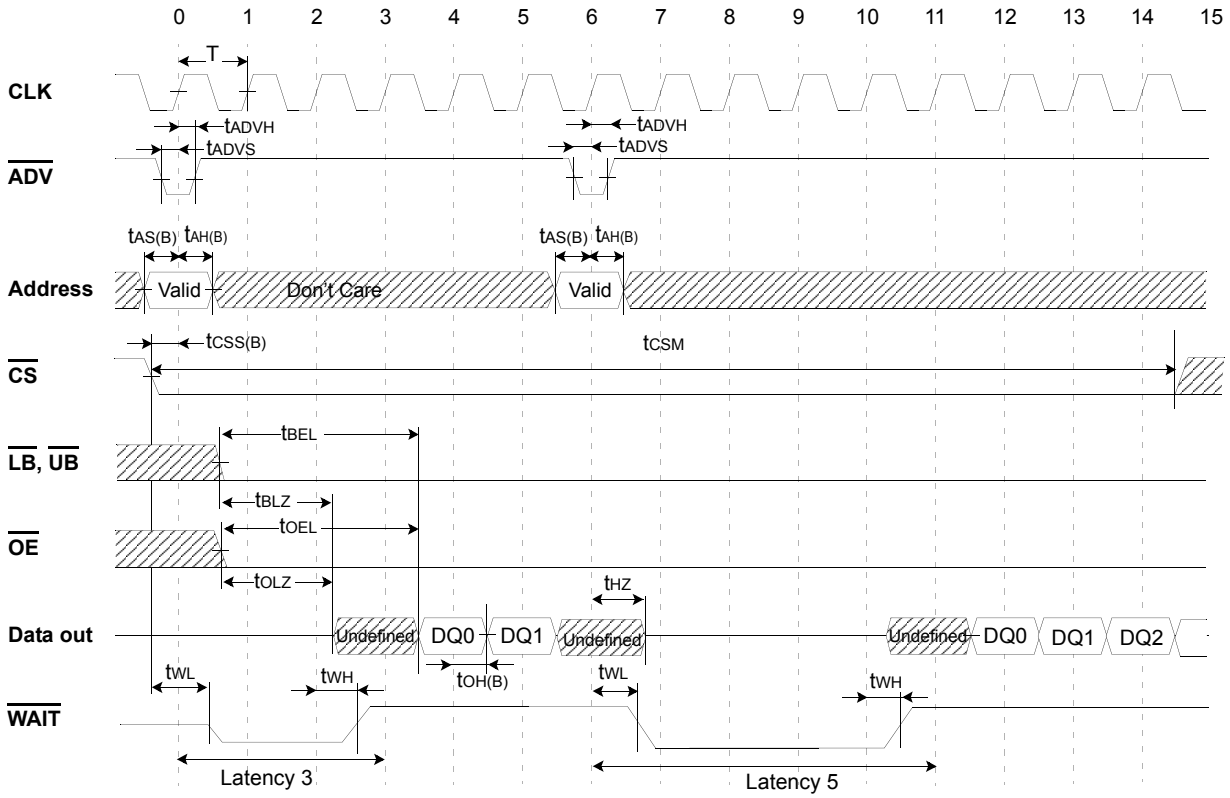
[Table 9] AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		108MHz		Units	Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	9.26	200	ns	t_{BLZ}	5	-	5	-	5	-	ns
t_{CSM} 1)	-	1700	-	1700	-	1700	-	1700	ns	t_{OLZ}	5	-	5	-	5	-	ns
t_{ADVS}	3	-	3	-	3	-	3	-	ns	t_{HZ}	-	10	-	10	-	10	ns
t_{ADVH}	2	-	2	-	2	-	2	-	ns	t_{CHZ}	-	10	-	10	-	10	ns
$t_{AS(B)}$	3	-	3	-	3	-	3	-	ns	t_{OHZ}	-	10	-	10	-	10	ns
$t_{AH(B)}$	2	-	2	-	2	-	2	-	ns	t_{BHZ}	-	10	-	10	-	10	ns
$t_{CSS(B)}$	3	-	3	-	3	-	3	-	ns	t_{CD}	-	11	-	9	-	7	ns
t_{CSHP} 1)	5	-	5	-	5	-	5	-	ns	$t_{OH(B)}$	2	-	2	-	2	-	ns
t_{BEL}	20	-	20	-	20	-	20	-	ns	t_{WL}	-	12	-	12	-	12	ns
t_{OEL}	20	-	20	-	20	-	20	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{WZ}	-	10	-	10	-	10	-	10	ns								

NOTE :
1) A refresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
$\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ Low time must not exceed t_{CSM} (1.7us).

14.1.4. Burst READ ($\overline{ADV}$ Interrupt) - Variable Latency

($\overline{WE}$=VIH, $\overline{WAIT}$=High-Z, Latency=3,Burst Length=4,WP=Low enable, WC=one clock prior to the data)



NOTE :
1) Delayed latency is taken for Burst READ by $\overline{ADV}$ interrupt. Refer to Latency Table.
2) Refresh is blocked during $\overline{ADV}$ Interrupt Read and continuous Burst Read by ADV interrupt should not be longer than t_{CSM} (1.7us)
3) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
4) Multiple clock risings are not allowed during low $\overline{ADV}$ period.
5) Burst interrupt is allowable after the first data received by controller.

[Table 10] AC CHARACTERISTICS

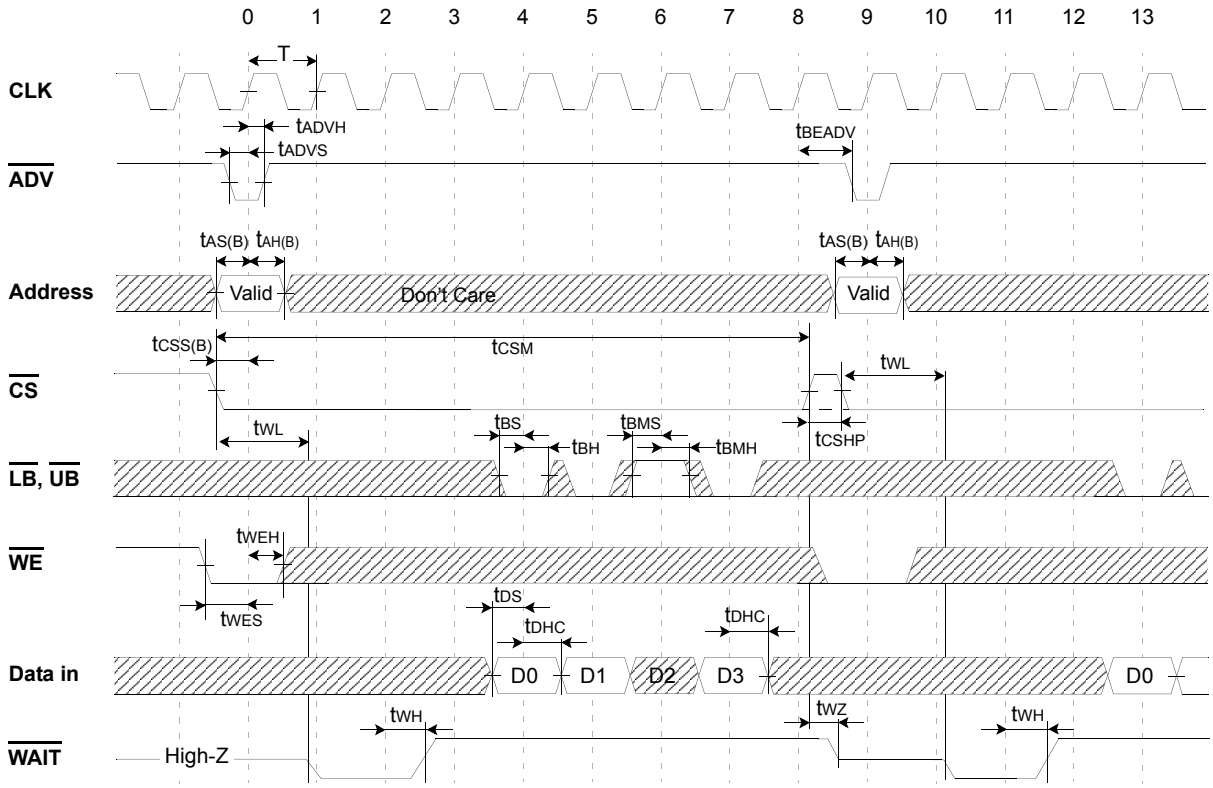
Symbol	66MHz		80MHz		104MHz		108MHz		Units	Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	9.26	200	ns	t_{BLZ}	5	-	5	-	5	-	ns
t_{CSM} 1)	-	1700	-	1700	-	1700	-	1700	ns	t_{OLZ}	5	-	5	-	5	-	ns
t_{ADVS}	3	-	3	-	3	-	3	-	ns	t_{HZ}	-	10	-	10	-	10	ns
t_{ADVH}	2	-	2	-	2	-	2	-	ns	t_{CHZ}	-	10	-	10	-	10	ns
$t_{AS(B)}$	3	-	3	-	3	-	3	-	ns	t_{OHZ}	-	10	-	10	-	10	ns
$t_{AH(B)}$	2	-	2	-	2	-	2	-	ns	t_{BHZ}	-	10	-	10	-	10	ns
$t_{CSS(B)}$	3	-	3	-	3	-	3	-	ns	t_{CD}	-	11	-	9	-	7	ns
t_{CSHP} 1)	5	-	5	-	5	-	5	-	ns	$t_{OH(B)}$	2	-	2	-	2	-	ns
t_{BEL}	20	-	20	-	20	-	20	-	ns	t_{WL}	-	12	-	12	-	12	ns
t_{OEL}	20	-	20	-	20	-	20	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{WZ}	-	10	-	10	-	10	-	10	ns								

NOTE :
1) A refresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
$\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ Low time must not exceed t_{CSM} (1.7us).

14.1.5. Burst WRITE

(OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

Burst WRITE



NOTE :
1) Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 1.7us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV and CS must remain High longer than 15ns(tCSHP > 15ns)
2) /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3) Multiple clock risings are not allowed during low ADV period.
4) Burst operation should not be longer than t_{CSM} (1.7μs) and CS must remain High longer than 15ns to avoid refresh fail.

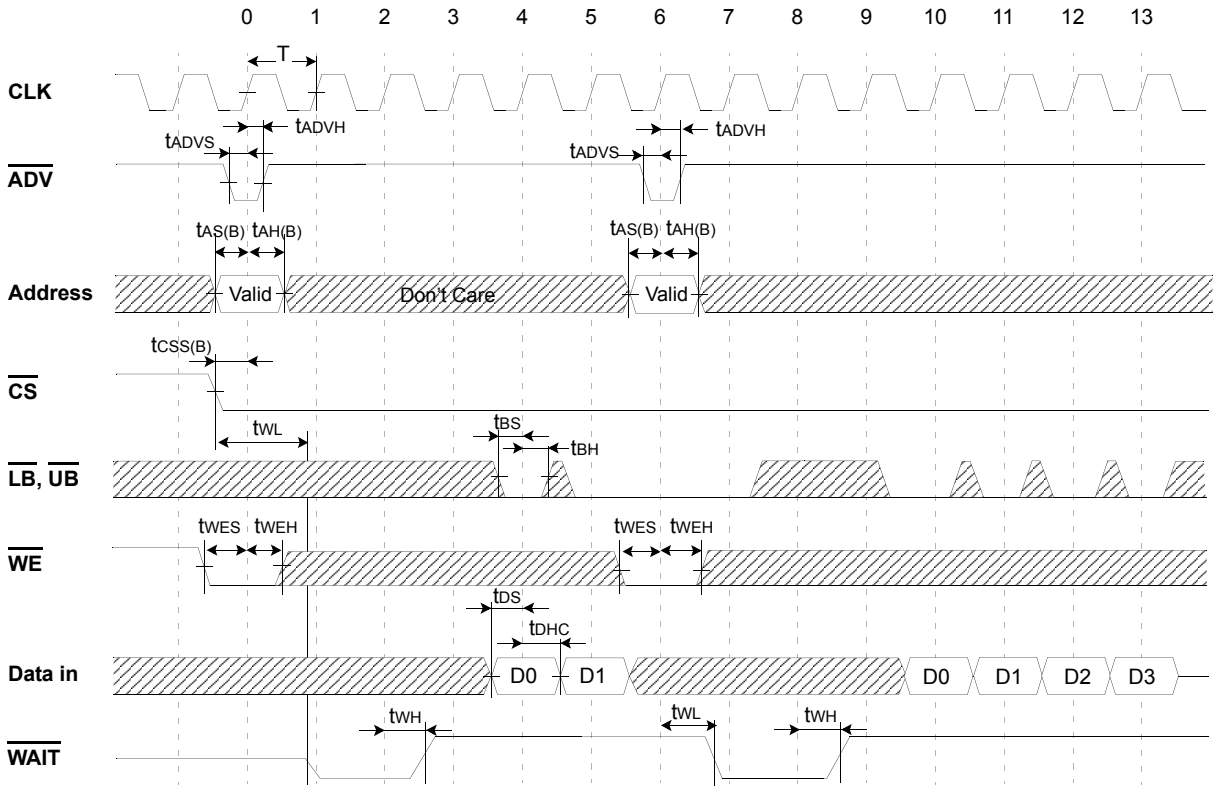
[Table 11] AC CHARACTERISTICS

Symbol	66MHz		80MHz		108MHz		Units	Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
t_{CSHP} [1)]	5	-	5	-	5	-	ns	t_{DS}	3	-	3	-	3	-	ns
t_{BS}	3	-	3	-	3	-	ns	t_{DHC}	2	-	2	-	2	-	ns
t_{BH}	2	-	2	-	2	-	ns	t_{WL}	-	12	-	12	-	12	ns
t_{BMS}	3	-	3	-	3	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{BMH}	2	-	2	-	2	-	ns	t_{WZ}	-	10	-	10	-	10	ns
t_{WES}	3	-	3	-	3	-	ns								
t_{WEH}	2	-	2	-	2	-	ns								

NOTE :
1) A refresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition :
CS high for longer than 15ns (t_{CSHP} > 15ns). CS Low time must not exceed t_{CSM} (1.7us).

14.1.6. Burst WRITE ($\overline{ADV}$ PULSE Interrupt)

($\overline{OE}$=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



NOTE :
1) Multiple clock risings are not allowed during low $\overline{ADV}$ period.
2) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
3) Burst interrupt is allowable after the first data word written.

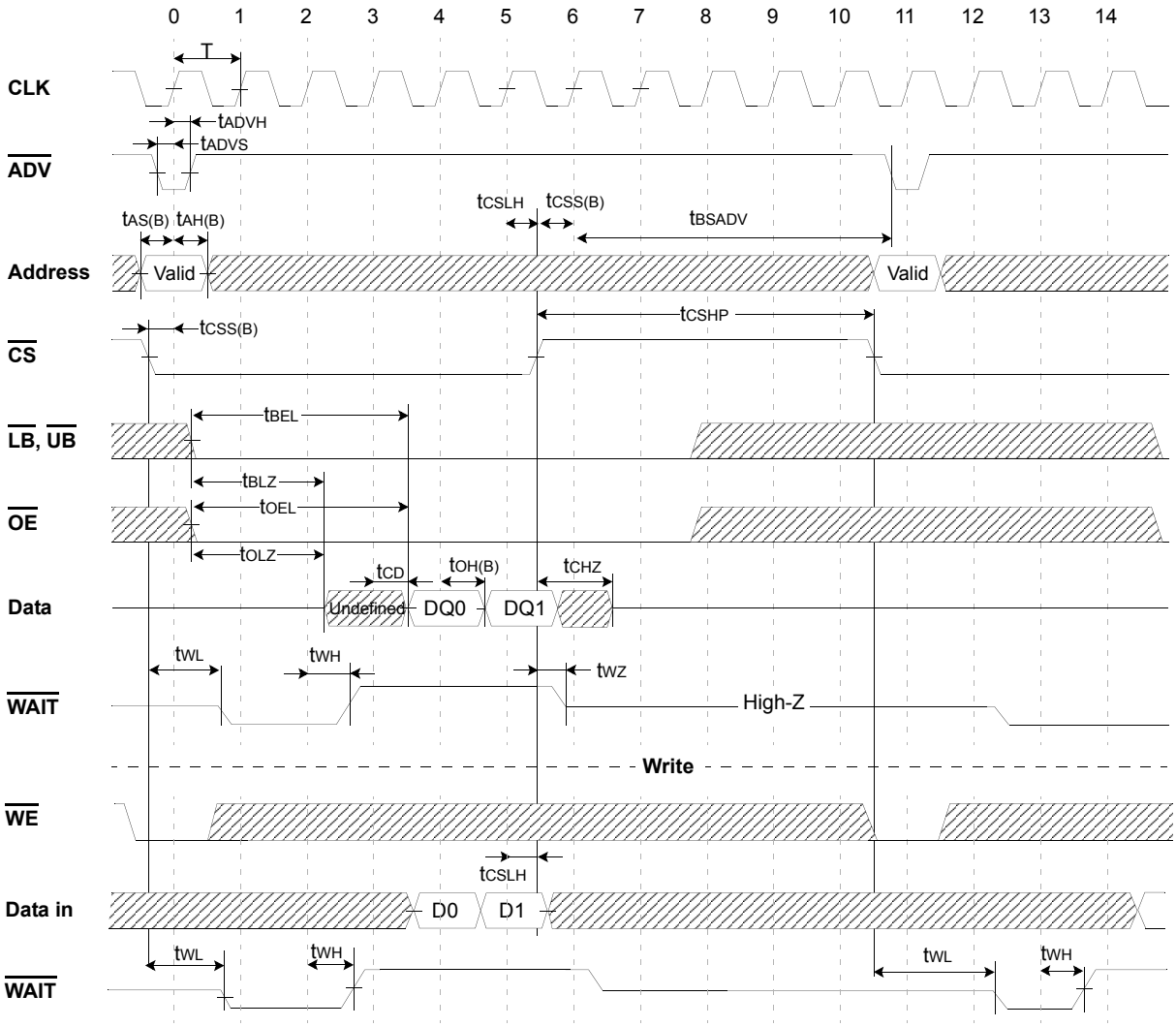
[Table 12] AC CHARACTERISTICS

Symbol	66MHz		80MHz		108MHz		Units	Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
t_{CSHP} 1)	5	-	5	-	5	-	ns	t_{DS}	3	-	3	-	3	-	ns
t_{BS}	3	-	3	-	3	-	ns	t_{DHC}	2	-	2	-	2	-	ns
t_{BH}	2	-	2	-	2	-	ns	t_{WL}	-	12	-	12	-	12	ns
t_{BMS}	3	-	3	-	3	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{BMH}	2	-	2	-	2	-	ns	t_{WZ}	-	10	-	10	-	10	ns
t_{WES}	3	-	3	-	3	-	ns								
t_{WEH}	2	-	2	-	2	-	ns								

NOTE :
1) A refresh opportunity must be provided every t_{CSM}. A refresh opportunity is satisfied by the condition : $\overline{CS}$ high for longer than 15ns (t_{CSHP} > 15ns). $\overline{CS}$ Low time must not exceed t_{CSM} (1.7us).

14.1.7. Burst READ STOP & Burst WRITE STOP

(Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



NOTE :

1) Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 1.7us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV and $\overline{CS}$ must remain High longer than 15ns (t_{CSHP} > 15ns)

2) Multiple clock risings are not allowed during low $\overline{ADV}$ period.

3) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)

[Table 13] AC CHARACTERISTICS

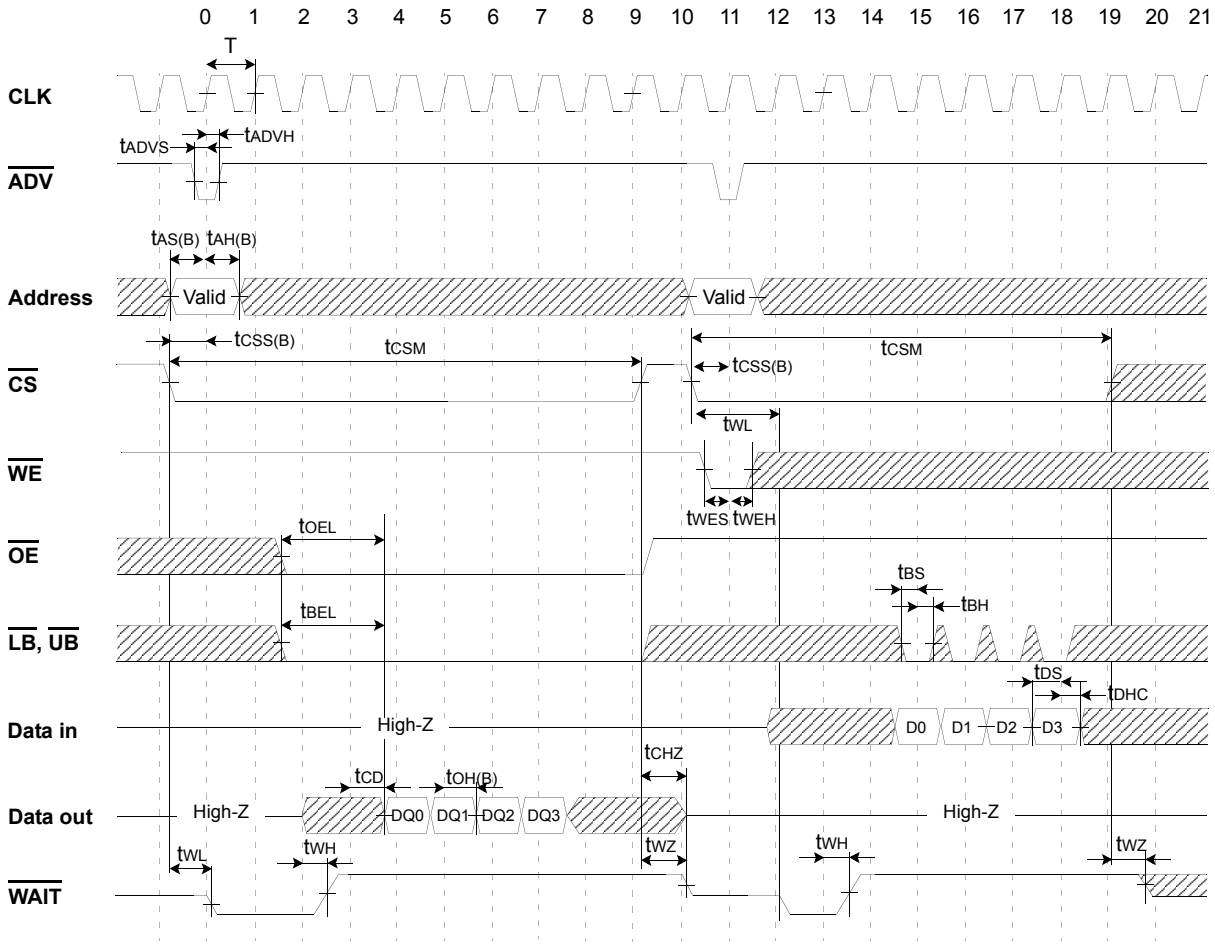
Symbol	66MHz		80MHz		108MHz		Units	Symbol	66MHz		80MHz		108MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
t_{CSHP} [1)]	5	-	5	-	5	-	ns	t_{DS}	3	-	3	-	3	-	ns
t_{BS}	3	-	3	-	3	-	ns	t_{DHC}	2	-	2	-	2	-	ns
t_{BH}	2	-	2	-	2	-	ns	t_{WL}	-	12	-	12	-	12	ns
t_{BMS}	3	-	3	-	3	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{BMH}	2	-	2	-	2	-	ns	t_{WZ}	-	10	-	10	-	10	ns
t_{WES}	3	-	3	-	3	-	ns	t_{BSADV}	-	0	-	0	-	0	ns
t_{WEH}	2	-	2	-	2	-	ns	$t_{OH(B)}$	2	-	2	-	2	-	ns

NOTE :

1) To avoid refresh fail, t_{CSHP} > 15ns :
$\overline{CS}$ must remain High longer than 15ns for refresh, the $\overline{CS}$ LOW time must not exceed t_{CSM} 1.7us.

14.1.8. Burst READ followed by Burst WRITE

(Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

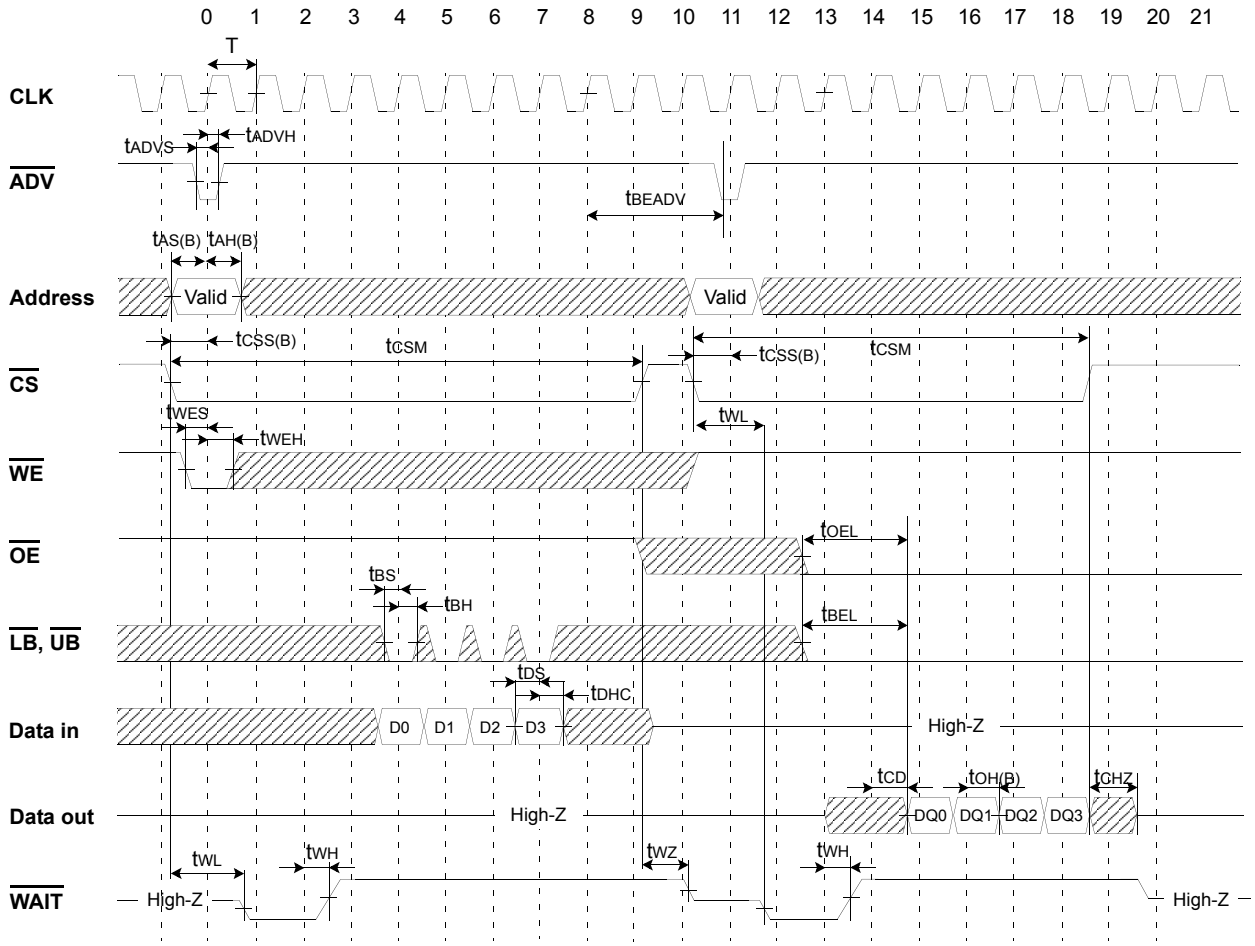


NOTE :

1) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2) Multiple clock risings are not allowed during low $\overline{ADV}$ period.
3) Burst operation should not be longer than t_{CSM} (1.7μs) and $\overline{CS}$ must remain High longer than 15ns to avoid refresh fail.

14.1.9. Burst WRITE followed by Burst READ

(Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



NOTE :

1) Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 1.7us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV and $\overline{CS}$ must remain High longer than 15ns (t_{CSHP} > 15ns)

2) /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)

3) Multiple clock risings are not allowed during low $\overline{ADV}$ period.

4) Burst operation should not be longer than t_{CSM} (1.7μs) and $\overline{CS}$ must remain High longer than 15ns to avoid refresh fail.