

## **64Mb (4M x 16 bit) U $t$ RAM2**

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**Document Title**

**4Mx16 bit Synchronous Burst Uni-Transistor Random Access Memory 2**

**Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	Initial - Design Target	Dec. 07, 2006	Preliminary
1.0	Finalized - Updated DC values	Dec. 12, 2007	Final
2.0	Revised - Corrected errata (package dimension)	Jan. 11, 2007	Final
3.0	Revised - Changed lcc2 cycle time from 70ns to "min tRC / min tWC" - Changed lcc2p cycle time to "min tRC+3 min tPC " - Inserted the sentence, (p.18) "A refresh opportunity must be provided every tCSM. A refresh opportunity is satisfied by the condition that $\overline{CS}$ HIGH for longer than 15ns. $\overline{CS}$ must not remain LOW longer than tCSM."	Sep. 18, 2007	Final

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**K1C6416B2D****UtRAM2****GENERAL DESCRIPTION**

SAMSUNG's UtRAM products are designed to meet the request from the customers who want to cope with the fast growing mobile applications that need high-speed random access memory. UtRAM is the solution for the mobile market with its low cost, high density and high performance feature. K1C6416B2D is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous operation (asynchronous page read and asynchronous write), the NOR flash like synchronous operation (synchronous burst read and asynchronous write) and the fully synchronous operation (synchronous burst read and synchronous burst write). These operation modes are defined through the Configuration Register Setting. It supports the special features for the standby power saving. Those are the PAR(Partial Array Refresh) mode, DPD(Deep Power Down) mode and internal TCSR(Temperature Compensated Self Refresh). It also supports variable and fixed latency, driver strength settings, Burst sequence (wrap or No-wrap) options and a device ID register (DIDR).

**FEATURES**

- Process technology: CMOS
- Organization: 4M x 16 bit
- Power supply voltage: 1.7V~1.95V
- Three state outputs
- Supports Configuration Register Set
  - CRE pin set up
  - Software set up
- Supports power saving modes
  - PAR (Partial Array Refresh)
  - DPD (Deep Power Down)
  - Internal TCSR (Temperature Compensated Self Refresh)
- Supports driver strength optimization
- Support 2 operation modes
  - Asynchronous mode (4-Page)
  - Synchronous mode
- Random access time:70ns
- Page access time:20ns
- Synchronous burst operation
  - Max. clock frequency : 104MHz
  - Fixed and Variable read latency
  - 4 / 8 / 16 / 32 and Continuous burst
  - Wrap / No-wrap
  - Latency : 3(Variable) @ 104MHz  
3(Variable) @ 80MHz  
2(Variable) @ 66MHz
- Burst stop
- Burst read suspend
- Burst write data masking

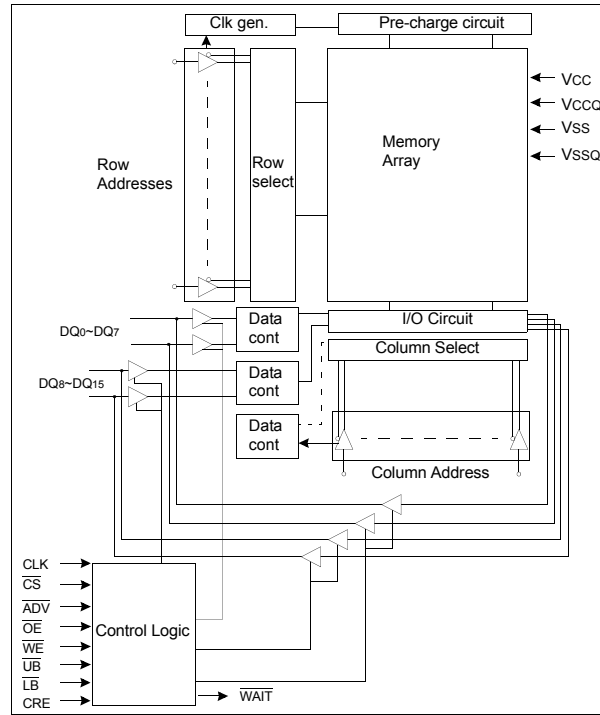
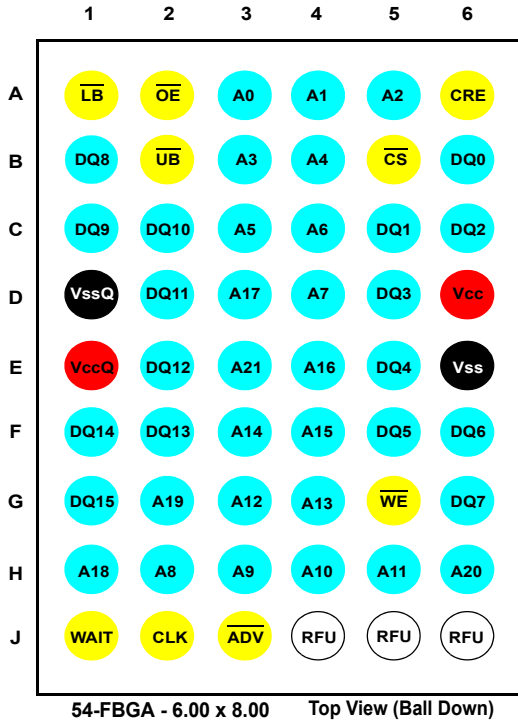
**PRODUCT FAMILY**

Product Family	Operating Mode	Operating Temp.	Vcc / Vccq	CLK Freq. (Max.)	Current Consumption	
					Standby (I <sub>SB1</sub> , Max.)	Operating (I <sub>CC2P</sub> , Max.)
K1C6416B2D-I	Asynch. Mode Synch. Mode	Industrial(-40~85°C)	1.7~1.95V	104MHz	180uA < 85°C 120uA < 40°C	40mA

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## PIN DESCRIPTIONS & FUNCTION BLOCK DIAGRAM



## BALL DESCRIPTIONS

Symbol	Type	Description
A[21:0]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
CLK (note1)	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV is active. CLK is static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
ADV (note1)	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV during asynchronous READ and WRITE operations. ADV can be held LOW during asynchronous READ and WRITE operations.
CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
CS	Input	Chip Select: Activates the device when LOW. When CS is HIGH, the device is disabled and goes into standby or deep power-down mode.
OE	Input	Output enable: Enables the output buffers when LOW. When OE is HIGH, the output buffers are disabled.
WE	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
LB	Input	Lower byte enable. DQ[7:0]
UB	Input	Upper byte enable. DQ[15:8]
DQ[15:0]	Input/Output	Data inputs/outputs.
WAIT (note1)	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CS. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CS is HIGH.
RFU	-	Reserved for future use.
VCC	Supply	Device power supply: (1.70V–1.95V) Power supply for device core operation.
VCCQ	Supply	I/O power supply: (1.70V–1.95V) Power supply for input/output buffers.
VSS	Supply	VSS must be connected to ground.
VSSQ	Supply	VSSQ must be connected to ground.

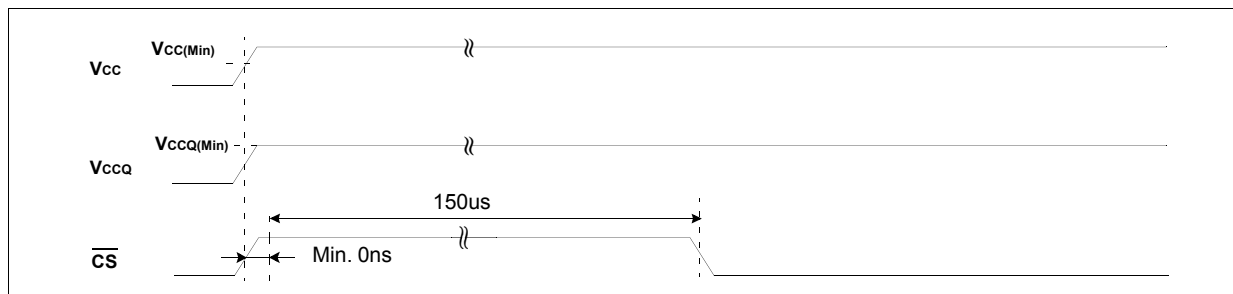
1. When using asynchronous mode exclusively, the CLK and ADV inputs can be tied to Vss. WAIT will be asserted but should be ignored during asynchronous mode operations.

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## POWER UP SEQUENCE

After  $V_{CC}$  and  $V_{CCQ}$  reach minimum operating voltage(1.7V), drive  $\overline{CS}$  High. Then the device gets into the Power Up mode. Wait for minimum 150 $\mu$ s to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the appropriate device operation, be sure to keep the following power up sequence. Asynch. mode is default mode and is set up after power up.



**K1C6416B2D**

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**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to V <sub>CCQ</sub> +0.3V	V
Power supply voltage relative to V <sub>ss</sub>	V <sub>CC</sub> , V <sub>CCQ</sub>	-0.2 to 2.5V	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V <sub>CC</sub>	1.7	1.8	1.95	V
Power supply voltage(I/O)	V <sub>CCQ</sub>	1.7	1.8	1.95	V
Ground	V <sub>SS</sub> , V <sub>SSQ</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	V <sub>CCQ</sub> -0.4	-	V <sub>CCQ</sub> +0.2 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.4	V

1. T<sub>A</sub>=-40 to 85°C, otherwise specified.
2. Overshoot: V<sub>CCQ</sub>+1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

**CAPACITANCE**

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

1. Freq.=1MHz, T<sub>A</sub>=25°C
2. Capacitance is sampled, not 100% tested.

**DC AND OPERATING CHARACTERISTICS**

Item	Symbol	Test Conditions	Min	Typ	Max	Unit		
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CCQ</sub>	-1	-	1	μA		
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ , CRE=V <sub>IL</sub> , $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CCQ</sub>	-1	-	1	μA		
Average Operating Current (Async)	I <sub>CC2</sub> <sup>6)</sup>	Cycle time=min t <sub>RC</sub> /min t <sub>WC</sub> , I <sub>IO</sub> =0mA <sup>4)</sup> , 100% duty, $\overline{CS}=V_{IL}$ , CRE=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	40	mA		
	I <sub>CC2P</sub>	Cycle time=min t <sub>RC</sub> +3 min t <sub>PC</sub> , I <sub>IO</sub> =0mA <sup>4)</sup> , 100% duty, $\overline{CS}=V_{IL}$ , CRE=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	40	mA		
Average Operating Current (Burst)	I <sub>CC3</sub>	Burst Length 4, Latency 5, 80MHz, I <sub>IO</sub> =0mA <sup>4)</sup> , Address transition 1 time, $\overline{CS}=V_{IL}$ , CRE=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	40	mA		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =0.2mA	-	-	0.2	V		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.2mA	1.4	-	-	V		
Standby Current(CMOS)	I <sub>SB1</sub> <sup>1)</sup>	$\overline{CS}=V_{CCQ}$ , CRE=0V, Other inputs=0V or V <sub>CCQ</sub> (Toggle is not allowed) <sup>5)</sup>	< 40°C	-	-	120	μA	
			< 85°C	-	-	180	μA	
Partial Refresh Current	I <sub>SBP</sub> <sup>2)</sup>	$\overline{CS}=V_{CCQ}$ , CRE=0V, Other inputs=0V or V <sub>CCQ</sub> (Toggle is not allowed) <sup>5)</sup>	< 40°C	1/2 Block	-	-	115	μA
				1/4 Block	-	-	110	
				1/8 Block	-	-	105	
			< 85°C	1/2 Block	-	-	165	μA
				1/4 Block	-	-	155	
				1/8 Block	-	-	145	
Deep Power Down Current	I <sub>SD</sub>	CRE=0V, $\overline{CS}=V_{CCQ}$ , Other inputs=0V or V <sub>CCQ</sub> (Toggle is not allowed) <sup>5)</sup>	-	-	30	μA		

1. I<sub>SB1</sub> is measured after 60ms after CS high. CLK should be fixed at high or at Low.
2. Full Array Partial Refresh Current(I<sub>SBP</sub>) is same as Standby Current(I<sub>SB1</sub>).
3. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize refresh cycle below 40°C.
4. I<sub>IO</sub>=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.
5. V<sub>IN</sub>=0V; all inputs should not be toggle.
6. Clock should not be inserted between ADV low and  $\overline{WE}$  low during Write operation.



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**CRE (CONTROL REGISTER ENABLE)**

The control registers store the values for the various modes to make UtRAM suitable for a various applications. The configuration register values are written via Address pins. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV, CS, or WE, whichever occurs first; LB and UB are "Don't Care." For reads, address inputs other than A[19:18] are "Don't Care," and register bits 15:0 are output as data (ADV HIGH) on A[15:0]. Immediately after performing a configuration register READ or WRITE operation, reading the memory array is highly recommended.

**Bus Configuration Register**

The BCR defines how the device interacts with the system memory bus. The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with A = 0001h on the third cycle.

A19~A18	A15	A14	A13~A11	A10	A8	A5~A4	A3	A2~A0
RS	OM	IL	LC	WP	WC	DS	BW	BL

Register Select			Operating Mode		Initial Latency		Latency Count			
A19	A18	RS	A15	OM	A14	IL	A13	A12	A11	LC
0	0	RCR	0	Synch.	0	Variable (default)	0	0	0	0
1	0	BCR	1	Asynch (default)	1	Fixed	0	0	1	1
0	1	DIDR					0	1	0	2
							0	1	1	3 (default)
							1	0	0	4
							1	0	1	5
							1	1	0	6
							1	1	1	7

Wait Polarity		Wait Config.		Driver Strength			Burst Wrap		Burst Length				
A10	WP	A8	WC	A5	A4	DS	A3	BW	A2	A1	A0	BL	
0	Active Low	0	at data	0	0	Full Drive	0	Wrap	0	0	1	4 word	
1	Active High (default)	1	1 CLK prior (default)	0	1	1/2 Drive (default)	1	No Wrap (default)	0	1	0	8 word	
				1	0	1/4 Drive			0	1	1	16 word	
				1	1	Reserved			1	0	0	32 word	
										1	1	1	Continuous (default)

- A6, A7, A9, A16, A17, A20, A21 are reserved and should be '1'
- The registers are set automatically to default value.
- Refresh command will be denied during continuous operation. CS low should not be longer than tBC(max. 2.5us)

**Refresh Configuration Register**

The refresh configuration register (RCR) defines how the device performs its self refresh. Altering the refresh parameters can reduce current consumption during standby mode. The RCR is accessed with CRE HIGH and A[19:18] = 00b; or through the register access software sequence with A = 0000h on the third cycle.

A19~A18	A7	A4	A2~A0
RS	PAGE	DPD	PAR

Register Select			Page		Deep Power Down		Partial Refresh			
A19	A18	RS	A7	PAGE	A4	DPD	A2	A1	A0	PAR
0	0	RCR	0	Disable	0	Enable	0	0	0	Full Array (default)
1	0	BCR	1	Enable(default)	1	Disable (default)	0	0	1	Bottom 1/2 Array
0	1	DIDR					0	1	0	Bottom 1/4 Array
							0	1	1	Bottom 1/8 Array
							1	0	0	None of Array
							1	0	1	Bottom 1/2 Array
							1	1	0	Bottom 1/4 Array
							1	1	1	Bottom 1/8 Array

- A3, A5, A6, A8~A15, A16, A17, A20, A21 are reserved and should be '1'
- The registers are set automatically to default value.

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**Burst Length (BCR[2:0]) Default = Continuous Burst**

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, 32 words or continuous.

**Burst Wrap (BCR[3]) Default = No Wrap**

The burst-wrap option determines if a 4-, 8-, 16-, or 32-word READ or WRITE burst wraps within the burst length, or steps through sequential addresses.

**Sequence and Burst Length**

Burst Wrap		Starting Address	4 word Burst Length	8 word Burst Length	16 word Burst Length	32 word Burst Length	Continuous Burst
BCR[3]	Wrap	Decimal	Linear	Linear	Linear	Linear	Linear
WRAP	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-29-30-31	0-1-2-3-4-5-~
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-30-31-0	1-2-3-4-5-6-~
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-31-0-1	2-3-4-5-6-7-~
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-0-1-2	3-4-5-6-7-8-~
		~		~	~	~	~
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-~4-5-6	7-8-9-10-11-12-~
		~			~	~	~
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-~12-13-14	15-16-17-18-19-20-~
		~				~	~
		31				31-0-1-~28-29-30	31-32-33-34-35-36-~
No WRAP	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-29-30-31	0-1-2-3-4-5-~
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-30-31-32	1-2-3-4-5-6-~
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-31-32-33	2-3-4-5-6-7-~
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-32-33-34	3-4-5-6-7-8-~
		~		~	~	~	~
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7-8-9-36-37-38	7-8-9-10-11-12-~
		~			~	~	~
		15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17-44-45-46	15-16-17-18-19-20-~
		~				~	~
		31				31-32-33-60-61-62	31-32-33-34-35-36-~

**Drive Strength (BCR[5:4]) Default = 1/2 Drive Strength**

The optimization of output driver strength is possible to adjust for the different data loadings. The device can minimize the noise generated on the data bus during read operation. The device supports full, 1/2 and 1/4 driver strength. The device's default mode is 1/2 driver strength. Outputs are configured at 1/2 drive strength during testing.

**Drive Strength**

Driver Strength	Full	1 / 2	1 / 4
Impedance(typ.)	25~30Ω	50Ω	100Ω
Recommendation	CL = 30pF to 50pF	CL = 15pF to 30pF 104 MHz at light load	CL = 15pF or lower

1. Impedance values are typical values, not 100% tested.

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### WAIT Configuration (BCR[8]) Default = 1 CLK Prior

The  $\overline{\text{WAIT}}$  signal is output signal indicating the status of the data on the bus whether or not it is valid.  $\overline{\text{WAIT}}$  configuration is to decide the timing when  $\overline{\text{WAIT}}$  asserts or deasserts.  $\overline{\text{WAIT}}$  asserts (or deasserts) one clock prior to the data when A8 is set to 0. ( $\overline{\text{WAIT}}$  asserts (or deasserts) at data clock when A8 is set to 1).  $\overline{\text{WAIT}}$  polarity is to decide the  $\overline{\text{WAIT}}$  signal level at which data is valid or invalid. Data is valid if  $\overline{\text{WAIT}}$  signal is high when A10 is set to 0. (Data is valid if  $\overline{\text{WAIT}}$  signal is low when A10 is set to 1). All the timing diagrams in this SPEC are illustrated based on following setup; A[10]:0 and A[8]:1.

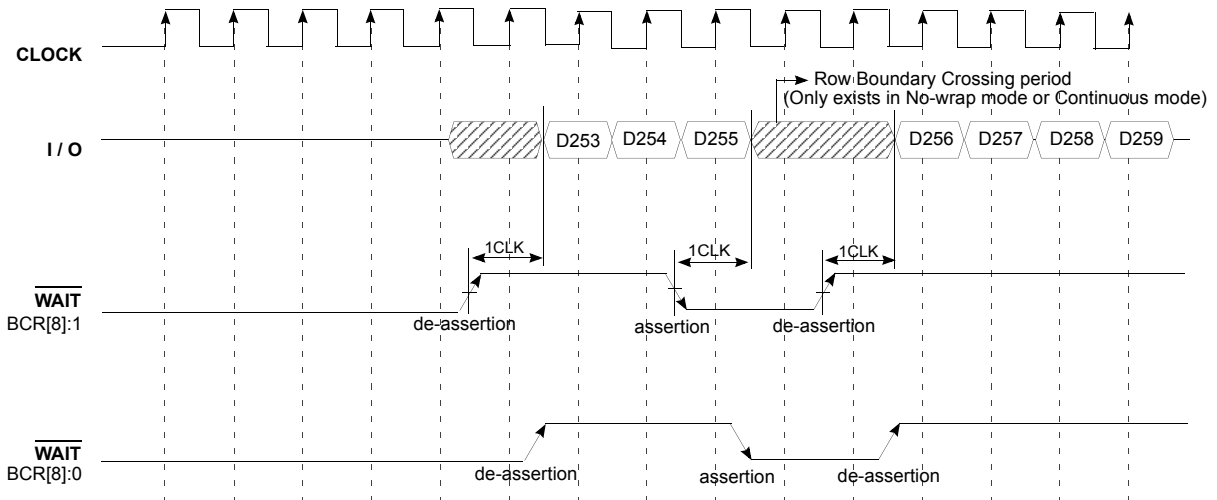
Below timing shows  $\overline{\text{WAIT}}$  signal's movement when word boundary crossing happens in No-wrap mode

### WAIT Polarity (BCR[10]) Default = Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

### WAIT Configuration During Burst Operation

No-Wrap. Row Boundary Crossing. LATENCY : 2. WP : Low Enable



Note: Non-default BCR setting: WAIT active LOW.

### Operating Mode (BCR[15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

### Latency Counter (BCR[13:11]) Default = 3 Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes.

### Initial Access Latency (BRC[14]) Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations. Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter.

Variable Latency Configuration Codes

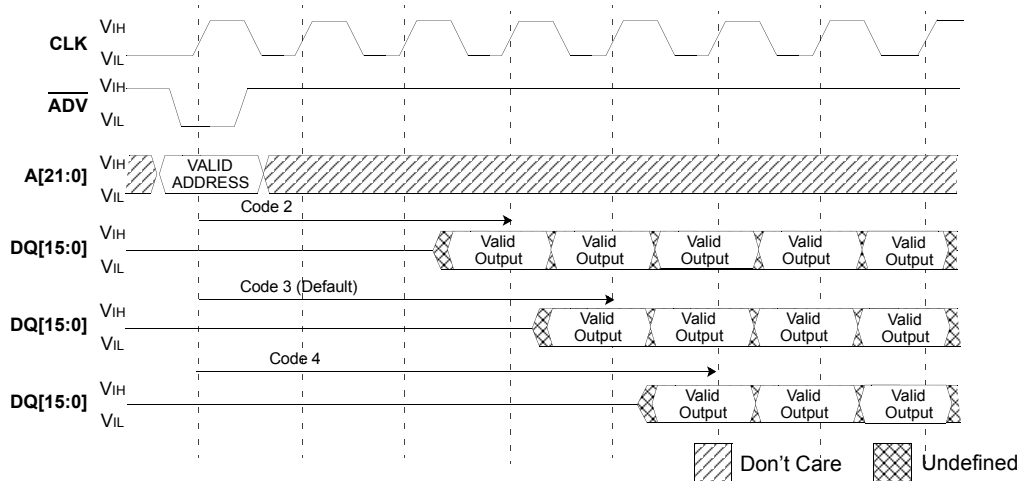
BCR[13:11]	Latency Configuration	Latency		Max Input CLK Frequency (MHz)		
		Normal	Refresh Collision	104	80	66
010	2(3 clocks)	2	4	66(15ns)	52(19,2ns)	40(25ns)
011	3(4 clocks)-default	3	6	104(9.62ns)	80(12.5ns)	66(15ns)
Others	Reserved	-	-	-	-	-

Fixed Latency Configuration Codes

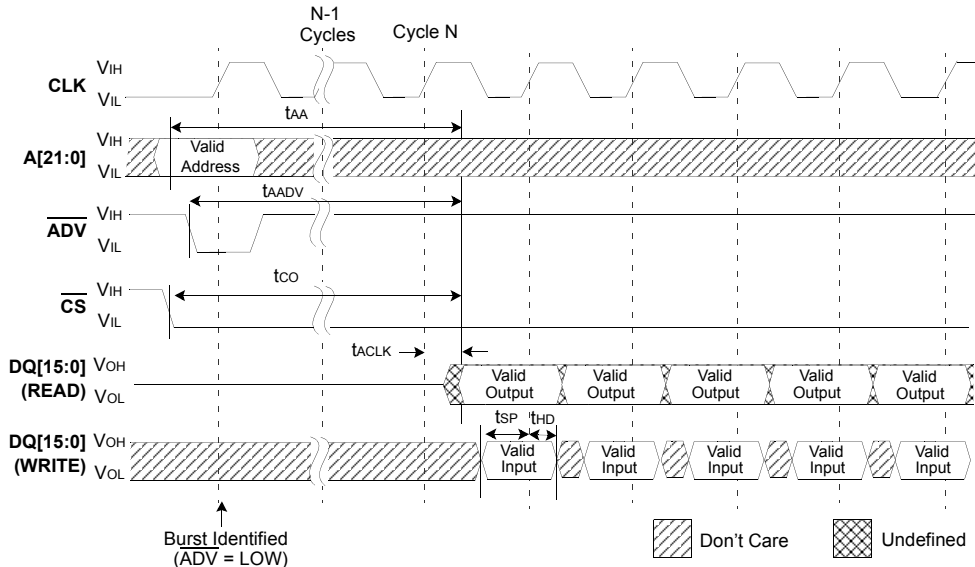
BCR[13:11]	Latency Configuration	Latency Count (N)	Max Input CLK Frequency (MHz)		
			104	80	66
010	2 (3 clocks)	2	33 (30ns)	20 (50ns)	20 (50ns)
011	3 (4 clocks)	3	52 (19.2ns)	40 (25ns)	33 (30ns)
100	4 (5 clocks)	4	66 (15ns)	52 (19.2ns)	40 (25ns)
101	5 (6 clocks)	5	80 (12.5ns)	66 (15ns)	52 (19.2ns)
110	6 (7 clocks)	6	104 (9.62ns)	80 (12.5ns)	66 (15ns)
Others	Reserved	-	-	-	-

1. Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.

Latency Counter (Variable Initial Latency, No Refresh Collision)



Latency Counter (Fixed Latency)



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### Partial Array Refresh (RCR[2:0]) Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

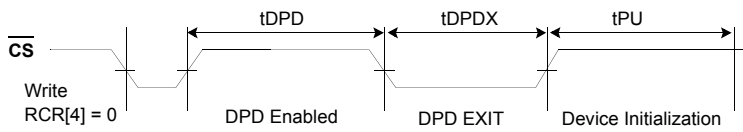
#### Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full Die	000000h-3FFFFFFh	4 Meg x 16	64Mb
0	0	1	One-half die	000000h-1FFFFFFh	2 Meg x 16	32Mb
0	1	0	One-quarter of die	000000h-0FFFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h-07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	200000h-3FFFFFFh	2 Meg x 16	32Mb
1	1	0	One-quarter of die	300000h-3FFFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	380000h-3FFFFFFh	512K x 16	8Mb

### Deep Power-Down (RCR[4]) Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by this memory. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the device will require 150µs to perform an initialization procedure before normal operations can resume. Deep power-down is enabled by setting RCR[4] = 0 and taking  $\overline{CS}$  HIGH. DPD can be enabled using CRE or the software sequence to access the RCR. Taking  $\overline{CS}$  LOW for at least 10µs disables DPD and sets RCR[4] = 1. It is not necessary to write to the RCR to disable DPD. BCR and RCR values (other than BCR[4]) are preserved during DPD.

#### DPD Entry and Exit Timing Parameters & Initialization and DPD Timing Parameters



Symbol	Min	Max	Unit
tDPD	10		µs
tDPDX	10		µs
tPU		150	µs

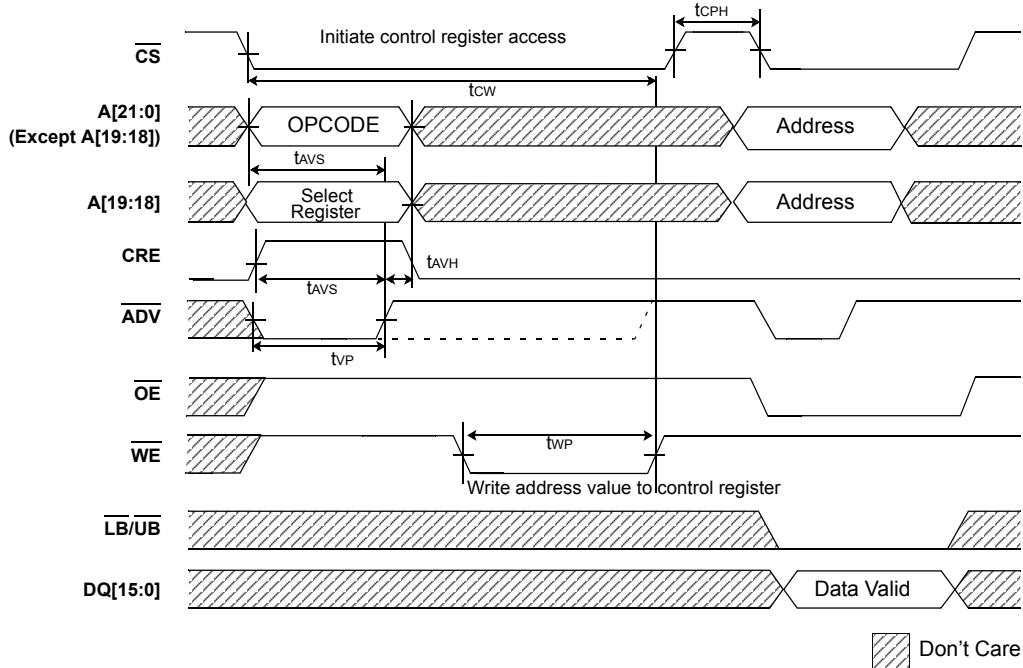
### Device Identification Register

The DIDR provides information on the device manufacturer, generation and the specific device configuration. This register is read-only. The DIDR is accessed with CRE HIGH and A[19:18] = 01b, or through the register access software sequence with A = 0002h on the third cycle.

#### Device Identification Register Mapping

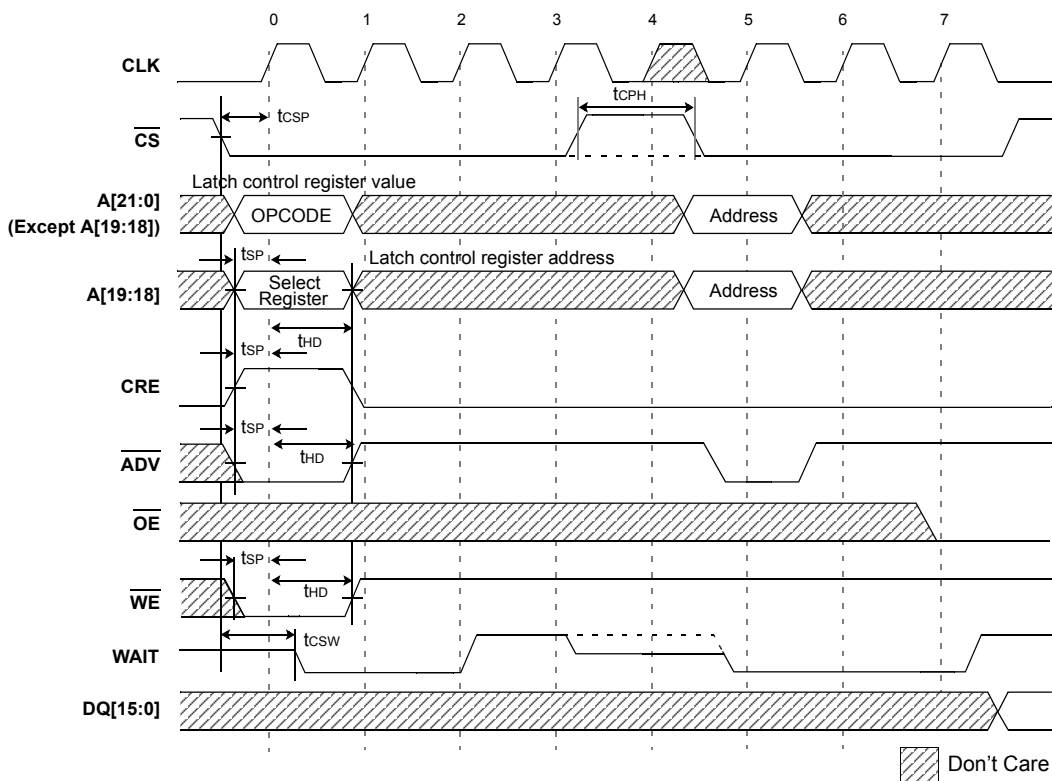
Bit Field	DIDR[15]		DIDR[14:11]		DIDR[10:8]		DIDR[7:5]		DIDR[4:0]
Field name	Row Length		Device version		Device density		U <sub>t</sub> RAM generation		Vendor ID
	Length	Bit Setting	Version	Bit Setting	Density	Bit Setting	Generation	Bit Setting	Bit Setting
Options	256 words	1b	5th	100b	64Mb	010b	U <sub>t</sub> RAM2	010b	01100

**Configuration Register WRITE, Asynchronous Mode, Followed by READ ARRAY Operation**



1.  $A[19:18] = 00b$  to load RCR, and  $10b$  to load BCR.

**Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation**

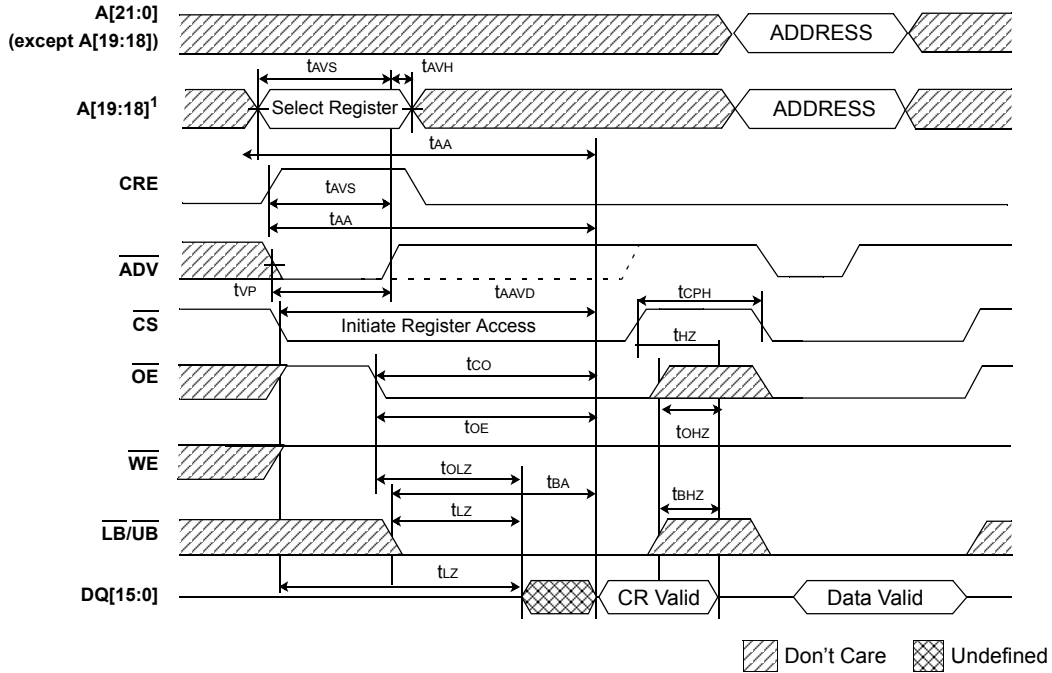


1. Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: Latency code two (three clocks);  $\overline{WAIT}$  active LOW;  $\overline{WAIT}$  asserted during delay.
2.  $A[19:18] = 00b$  to load RCR, and  $10b$  to load BCR.
3.  $\overline{CS}$  must remain LOW to complete a burst-of-one WRITE.  $\overline{WAIT}$  must be monitored—additional  $\overline{WAIT}$  cycles caused by refresh collisions require a corresponding number of additional  $\overline{CS}$  LOW cycles.

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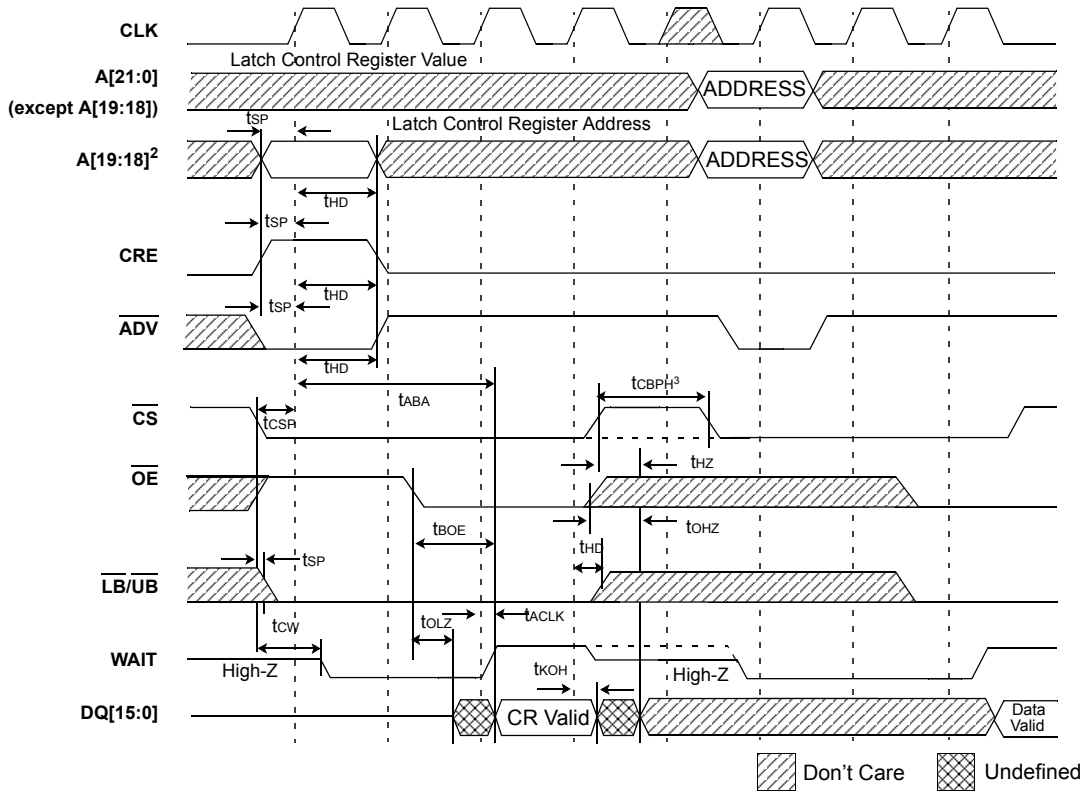
U<sub>t</sub>RAM2

Register READ, Asynchronous Mode Followed by READ ARRAY Operation



1. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

Register READ, Synchronous Mode Followed by READ ARRAY Operation

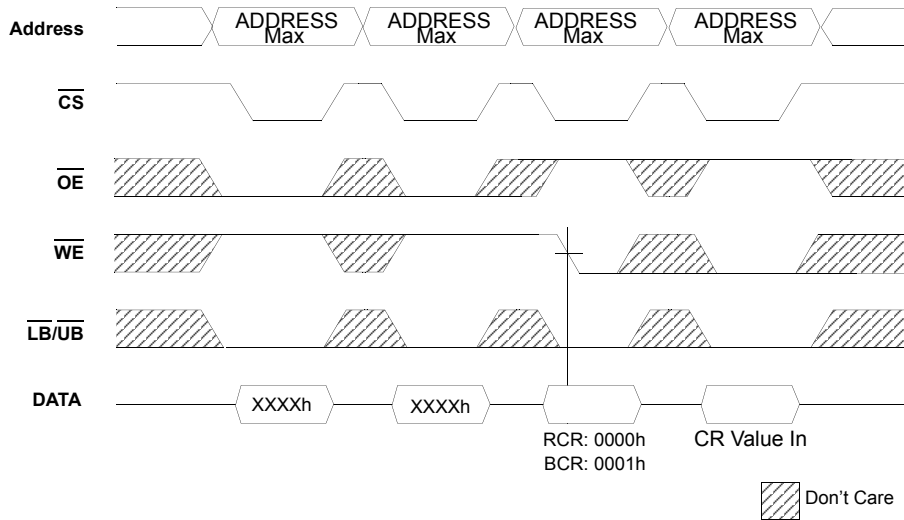


1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.
3. CS must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CS LOW cycles.

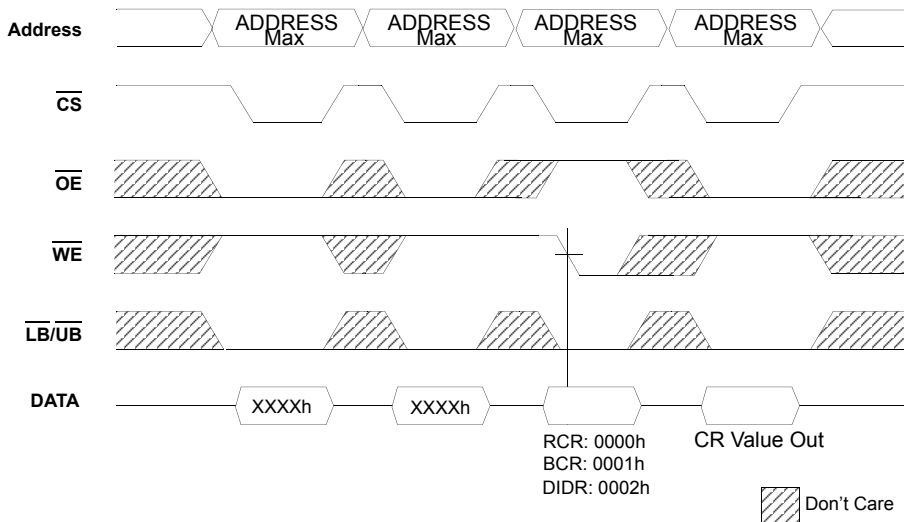
**Software Access**

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence. The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations. The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation. The address used during all READ and WRITE operations is the highest address of the device being accessed (3FFFFFF); the contents of this address are not changed by using this sequence. The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ[15:0] transfer data in to or out of bits 15–0 of the registers. The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

**Load Configuration Register**



**Read Configuration Register**





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**BUS OPERATING MODES**

The bus interface supports asynchronous and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR.

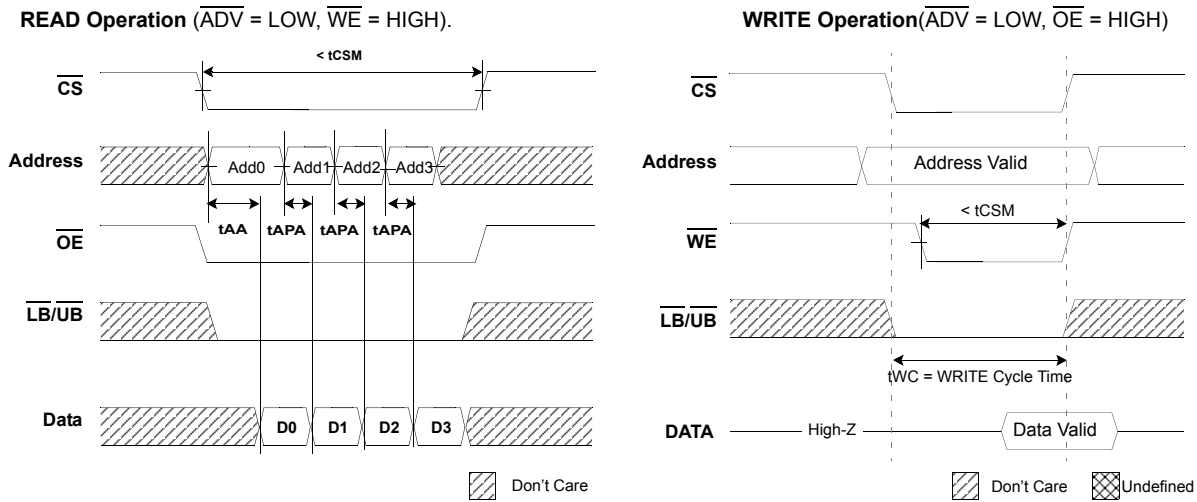
**Asynchronous Mode (default mode)**

**Asynchronous (Page) read operation**

Asynchronous read operation starts when  $\overline{CS}$ ,  $\overline{OE}$  and  $\overline{UB}$  or  $\overline{LB}$  are asserted.  $\overline{ADV}$  can be taken HIGH to capture the address. First data will be driven out of the DQ bus after random access time( $t_{AA}$ ) and second, third and fourth data can be driven out after page access time( $t_{APA}$ ) when using the page addresses (A0, A1).  $\overline{WE}$  should be de-asserted during read operation. The CLK input must be held static LOW during read operation. WAIT will be driven while the device is enabled and its state should be ignored.

**Asynchronous write operation**

Asynchronous write operation starts when  $\overline{CS}$ ,  $\overline{WE}$  and  $\overline{UB}$  or  $\overline{LB}$  are asserted. The data to be written is latched on the rising edge of  $\overline{CS}$ ,  $\overline{WE}$ , or  $\overline{LB}/\overline{UB}$  (whichever occurs first).  $\overline{OE}$  is don't care during write operation and  $\overline{WE}$  will override  $\overline{OE}$ .  $\overline{WE}$  LOW time must be limited to  $t_{CSM}$ . The CLK input must be held static LOW during write operation. WAIT signal is Hi-Z.



**Functional Description (Asynch. mode)**

Asynchronous Mode BCR[15] = 1	Power	CLK	$\overline{ADV}$	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	CRE	$\overline{UB}/\overline{LB}$	WAIT	DQ[15:0]	Notes
Read	Active	L	L	L	L	H	L	L	Low-Z	Data out	4
Write	Active	L	L	L	X	L	L	L	Low-Z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5,6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4,6
Configuration register write	Active	L	L	L	X	L	H	X	Low-Z	High-Z	
Configuration register read	Active	L	L	L	L	H	H	L	Low-Z	Config. Reg.out	
DPD	Deep Power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

1. CLK must be LOW during asynch read and asynch write modes; and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When  $\overline{LB}$  and  $\overline{UB}$  are in select mode (LOW), DQ[15:0] are affected. When only  $\overline{LB}$  is in select mode, DQ[7:0] are affected. When only  $\overline{UB}$  is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. VIN = VCCQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when  $\overline{CS}$  transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until  $\overline{CS}$  transitions from HIGH to LOW.

**Burst Mode Operation**

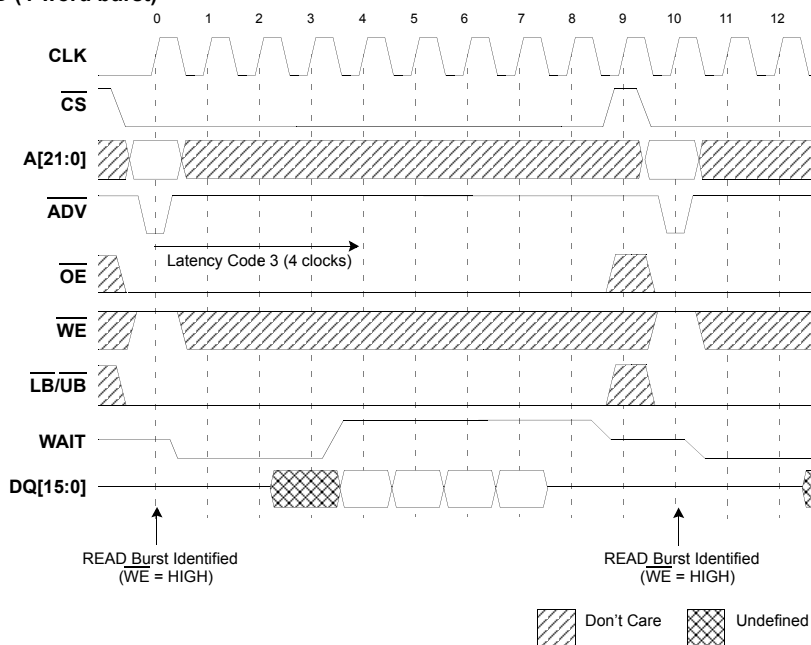
**Synchronous Burst Read Operation**

Burst Read command is implemented when  $\overline{ADV}$  is detected low at clock rising edge.  $\overline{WE}$  should be de-asserted. Burst operation re-starts whenever  $\overline{ADV}$  is detected low at clock rising edge even in the middle of operation.

**Synchronous Burst Write Operation**

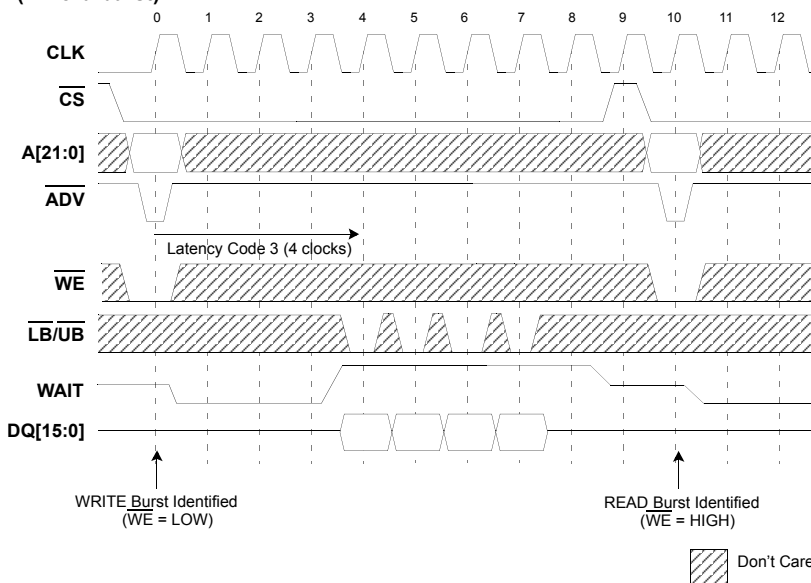
Burst Write command is implemented when  $\overline{ADV}$  &  $\overline{WE}$  are detected low at clock rising edge. Burst Write operation re-starts whenever  $\overline{ADV}$  is detected low at clock rising edge even in the middle of Burst Write operation.

**Burst Mode READ (4-word burst)**



1. Non-default BCR settings for burst mode READ (4-word burst): Fixed or variable latency;
2. Latency code 3 (4 clocks); WAIT active LOW; WAIT asserted during delay.
3. Diagram in the figure above is representative of variable latency with no refresh collision or fixed-latency access.

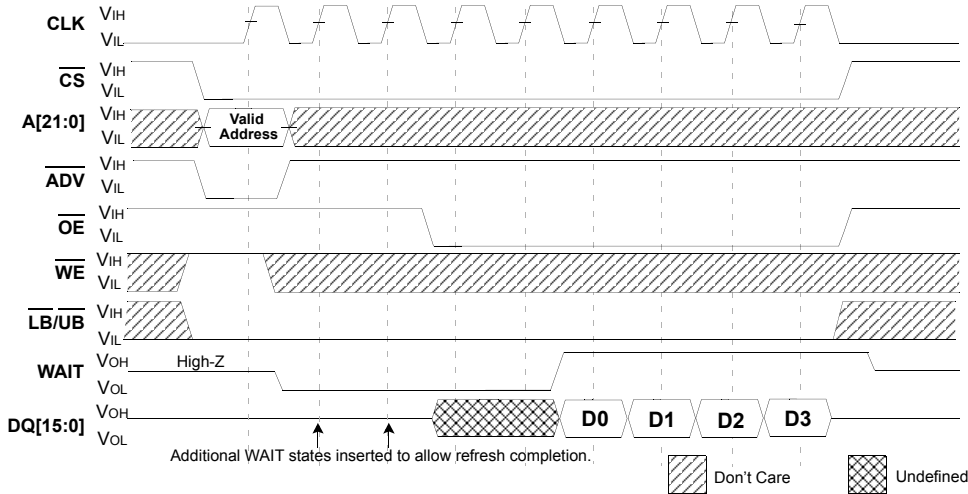
**Burst Mode WRITE (4-word burst)**



1. Non-default BCR settings for burst mode WRITE (4-word burst): Fixed or variable latency;
2. Latency code 3 (4 clocks); WAIT active LOW; WAIT asserted during delay.

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles. Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

**Refresh Collision During Variable-Latency READ Operation**



1. Non-default BCR settings for refresh collision during variable-latency READ operation:
2. Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

**Functional Description (Synch. mode)**

Burst Mode BCR[15] = 0	Power	CLK	ADV	CS	OE	WE	CRE	UB / LB	WAIT	DQ[15:0]	Notes
Async read	Active	L	L	L	L	H	L	L	Low-Z	Data out	4,8
Async write	Active	L	L	L	X	L	L	L	Low-Z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5,6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4,6
Initial burst read	Active		L	L	X	H	L	L	Low-Z	X	4,9
Initial burst write	Active		L	L	H	L	L	X	Low-Z	X	4,9
Burst continue	Active		H	L	X	X	X	L	Low-Z	Data in or Data out	4,9
Burst suspend	Active	X	X	L	H	X	X	X	Low-Z	High-Z	4,9
Configuration register write	Active		L	L	X	L	H	X	Low-Z	High-Z	9,10
Configuration register read	Active		L	L	L	H	H	L	Low-Z	Config. reg.out	9,10
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

1. CLK must be LOW during async read and async write modes; and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB and UB are in select mode (LOW), DQ[15:0] are affected. When only LB is in select mode, DQ[7:0] are affected. When only UB is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. VIN = VCCQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when CS transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CS transitions from HIGH to LOW.
8. When the BCR is configured for sync mode, sync READ and WRITE, and async WRITE are supported by all vendors. (Some vendors also support asynchronous READ.)
9. Burst mode operation is initialized through the bus configuration register (BCR[15]).
10. Initial cycle. Following cycles are the same as BURST CONTINUE. CS must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).

**Mixed-Mode Operation**

The device supports a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous WRITE operations require that the clock (CLK) remain LOW during the entire sequence. The  $\overline{ADV}$  signal can be used to latch the target address,  $\overline{CS}$  can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; however, the  $\overline{CS}$  LOW time must not exceed tCSM. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers.

**Burst Suspend**

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended,  $\overline{OE}$  should be taken HIGH to disable the outputs. otherwise,  $\overline{OE}$  can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence,  $\overline{OE}$  is taken LOW, then CLK is restarted after valid data is available on the bus. The  $\overline{CS}$  LOW time is limited by refresh considerations.  $\overline{CS}$  must not stay LOW longer than tCSM. If a burst suspension will cause  $\overline{CS}$  to remain LOW for longer than tCSM,  $\overline{CS}$  should be taken HIGH and the burst restarted with a new  $\overline{CS}$  LOW/ $\overline{ADV}$  LOW cycle.

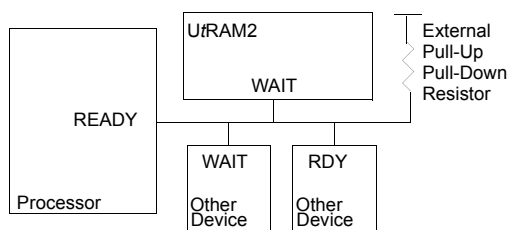
**Boundary Crossing**

Continuous bursts or No wrap burst have the ability to start at a specified address and burst to the end of the address. It goes back to the first address and continues the burst operation. WAIT will be asserted at the boundary of the row and be desasserted after crossing boundary of the row.

**WAIT Operation**

The WAIT output is typically connected to a shared systemlevel WAIT signal. The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus. Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that additional time is required before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into this device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.  $\overline{CS}$  must remain asserted during WAIT cycles (WAIT asserted and WAIT configuration BCR[8] = 1). Bringing  $\overline{CS}$  HIGH during WAIT cycles may cause data corruption. (Note that for BCR[8] = 0, the actual WAIT cycles end one cycle after WAIT deasserts. When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed. When the refresh operation has completed, the READ operation will continue normally. WAIT will be asserted but should be ignored during asynchronous READ and WRITE operations. By using fixed initial latency (BCR[14] = 1), this device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst.

**Wired or WAIT Configuration**



**LB / UB Operation**

The LB enable and UB enable signals support byte-wide data WRITES. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of  $\overline{CS}$ ,  $\overline{WE}$ , LB, or UB, whichever occurs first. LB and UB must be LOW during READ cycles. When both the LB and UB are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as  $\overline{CS}$  remains LOW.

## **LOW-POWER OPERATION**

### **Temperature Compensated Self Refresh**

Temperature compensated self refresh (TCSR) allows for adequate refresh at different temperatures. This U $\dagger$ RAM2 device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

### **Partial Array Refresh**

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

### **Deep Power-Down Operation**

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the U $\dagger$ RAM2 device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the U $\dagger$ RAM2 device will require 150 $\mu$ s to perform an initialization procedure before normal operations can resume. During this 150 $\mu$ s period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification. DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when  $\overline{CS}$  goes HIGH. DPD is disabled the next time  $\overline{CS}$  goes LOW and stays LOW for at least 10 $\mu$ s.

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**AC Input/Output Reference Waveform & AC Output Load Circuit**



1. AC test inputs are driven at VCCQ for a logic 1 and VSSQ for a logic 0. Input rise and fall times (10% to 90%) <1.6ns.
2. Input timing begins at VCCQ/2 and Output timing ends at VCCQ/2.
3. All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b)

**TIMING REQUIREMENTS**

**Asynchronous READ Cycle Timing Requirements**

Parameter	Symbol	Min	Max	Unit	Notes
Address access time	tAA		70	ns	
ADV access time	tAADV		70	ns	
Page access time	tAPA		20	ns	
Address setup to $\overline{ADV}$ HIGH	tAVS	5		ns	
Address hold from $\overline{ADV}$ going HIGH	tAVH	2		ns	
$\overline{LB}/\overline{UB}$ access time	tBA		70	ns	
$\overline{LB}/\overline{UB}$ disable to DQ High-Z output	tBHZ		8	ns	1
$\overline{LB}/\overline{UB}$ enable to Low-Z output	tBLZ	10		ns	2
Maximum $\overline{CS}$ pulse width	tCSM		2.5	us	4
$\overline{CS}$ LOW to WAIT valid	tCSW	1	7.5	ns	
Chip select access time	tCO		70	ns	
$\overline{CS}$ LOW to $\overline{ADV}$ HIGH	tCVS	7		ns	
Chip disable to DQ and WAIT High-Z output	tHZ		8	ns	1
Chip enable to Low-Z output	tLZ	10		ns	2
Output enable to valid output	tOE		20	ns	
Output hold from address change	tOH	5		ns	
Output disable to DQ High-Z output	tOHZ		8	ns	1
Output enable to Low-Z output	tOLZ	5		ns	2
Page READ cycle time	tPC	20		ns	
READ cycle time	tRC	70		ns	
$\overline{ADV}$ pulse width LOW	tVP	5		ns	

**Asynchronous WRITE Cycle Timing Requirements**

Parameter	Symbol	Min	Max	Unit	Notes
Address and $\overline{ADV}$ LOW setup time	tAS	0		ns	
Address setup to $\overline{ADV}$ going HIGH	tAVS	5		ns	
Address hold from $\overline{ADV}$ going HIGH	tAVH	2		ns	
Address valid to end of WRITE	tAW	70		ns	
$\overline{LB}/\overline{UB}$ select to end of WRITE	tBW	70		ns	
$\overline{CS}$ LOW to WAIT valid	tCSW	1	7.5	ns	
$\overline{CS}$ HIGH between subsequent async operations	tCPH	5		ns	1,4
$\overline{CS}$ LOW to $\overline{ADV}$ HIGH	tCVS	7		ns	2
Chip enable to end of WRITE	tCW	70		ns	3
Data HOLD from WRITE time	tDH	0		ns	
Data WRITE setup time	tDW	20		ns	
Chip disable to WAIT High-Z output	tHZ		8	ns	
Chip enable to Low-Z output	tLZ	10		ns	1
End WRITE to Low-Z output	tOW	5		ns	2
$\overline{ADV}$ pulse width	tVP	5		ns	
$\overline{ADV}$ setup to end of WRITE	tVS	70		ns	
WRITE cycle time	tWC	70		ns	1
WRITE to DQ High-Z output	tWHZ		8	ns	2
WRITE pulse width	tWP	55		ns	
WRITE pulse width HIGH	tWPH	10		ns	
WRITE recovery time	tWR	0		ns	

1. The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ/2.
2. The Low-Z timings measure a 100mV transition away from the High-Z (VCCQ/2) level toward either VOH or VOL.
3.  $\overline{WE}$  LOW time must be limited to tCSM (2.5µs).
4. A refresh opportunity must be provided every tCSM. A refresh opportunity is satisfied by the condition that  $\overline{CS}$  HIGH for longer than 15ns.  $\overline{CS}$  must not remain LOW longer than tCSM.

**K1C6416B2D**

**U<sub>t</sub>RAM2**

**Burst READ Cycle Timing Requirements**

Parameter	Symbol	104MHz		80MHz		66MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address access time (fixed latency)	tAA		70		70		70	ns	
ADV access time (fixed latency)	tAADV		70		70		70	ns	
Address hold from ADV going HIGH	tAVH	2		2		2		ns	
Burst to READ access time (variable latency)	tABA		35		46		55	ns	
CLK to output delay	tACLK		7		9		11	ns	
Burst OE LOW to output delay	tBOE		20		20		20	ns	
CS HIGH between subsequent burst or mixed mode operations	tCBPH	5		6		8		ns	3
Maximum CS pulse width	tCSM		2.5		2.5		2.5	μs	3
CS or ADV LOW to WAIT valid	tCSW	1	7.5	1	7.5	1	7.5	ns	
CLK period	tCLK	9.62		12.5		15		ns	
Chip select access time (fixed latency)	tCO		70		70		70	ns	
CS setup time to active CLK edge	tCSP	3		4		5		ns	
Hold time from active CLK edge	tHD	2		2		2		ns	
Chip disable to DQ and WAIT High-Z output	tHZ		8		8		8	ns	1
CLK rise or fall time	tKHKL		1.6		1.8		2.0	ns	
CLK to WAIT valid	tKHTL	2	7	2	9	2	11	ns	
Output HOLD from CLK	tKOH	2		2		2		ns	
CLK HIGH or LOW time	tKP	3		4		5		ns	
Output disable to DQ High-Z output	tOHZ		8		8		8	ns	1
Output enable to Low-Z output	tOLZ	5		5		5		ns	2
Setup time to active CLK edge	tSP	3		4		5		ns	
ADV HIGH to CLK Rising	tAHCRC	2		2		2		ns	

**Burst WRITE Cycle Timing Requirements**

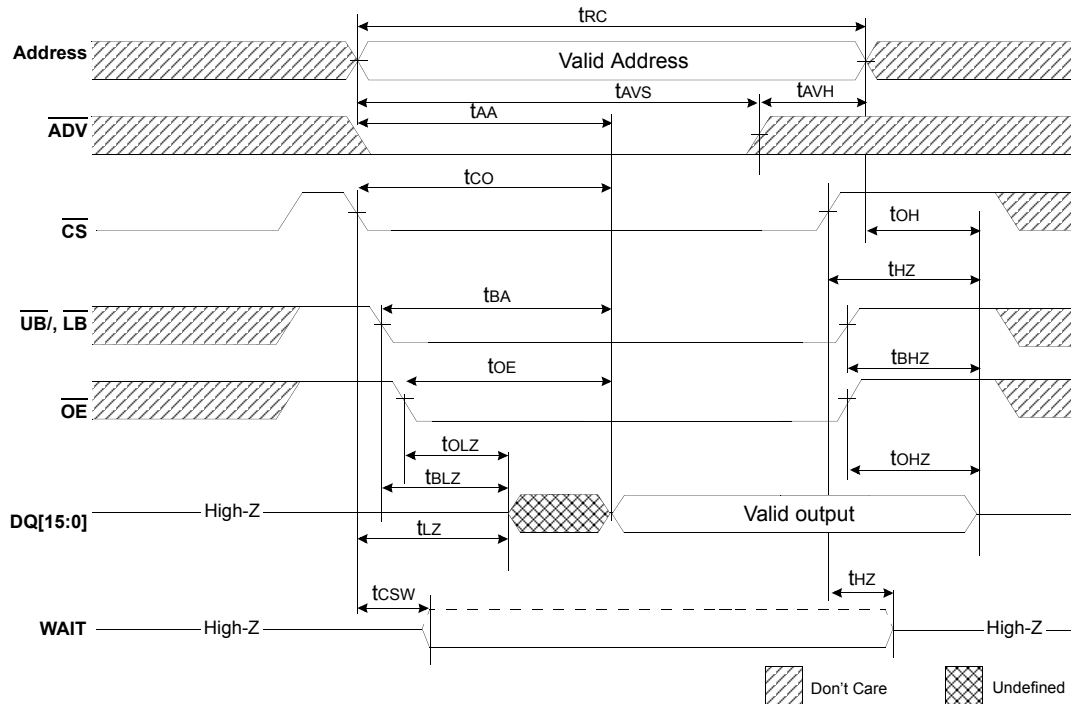
Parameter	Symbol	104MHz		80MHz		66MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address and ADV LOW setup time	tAS	0		0		0		ns	
Address hold from ADV going HIGH	tAVH	2		2		2		ns	
CS HIGH between subsequent burst or mixed mode operations	tCBPH	5		6		8		ns	3
Maximum CS pulse width	tCSM		2.5		2.5		2.5	μs	3
CS LOW to WAIT valid	tCSW	1	7.5	1	7.5	1	7.5	ns	
Clock period	tCLK	9.62		12.5		15		ns	
CS setup to CLK active edge	tCSP	3		4		5		ns	
Hold time from active CLK edge	tHD	2		2		2		ns	
Chip disable to WAIT High-Z output	tHZ		8		8		8	ns	1
Last clock to ADV LOW (fixed latency)	tKADV	15		15		15		ns	
CLK rise or fall time	tKHKL		1.6		1.8		2.0	ns	
Clock to WAIT valid	tKHTL	2	7	2	9	2	11	ns	
CLK HIGH or LOW time	tKP	3		4		5		ns	
Setup time to activate CLK edge	tSP	3		4		5		ns	
ADV HIGH to CLK Rising	tAHCRC	2		2		2		ns	

1. The High-Z timings measure a 100mV transition from either V<sub>OH</sub> or V<sub>OL</sub> toward V<sub>CCQ</sub>/2.
2. The Low-Z timings measure a 100mV transition away from the High-Z (V<sub>CCQ</sub>/2) level toward either V<sub>OH</sub> or V<sub>OL</sub>.
3. A refresh opportunity must be provided every t<sub>CSM</sub>. A refresh opportunity is satisfied by the condition that CS HIGH for longer than 15ns. CS must not remain LOW longer than t<sub>CSM</sub>.

**K1C6416B2D**

**U<sub>t</sub>RAM2**

**Asynchronous READ**  
(CRE=V<sub>IL</sub>, WE=V<sub>IH</sub>)



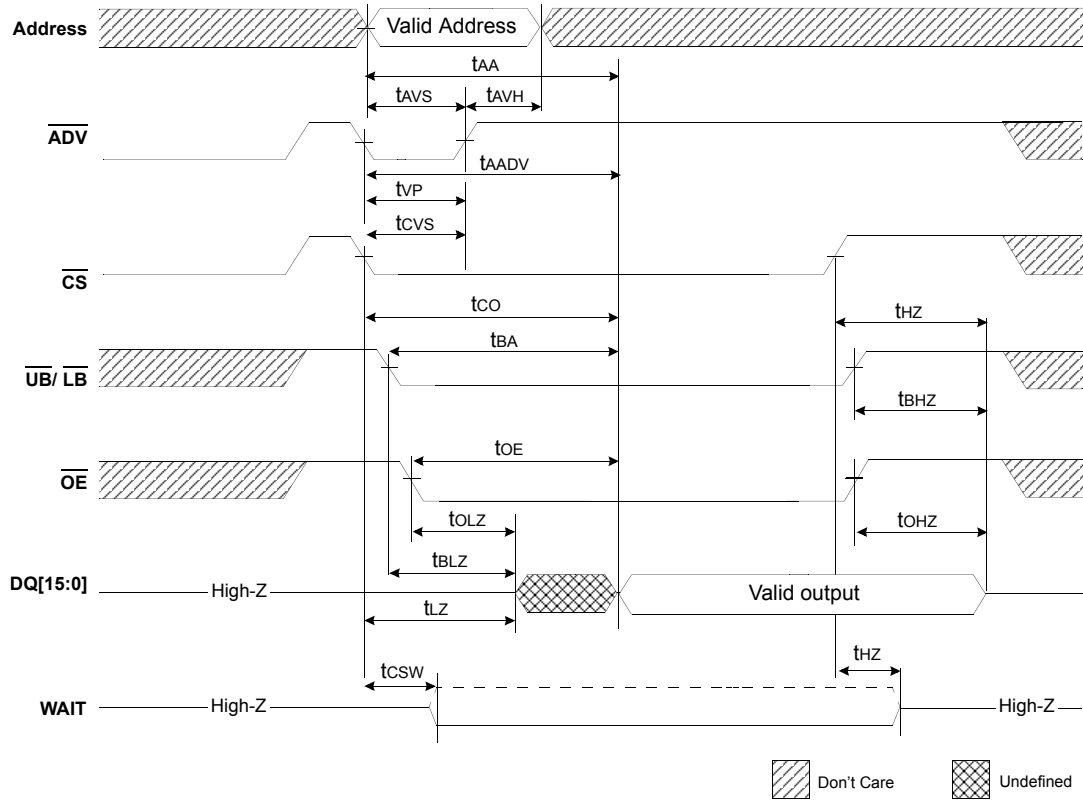
1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. t<sub>HZ</sub> and t<sub>OZH</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. At any given temperature and voltage condition, t<sub>HZ</sub>(Max.) is less than t<sub>LZ</sub>(Min.) both for a given device and from device to device interconnection.
4. t<sub>OE</sub>(max) is met only when OE becomes enabled after t<sub>AA</sub>(max).
5. If invalid address signals shorter than min. t<sub>RC</sub> are continuously repeated for over 2.5us, the device needs a normal read timing(t<sub>RC</sub>) or needs to sustain standby state for min. t<sub>RC</sub> at least once in every 2.5us.



**K1C6416B2D**

**U<sub>t</sub>RAM2**

**Asynchronous READ Using ADV**  
(CRE=V<sub>IL</sub>, WE=V<sub>IH</sub>)

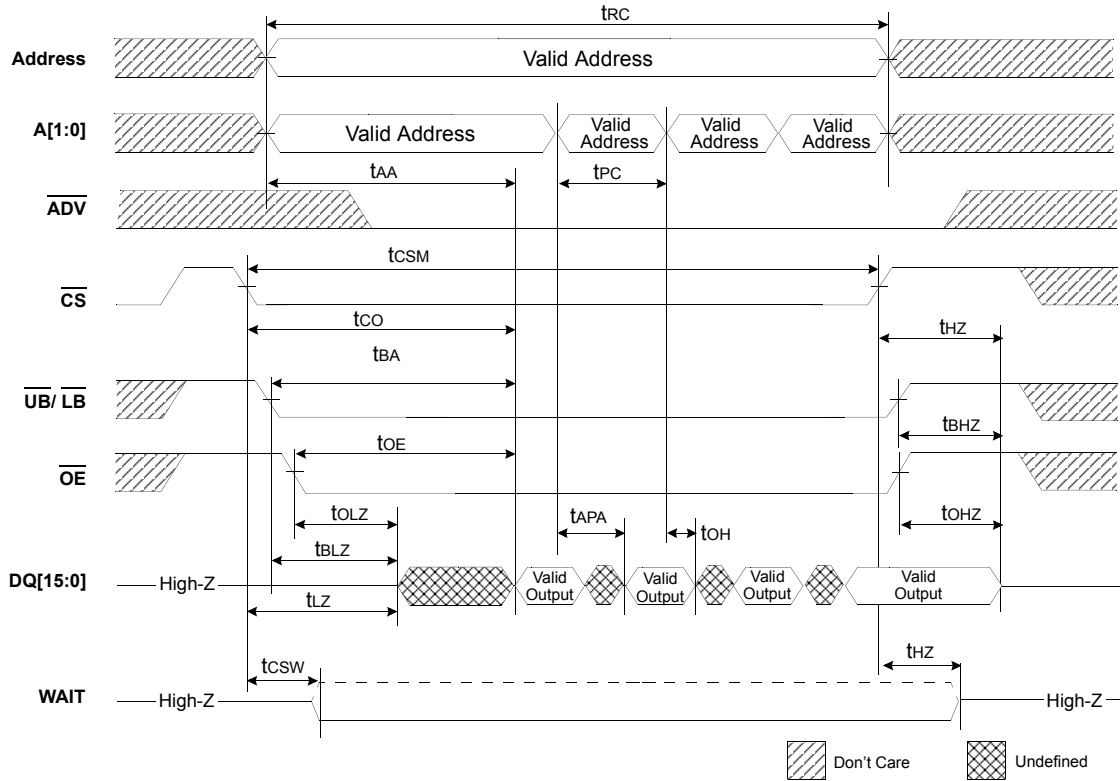


1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
4. tOE(max) is met only when OE becomes enabled after tAA(max).
5. If invalid address signals shorter than min. tRC are continuously repeated for over 2.5us, the device needs a normal read timing(tRC) or needs to sustain standby state for min. tRC at least once in every 2.5us.

# K1C6416B2D

# U<sub>t</sub>RAM2

## PAGE MODE READ (CRE=V<sub>IL</sub>, WE=V<sub>IH</sub>)

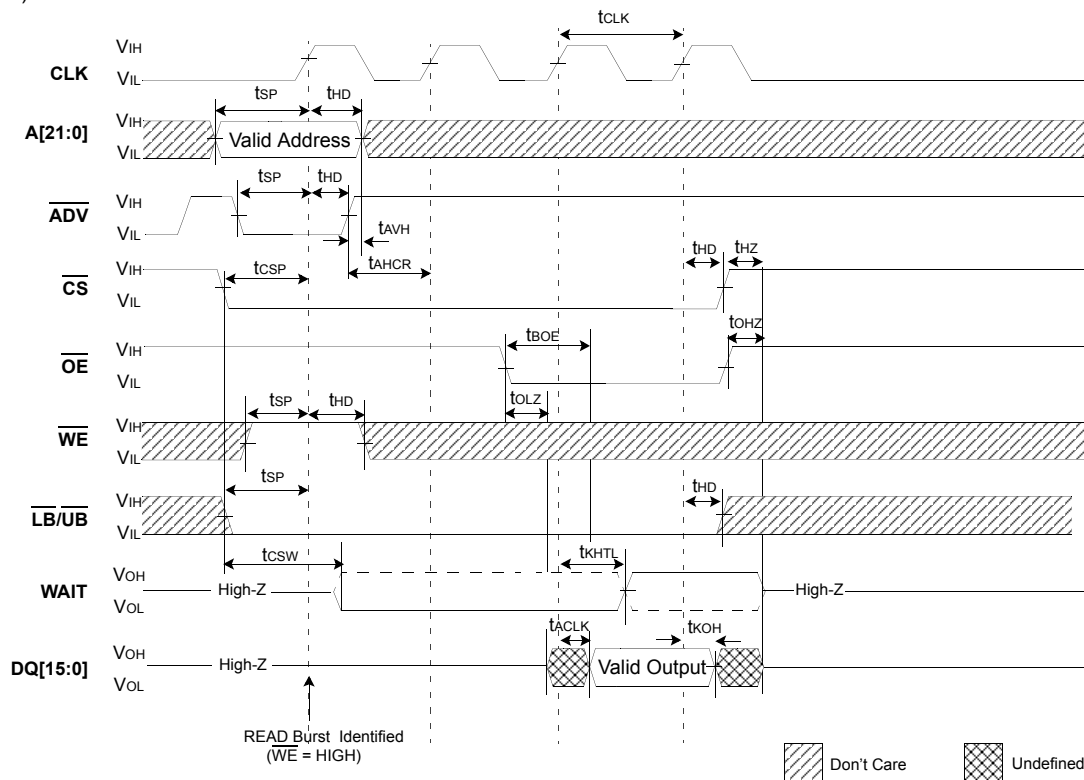


1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. At any given temperature and voltage condition, t<sub>HZ</sub>(Max.) is less than t<sub>LZ</sub>(Min.) both for a given device and from device to device interconnection.
4. t<sub>OE</sub>(max) is met only when OE becomes enabled after t<sub>AA</sub>(max).
5. If invalid address signals shorter than min. t<sub>RC</sub> are continuously repeated for over 2.5us, the device needs a normal read timing(t<sub>RC</sub>) or needs to sustain standby state for min. t<sub>RC</sub> at least once in every 2.5us.

K1C6416B2D

U<sub>t</sub>RAM2

Single-Access Burst READ Operation—Variable Latency  
(CRE=V<sub>IL</sub>)

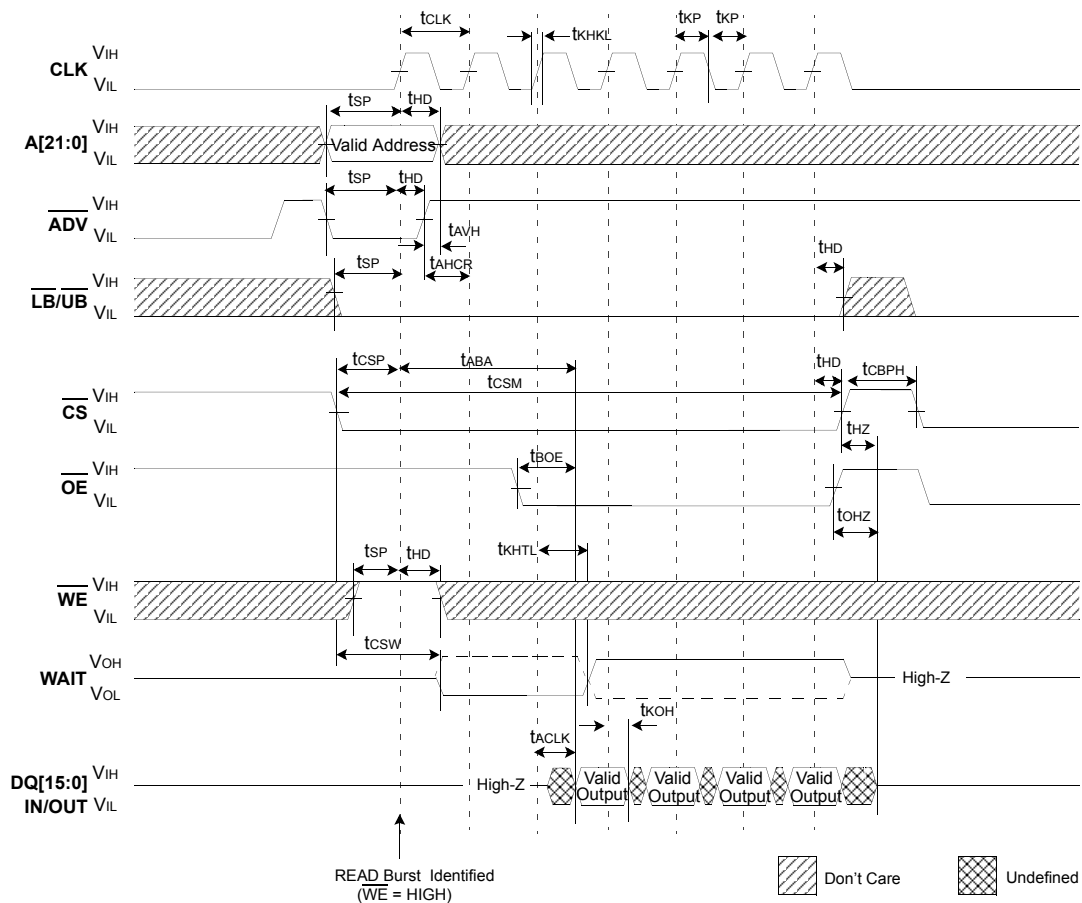


1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

# K1C6416B2D

# U<sub>t</sub>RAM2

## 4-Word Burst READ Operation—Variable Latency (CRE=V<sub>IL</sub>)

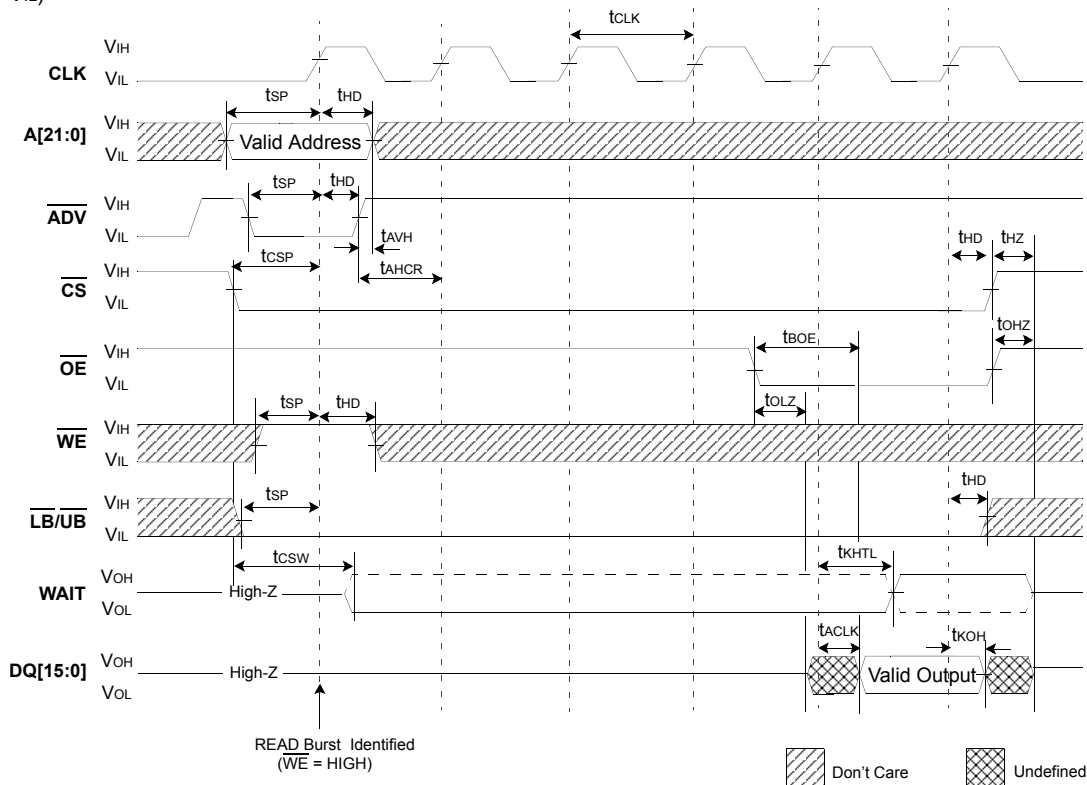


1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

# K1C6416B2D

# U<sub>t</sub>RAM2

## Single-Access Burst READ Operation—Fixed Latency (CRE=V<sub>IL</sub>)

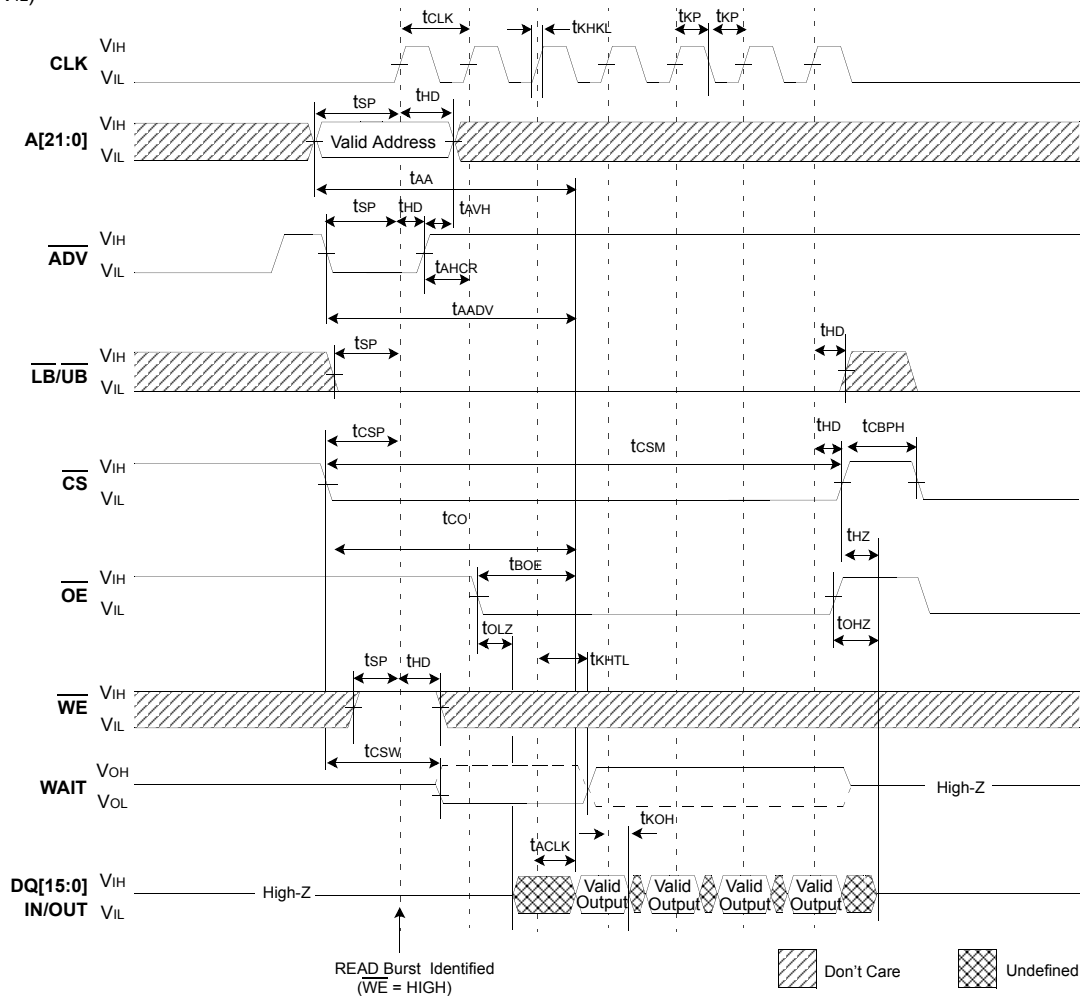


1. Non-default BCR settings: Fixed latency; latency code four (five clocks); WAIT active LOW; WAIT asserted during delay.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

**K1C6416B2D**

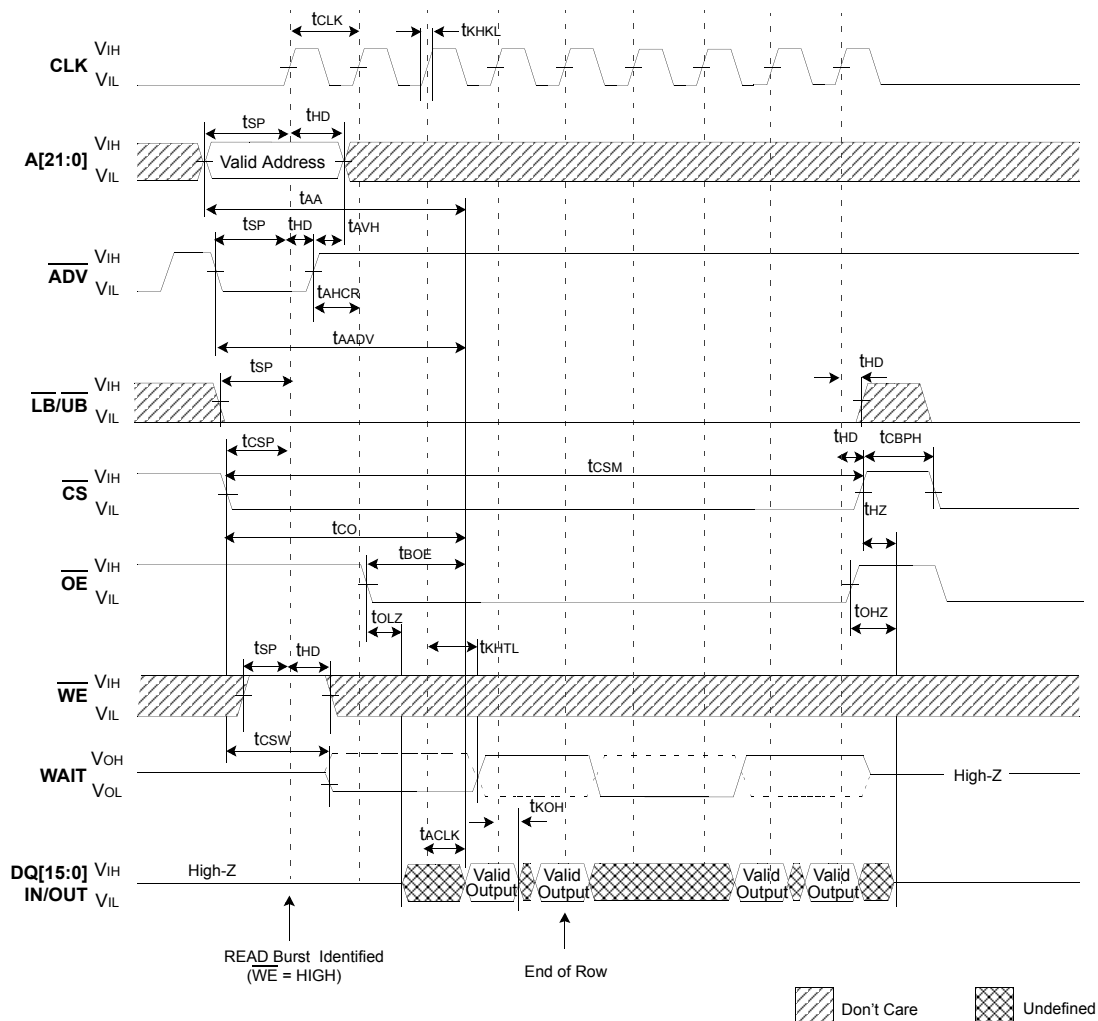
**UtRAM2**

**4-Word Burst READ Operation—Fixed Latency**  
(CRE=V<sub>IL</sub>)



1. Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

**4-Word Burst READ Operation— Row Boundary Crossing**  
(CRE=V<sub>IL</sub>)

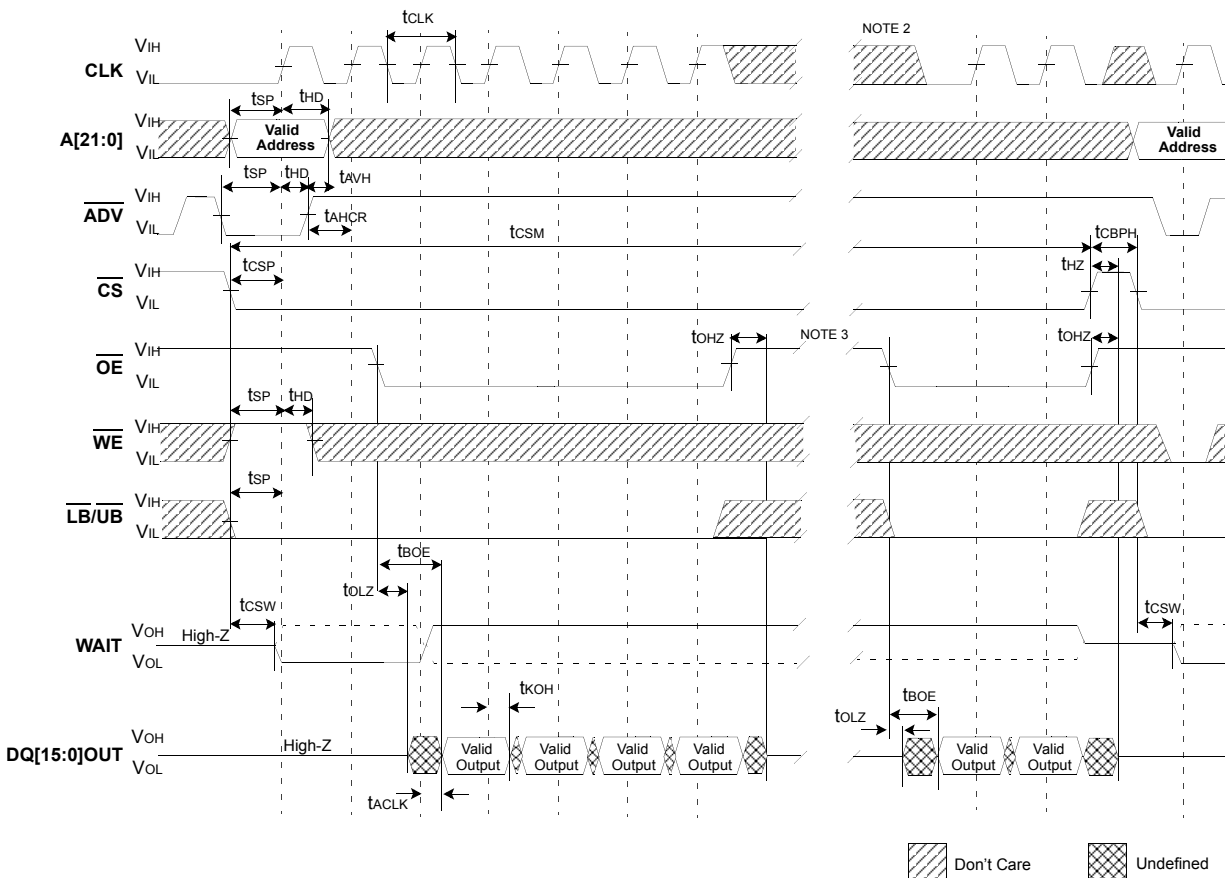


1. Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

# K1C6416B2D

# UtRAM2

## READ Burst Suspend (CRE=V<sub>IL</sub>)



**Notes:**

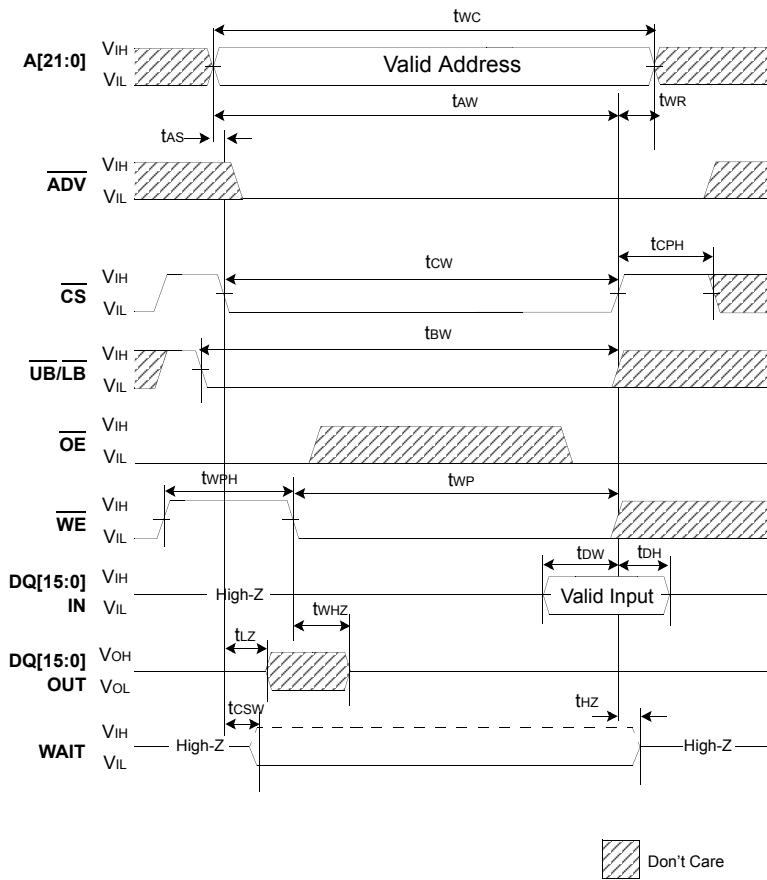
1. Non-default BCR settings for READ burst suspend: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. CLK can be stopped LOW or HIGH, but must be static, with no LOW-to-HIGH transitions during burst suspend.
3. OE can stay LOW during burst suspend. If OE is LOW, DQ[15:0] will continue to output valid data.
4. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.



K1C6416B2D

U<sub>t</sub>RAM2

CS-Controlled Asynchronous WRITE  
(CRE=V<sub>IL</sub>)

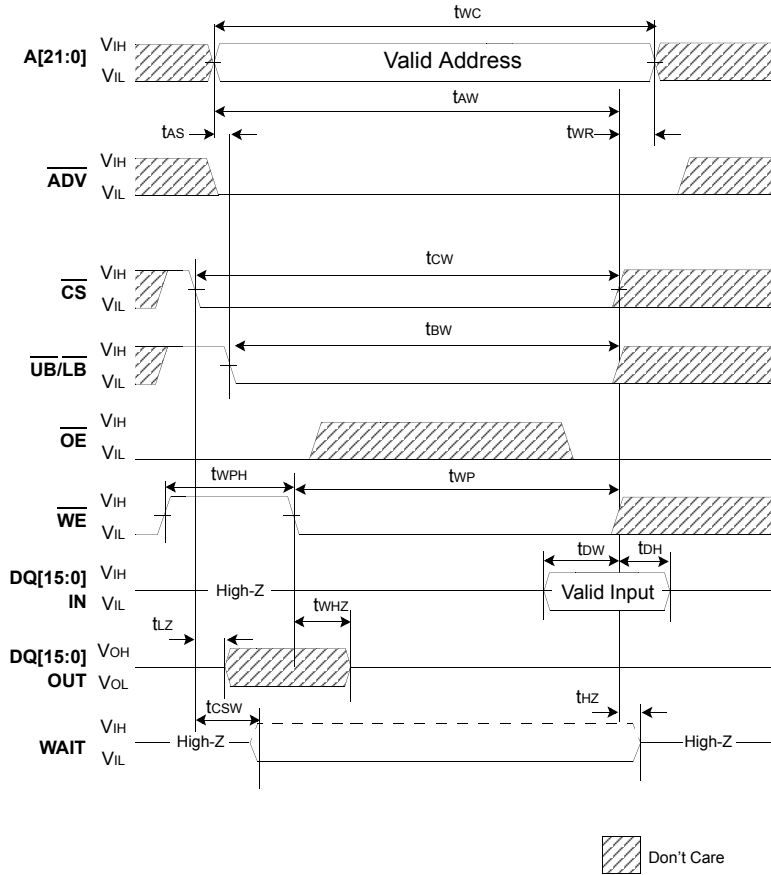


1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. A write occurs during the overlap(t<sub>WP</sub>) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high or  $\overline{WE}$  goes high or  $\overline{UB/LB}$  goes high. The t<sub>WP</sub> is measured from the beginning of write to the end of write.
3. t<sub>CW</sub> is measured from the  $\overline{CS}$  going low to the end of write.
4. t<sub>AS</sub> is measured from the address valid to the beginning of write.
5. t<sub>WR</sub> is measured from the end of write to the address change. t<sub>WR</sub> is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

**K1C6416B2D**

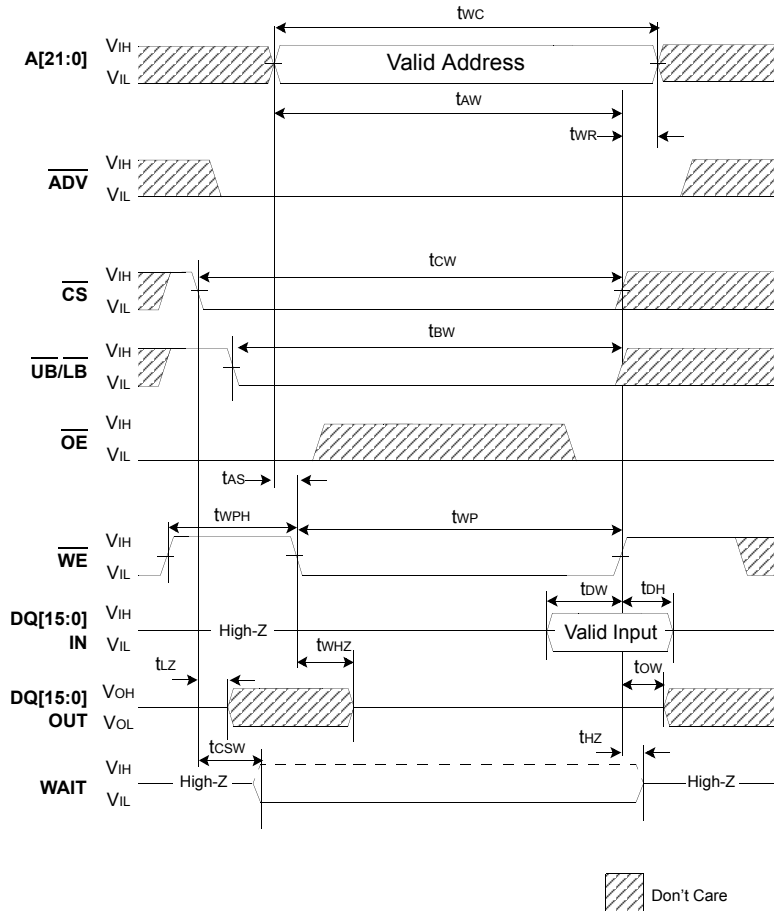
**U<sub>t</sub>RAM2**

**LB/UB-Controlled Asynchronous WRITE**  
(CRE=V<sub>IL</sub>)



1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. A write occurs during the overlap(t<sub>WP</sub>) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high or  $\overline{WE}$  goes high or  $\overline{UB}/\overline{LB}$  goes high. The t<sub>WP</sub> is measured from the beginning of write to the end of write.
3. t<sub>CW</sub> is measured from the  $\overline{CS}$  going low to the end of write.
4. t<sub>AS</sub> is measured from the address valid to the beginning of write.
5. t<sub>WR</sub> is measured from the end of write to the address change. t<sub>WR</sub> is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

**WE-Controlled Asynchronous WRITE**  
(CRE=V<sub>IL</sub>)

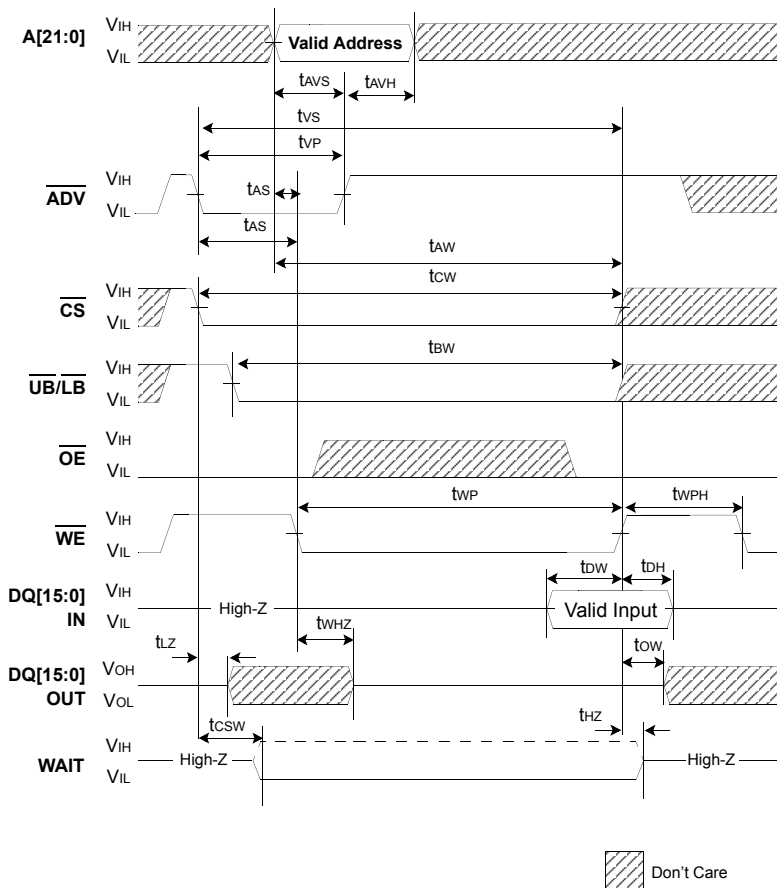


1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high or  $\overline{WE}$  goes high or  $\overline{UB/LB}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{cw}$  is measured from the  $\overline{CS}$  going low to the end of write.
4.  $t_{as}$  is measured from the address valid to the beginning of write.
5.  $t_{wr}$  is measured from the end of write to the address change.  $t_{wr}$  is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

K1C6416B2D

U<sub>t</sub>RAM2

**Asynchronous WRITE Using ADV**  
(CRE=V<sub>IL</sub>)



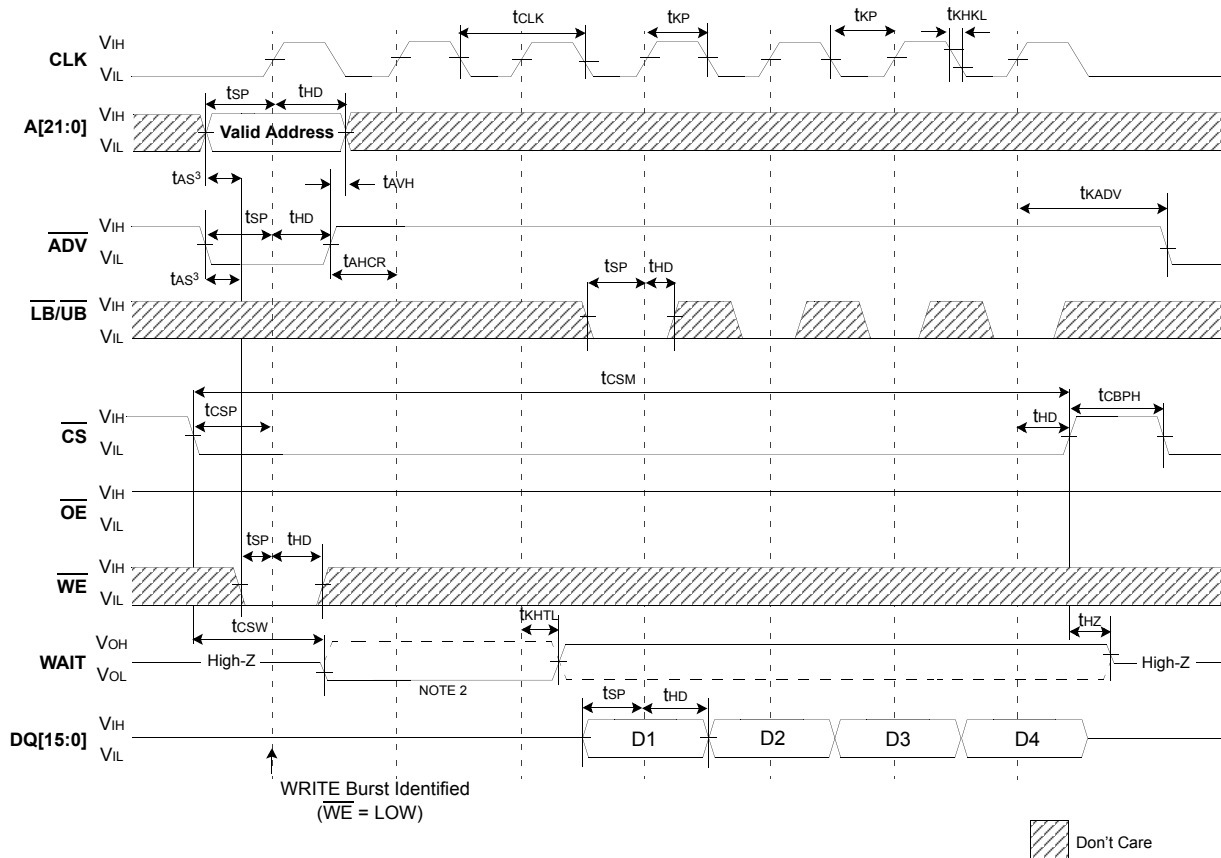
1. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
2. A write occurs during the overlap ( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high or  $\overline{WE}$  goes high or  $\overline{UB/LB}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CSW}$  is measured from the  $\overline{CS}$  going low to the beginning of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{wr}$  is measured from the end of write to the address change.  $t_{wr}$  is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

**K1C6416B2D**

**UtRAM2**

**Burst WRITE Operation—Variable Latency Mode**

(CRE=VIL)



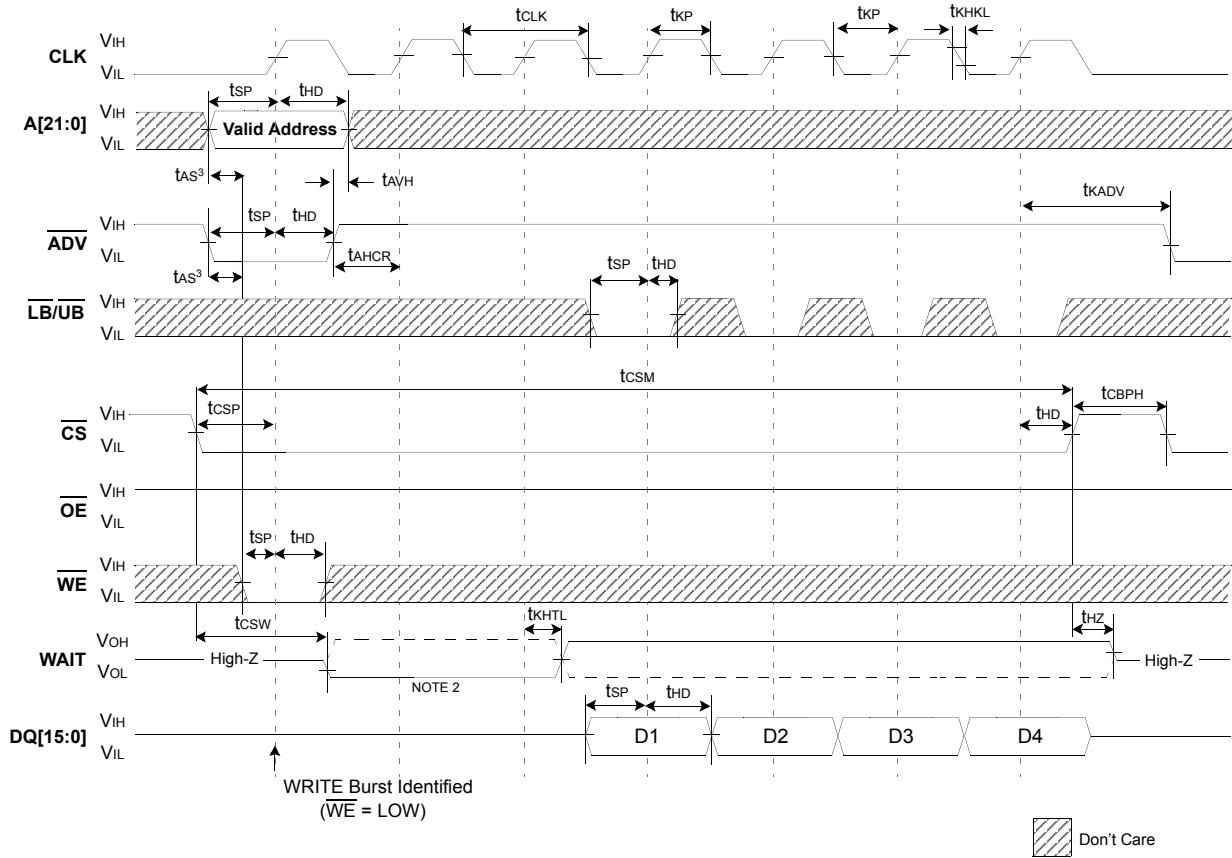
**Notes:**

1. Non-default BCR settings for burst WRITE operation in variable latency mode: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. t<sub>AS</sub> required if t<sub>CSP</sub> > 20ns.
4. Don't care must be in VIL or VIH.

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UtRAM2

**Burst WRITE Operation—Fixed Latency Mode**  
(CRE=VIL)



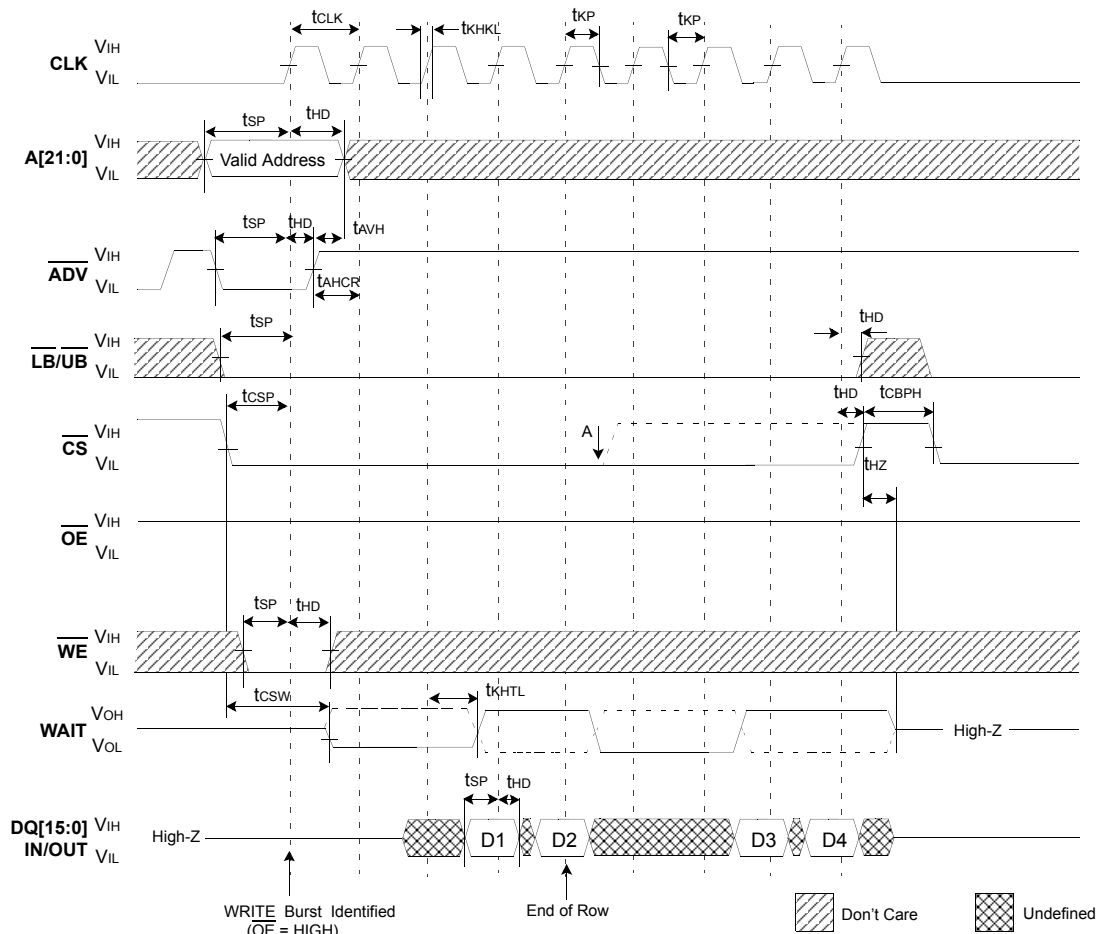
Notes:

1. Non-default BCR settings for burst WRITE operation in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. tAS required if tCSP > 20ns.
4. Don't care must be in VIL or VIH.

**K1C6416B2D**

**UtRAM2**

**4-Word Burst WRITE Operation— Row Boundary Crossing**  
(CRE=V<sub>IL</sub>)

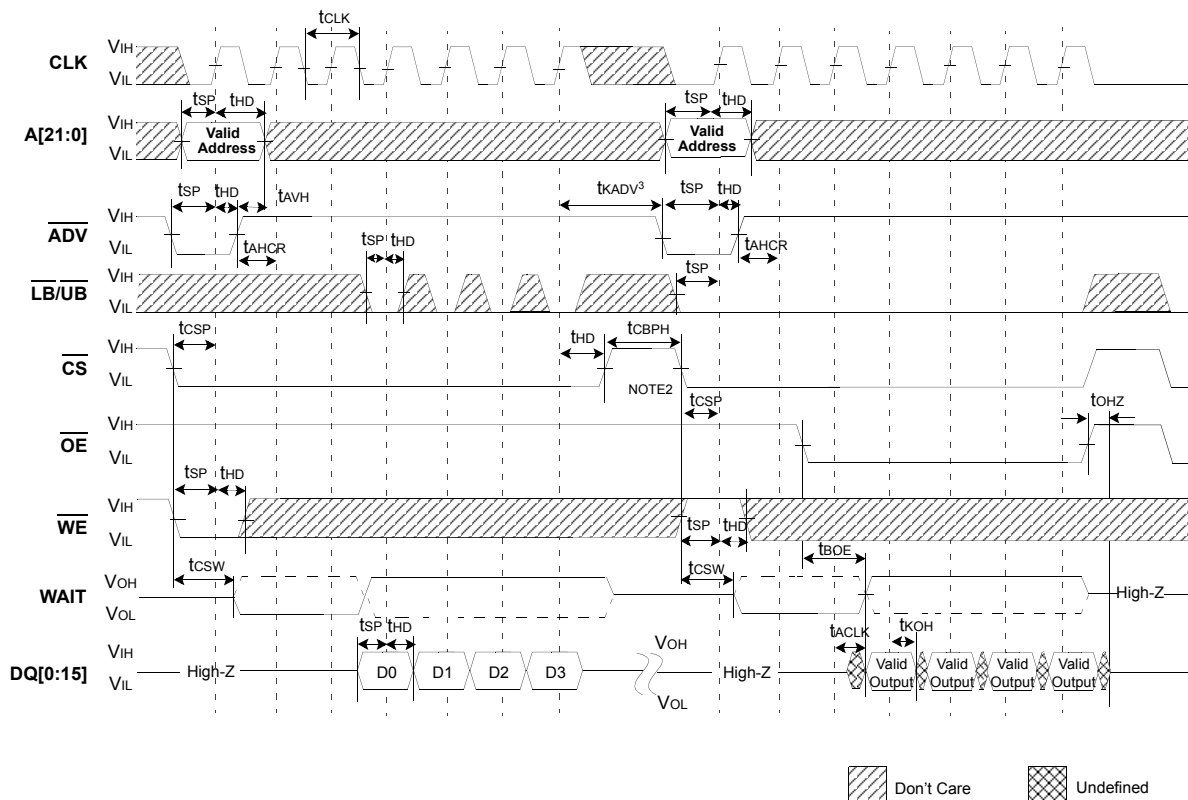


1. Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.
3. D2 can be written when CS goes high at Point A.

K1C6416B2D

U<sub>t</sub>RAM2

**Burst WRITE Followed by Burst READ**  
(CRE=V<sub>IL</sub>)



Notes:

1. Non-default BCR settings for burst WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A refresh opportunity must be provided every  $t_{CSM}$ . A refresh opportunity is satisfied by either of the following two conditions: a) clocked  $\overline{CS}$  HIGH, or b)  $\overline{CS}$  HIGH for longer than 15ns.  $\overline{CS}$  can stay LOW between burst READ and burst WRITE operations, but  $\overline{CS}$  must not remain LOW longer than  $t_{CSM}$ . See burst interrupt diagrams for cases where  $\overline{CS}$  stays LOW between bursts.
3. Only fixed latency requires  $t_{KADV}$ .
4. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

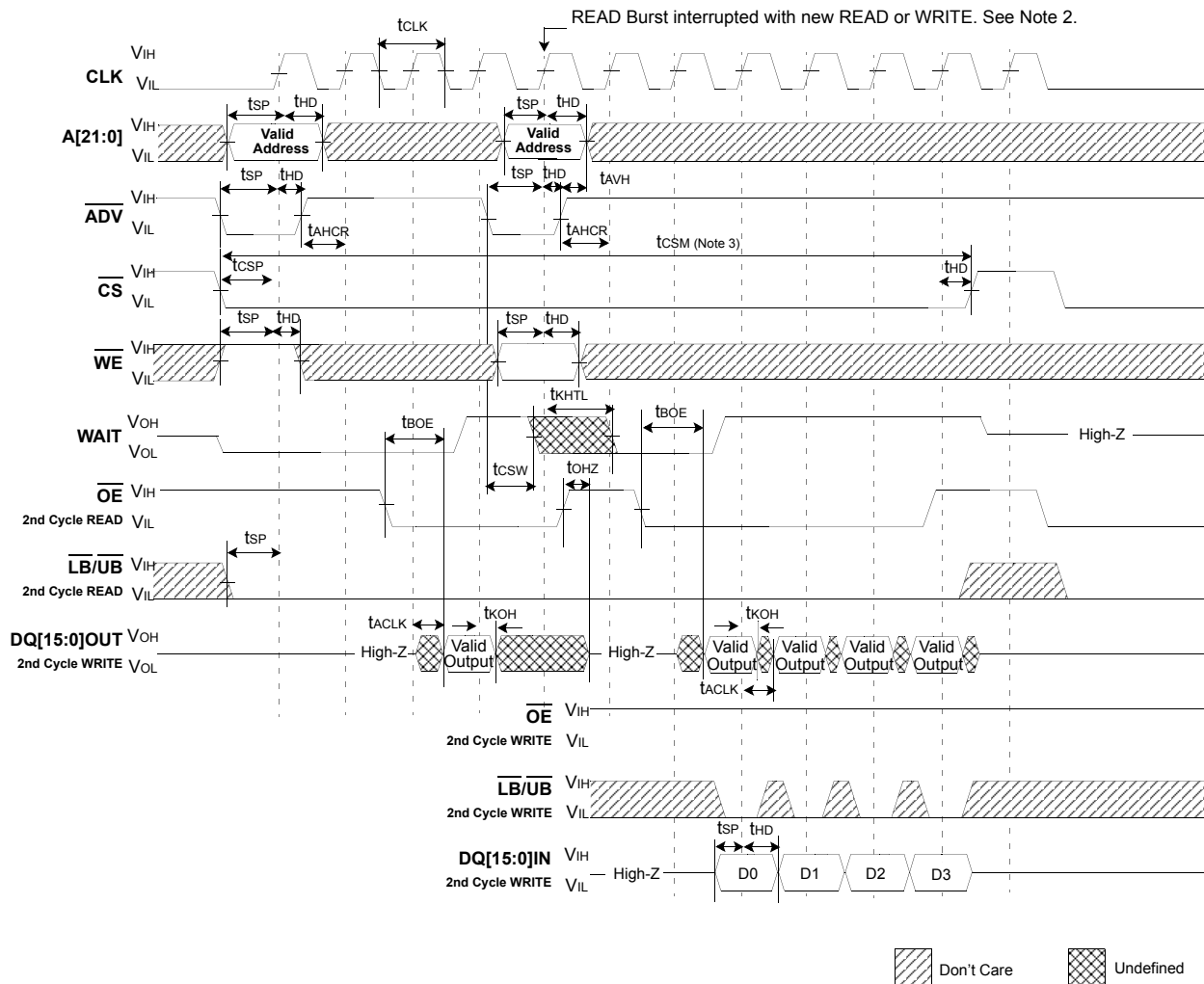


K1C6416B2D

UtRAM2

Burst READ Interrupted by Burst READ or WRITE

(CRE=V<sub>IL</sub>)

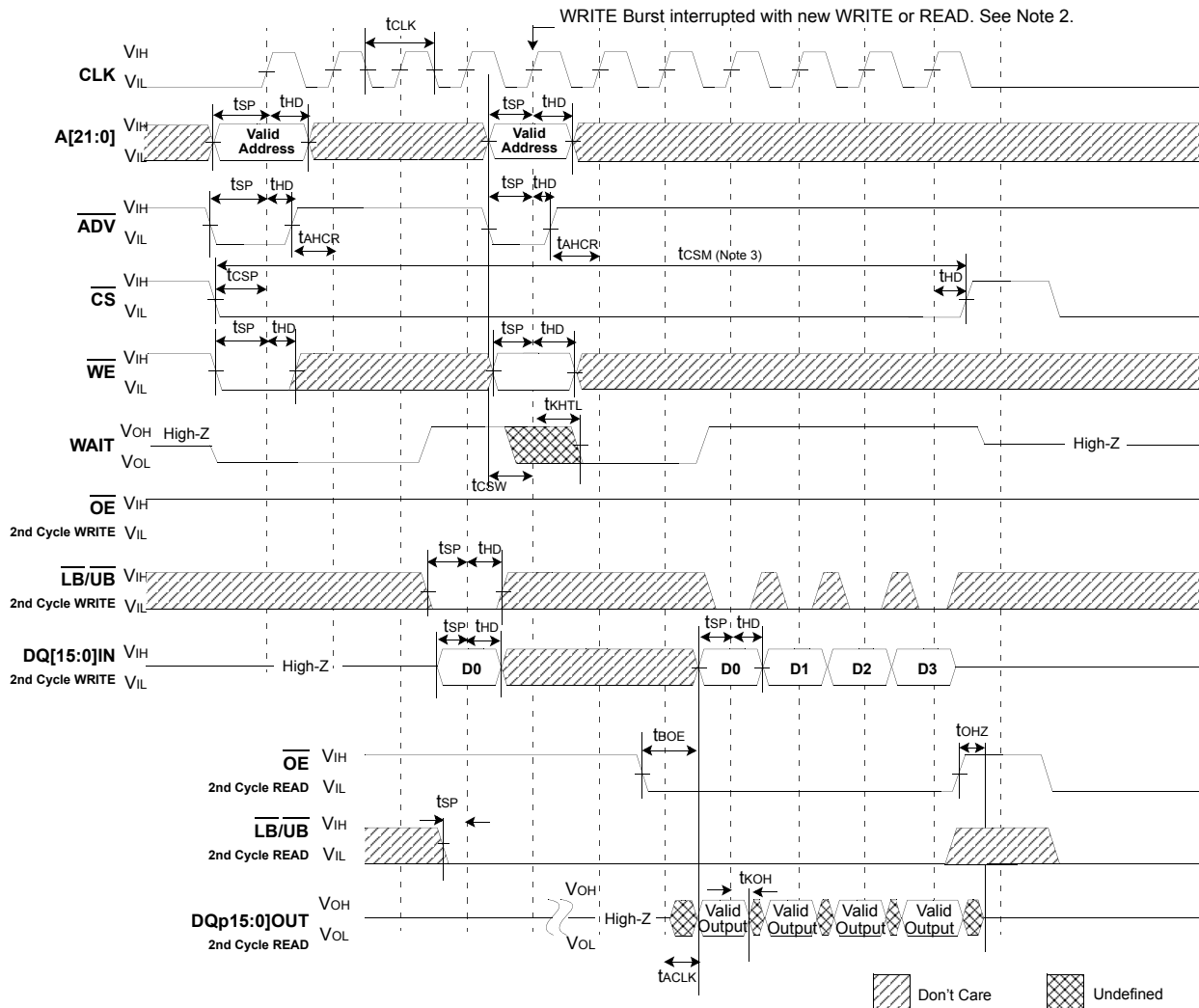


Notes:

1. Non-default BCR settings for burst READ interrupted by burst READ or WRITE: Fixed or variable latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.
2. Burst interrupt shown on first allowable clock (i.e., after the first data received by the controller).
3. CS can stay LOW between burst operations, but CS must not remain LOW longer than tCSCM.
4. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

**Burst WRITE Interrupted by Burst WRITE or READ—Variable Latency Mode**

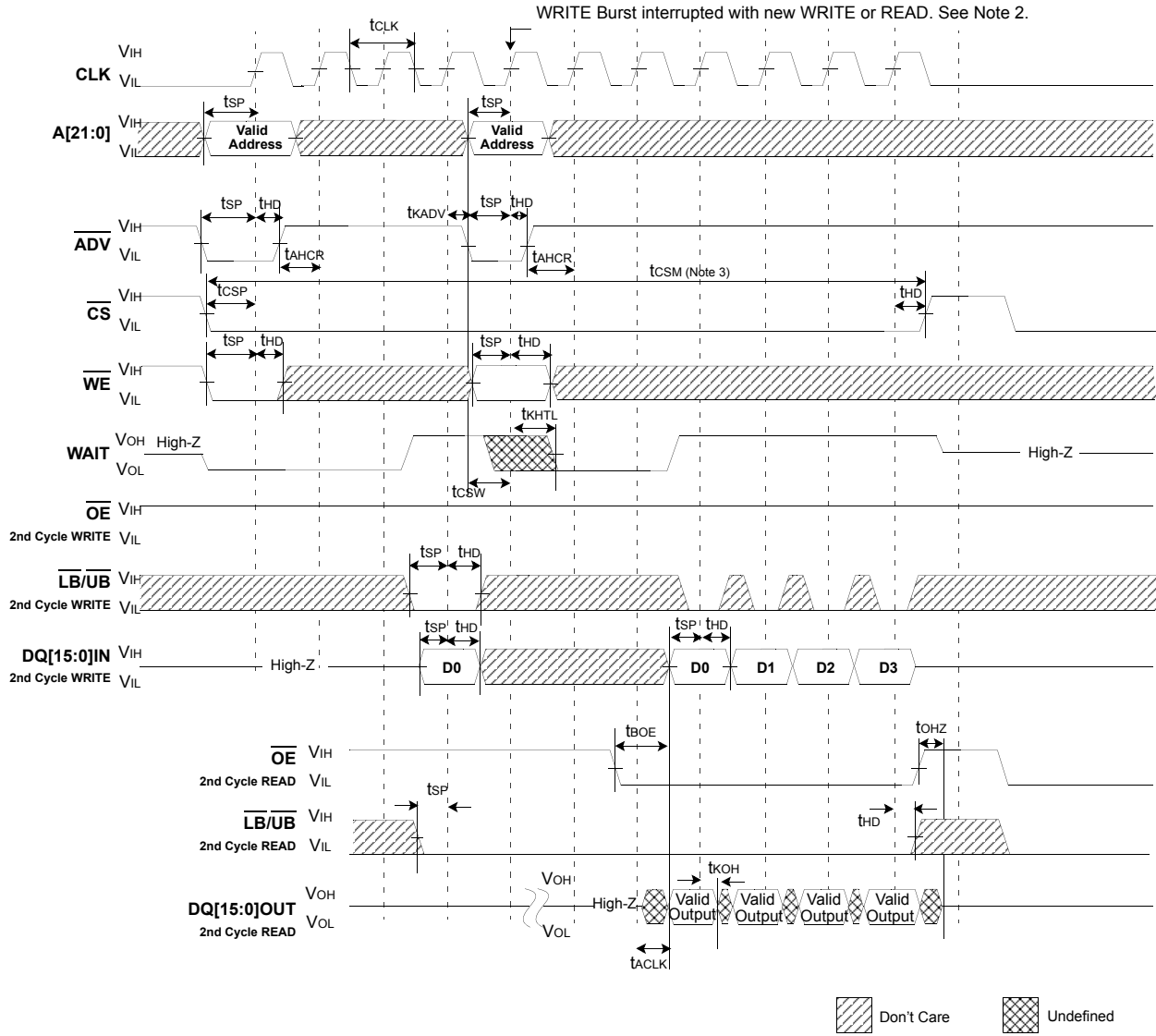
(CRE=VIL)



Notes:

1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in variable latency mode: Variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
3. CS can stay LOW between burst operations, but CS must not remain LOW longer than tCSM.
4. Don't care must be in VIL or VIH.

**Burst WRITE Interrupted by Burst WRITE or READ—Fixed Latency Mode**  
(CRE=V<sub>IL</sub>)



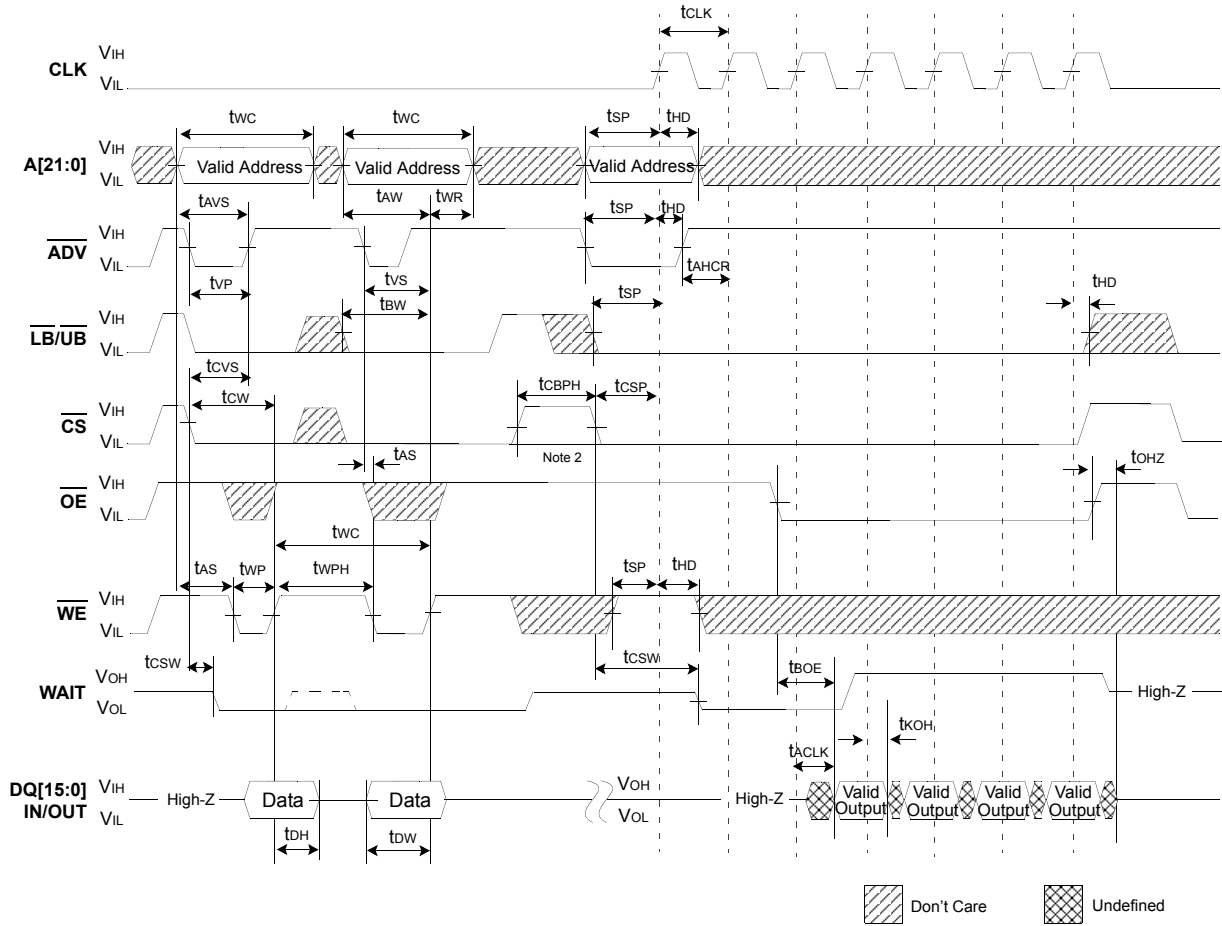
**Notes:**

1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Burst interrupt shown on first allowable clock (i.e., after first data word written).
3. CS can stay LOW between burst operations, but CS must not remain LOW longer than t<sub>CSM</sub>.
4. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

K1C6416B2D

U<sub>t</sub>RAM2

Asynchronous WRITE Followed by Burst READ  
(CRE=V<sub>IL</sub>)



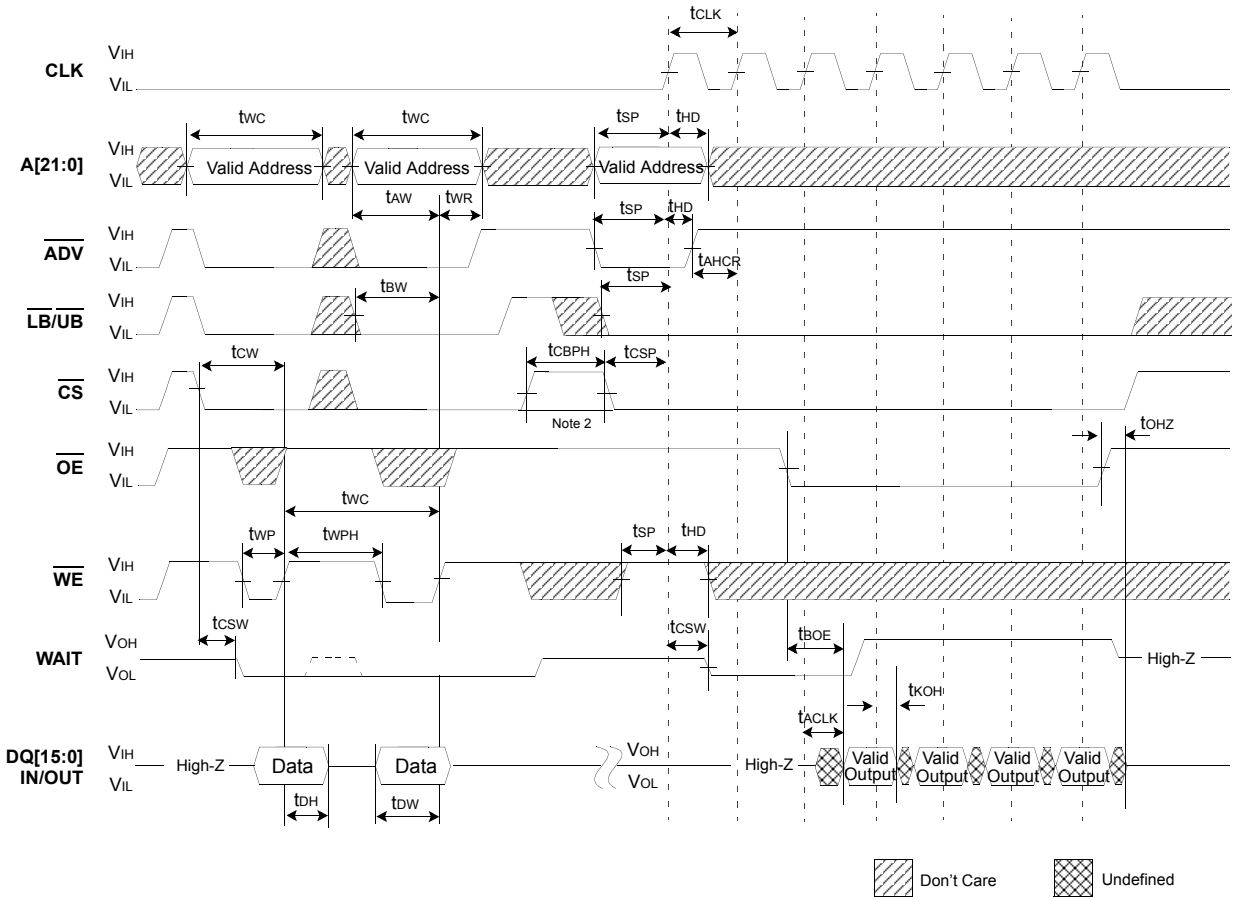
Notes:

1. Non-default BCR settings for asynchronous WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations,  $\overline{CS}$  must go HIGH.  $\overline{CS}$  can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every  $t_{CSM}$ . A refresh opportunity is satisfied by either of the following two conditions: a) clocked  $\overline{CS}$  HIGH, or b)  $\overline{CS}$  HIGH for longer than 15ns.
3. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

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U<sub>t</sub>RAM2

Asynchronous WRITE (ADV LOW) Followed By Burst READ  
(CRE=V<sub>IL</sub>)



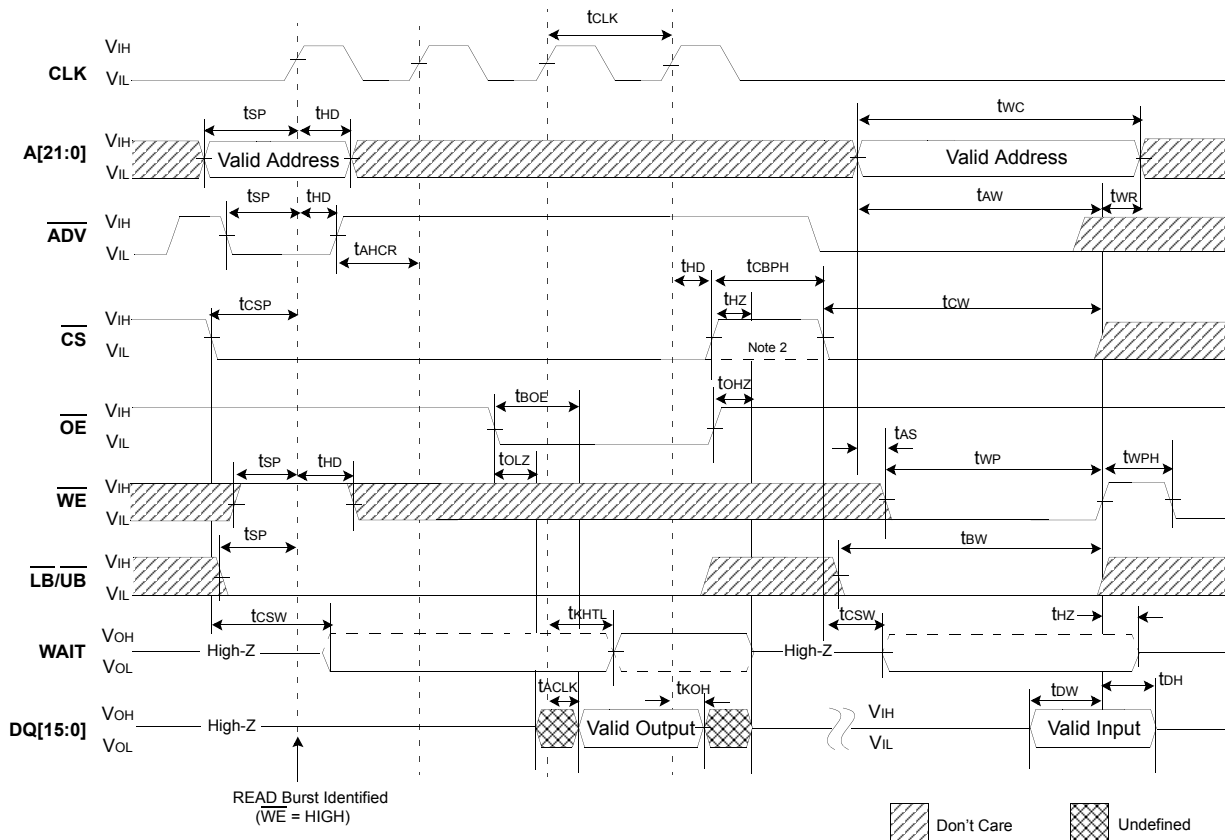
Notes:

1. Non-default BCR settings for asynchronous WRITE, with  $\overline{ADV}$  LOW, followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations,  $\overline{CS}$  must go HIGH.  $\overline{CS}$  can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every  $t_{CSM}$ . A refresh opportunity is satisfied by either of the following two conditions: a) clocked CS HIGH, or b) CS HIGH for longer than 15ns.
3. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

K1C6416B2D

U<sub>t</sub>RAM2

**Burst READ Followed by Asynchronous WRITE (WE-Controlled)**  
(CRE=V<sub>IL</sub>)



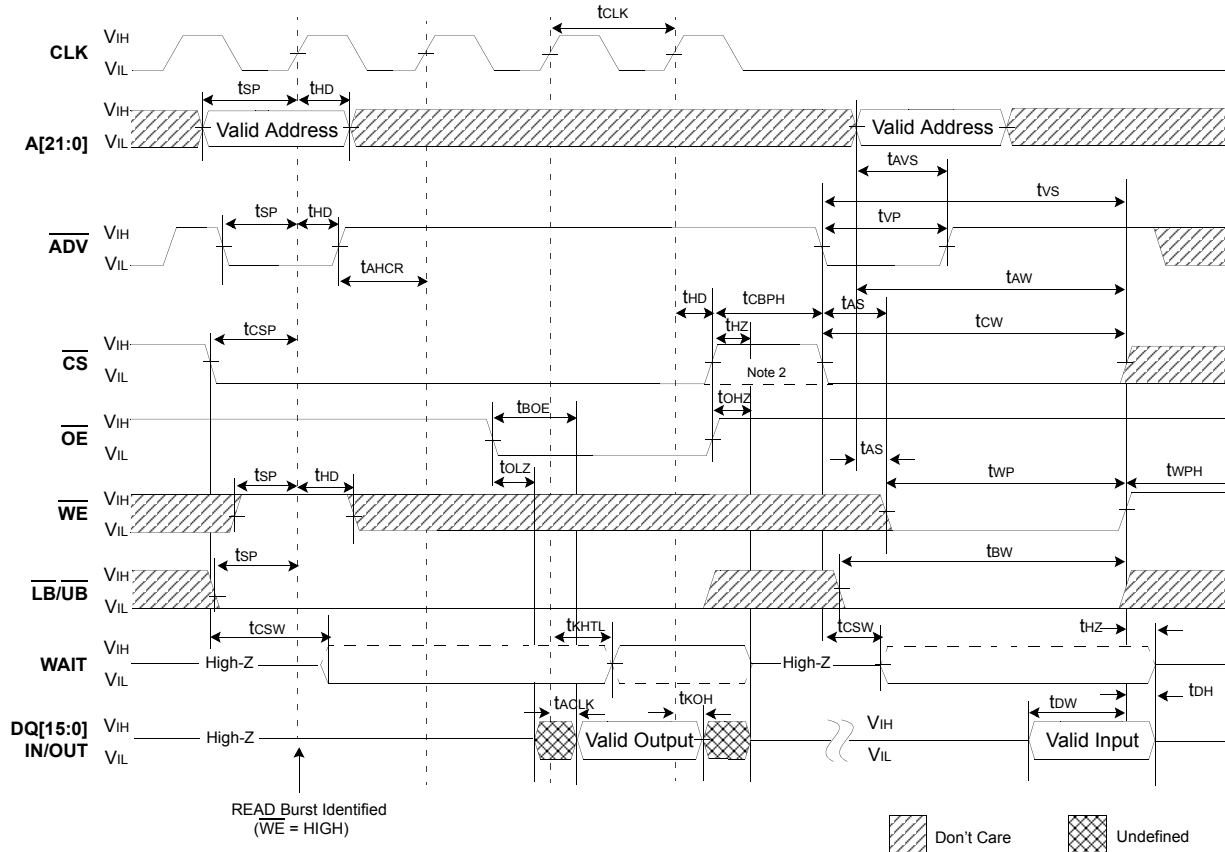
Notes:

1. Non-default BCR settings for burst READ followed by asynchronous  $\overline{WE}$ -controlled WRITE: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations,  $\overline{CS}$  must go HIGH.  $\overline{CS}$  can stay LOW when transitioning from fixed-latency burst READs; asynchronous operation begins at the falling edge of  $\overline{ADV}$ . A refresh opportunity must be provided every t<sub>CSM</sub>. A refresh opportunity is satisfied by either of the following two conditions: a) clocked  $\overline{CS}$  HIGH, or b)  $\overline{CS}$  HIGH for longer than 15ns.
3. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

K1C6416B2D

U<sub>t</sub>RAM2

**Burst READ Followed by Asynchronous WRITE Using ADV**  
(CRE=V<sub>IL</sub>)



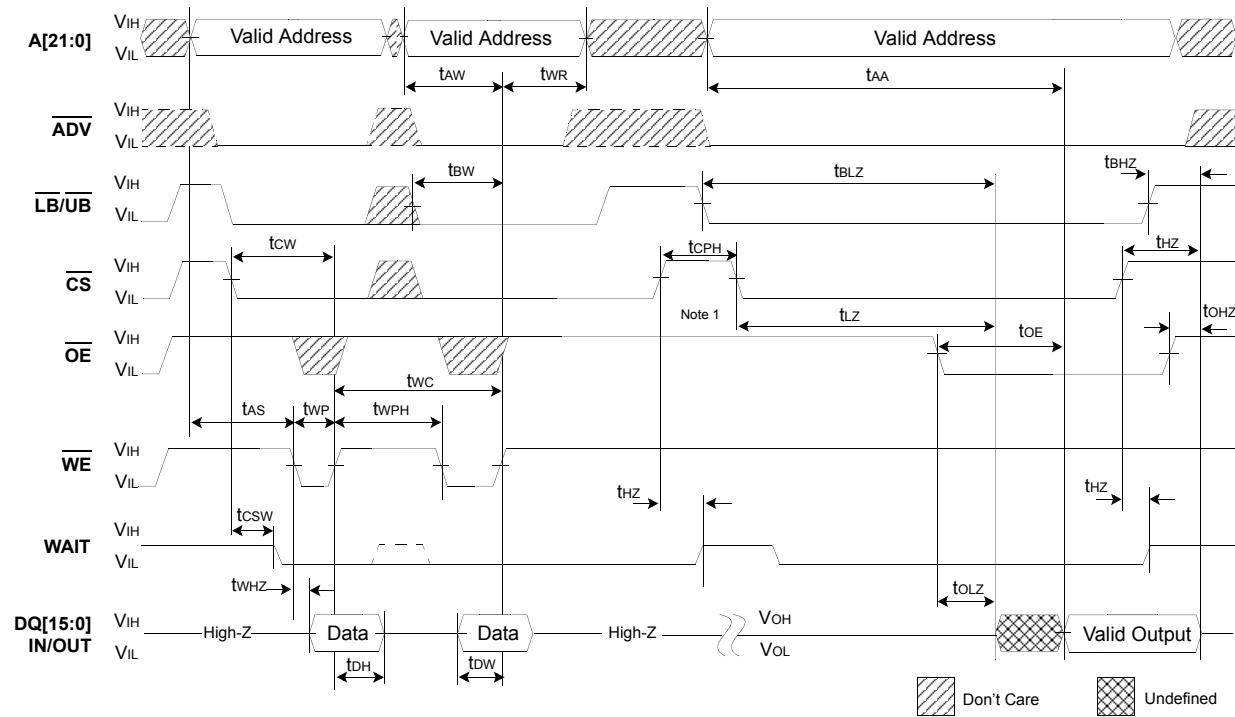
Notes:

1. Non-default BCR settings for burst READ followed by asynchronous WRITE using  $\overline{ADV}$ : Fixed or variable latency; latency code two (three clocks);  $\overline{WAIT}$  active LOW;  $\overline{WAIT}$  asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations,  $\overline{CS}$  must go HIGH.  $\overline{CS}$  can stay LOW when transitioning from fixed-latency burst READs; asynchronous operation begins at the falling edge of  $\overline{ADV}$ . A refresh opportunity must be provided every  $t_{CSM}$ . A refresh opportunity is satisfied by either of the following two conditions: a) clocked  $\overline{CS}$  HIGH, or b)  $\overline{CS}$  HIGH for longer than 15ns.
3. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

**K1C6416B2D**

**U<sub>t</sub>RAM2**

**Asynchronous WRITE Followed by Asynchronous READ—ADV LOW**  
(CRE=V<sub>IL</sub>)



Notes:

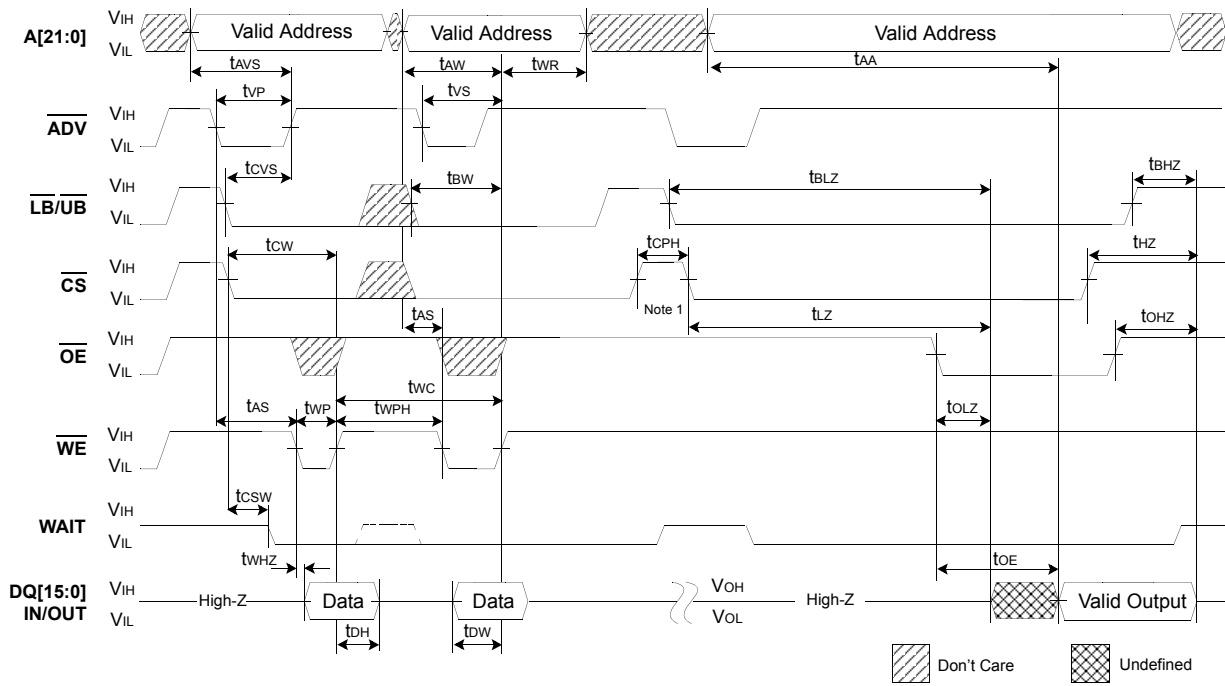
1. When configured for synchronous mode ( $\overline{BCR}[15] = 0$ ),  $\overline{CS}$  must remain HIGH for at least 5ns ( $t_{CPH}$ ) to schedule the appropriate refresh interval. Otherwise,  $t_{CPH}$  is only required after CS-controlled WRITES.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.



**K1C6416B2D**

**U<sub>t</sub>RAM2**

**Asynchronous WRITE Followed by Asynchronous READ**  
(CRE=V<sub>IL</sub>)



Notes:

1. When configured for synchronous mode ( $\overline{\text{BCR}}[15] = 0$ ),  $\overline{\text{CS}}$  must remain HIGH for at least 5ns ( $t_{\text{CPH}}$ ) to schedule the appropriate refresh interval. Otherwise,  $t_{\text{CPH}}$  is only required after  $\overline{\text{CS}}$ -controlled WRITES.
2. Don't care must be in V<sub>IL</sub> or V<sub>IH</sub>.

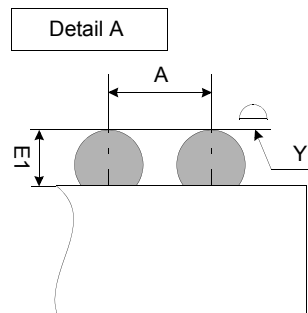
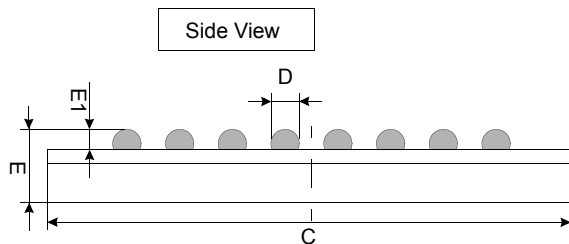
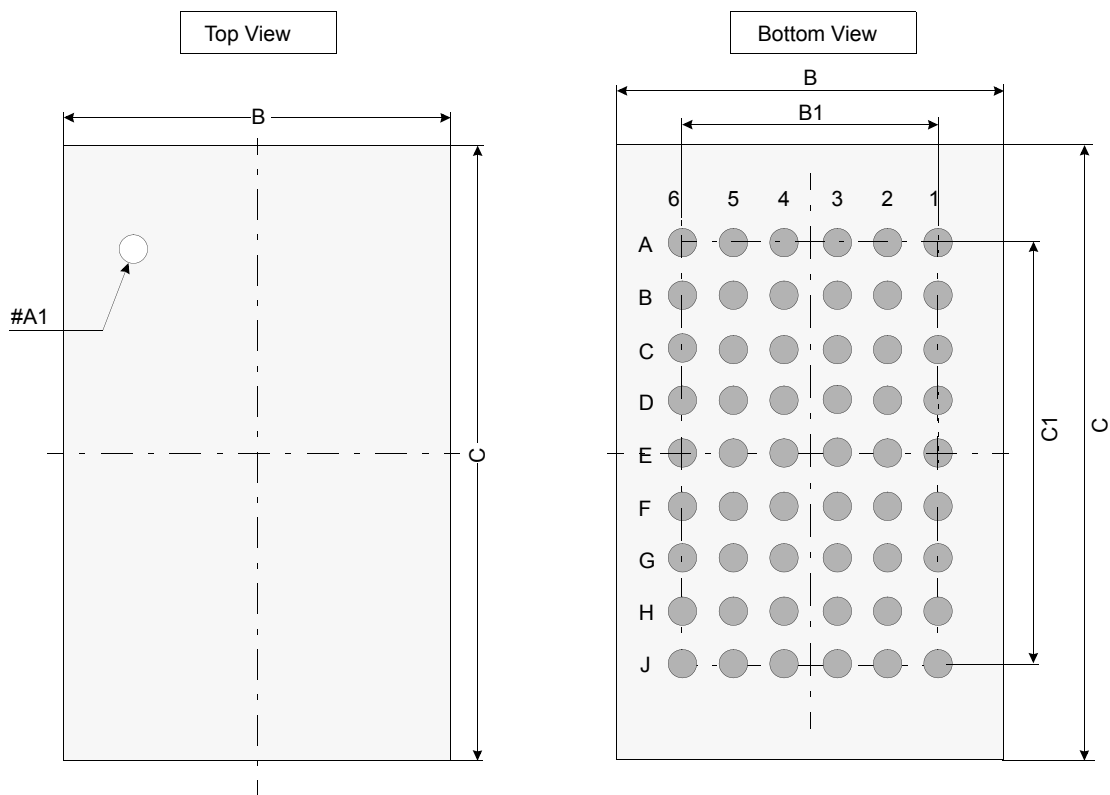
# K1C6416B2D

# U<sub>t</sub>RAM2

## PACKAGE DIMENSION

54 BALL FINE PITCH BGA(0.75mm ball pitch)

Unit: millimeters



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	6.00	-
D	0.40	0.45	0.50
E	-	-	1.00
E1	0.25	-	-
Y	-	-	0.10

### Notes.

1. Ball counts: 54(9 row x 6 column)
2. Ball pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are  $\pm 0.050$  unless specified beside figure.
4. Typ: Typical
5. Y is coplanarity