

*16M x 4bit CMOS Dynamic RAM with Extended Data Out*

**DESCRIPTION**

This is a family of 16,777,216 x 4 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), package type (SOJ or TSOP-II) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. This 16Mx4 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

**FEATURES**

• **Part Identification**

- K4E660411B-JC(5.0V, 8K Ref., SOJ)
- K4E640411B-JC(5.0V, 4K Ref., SOJ)
- K4E660411B-TC(5.0V, 8K Ref., TSOP)
- K4E640411B-TC(5.0V, 4K Ref., TSOP)

• **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	550	715
-50	495	660
-60	440	605

• **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time
		Normal
K4E660411B*	8K	64ms
K4E640411B	4K	

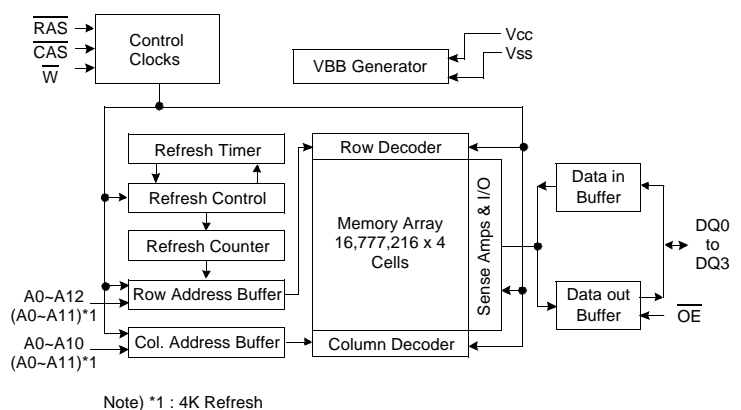
\* Access mode &  $\overline{\text{RAS}}$  only refresh mode : 8K cycle/64ms  
 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  & Hidden refresh mode : 4K cycle/64ms

• **Performance Range**

Speed	t <sub>TRAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>HPC</sub>
-45	45ns	12ns	74ns	17ns
-50	50ns	13ns	84ns	20ns
-60	60ns	15ns	104ns	25ns

- Extended Data Out Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5.0V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5.0V±10% power supply

**FUNCTIONAL BLOCK DIAGRAM**



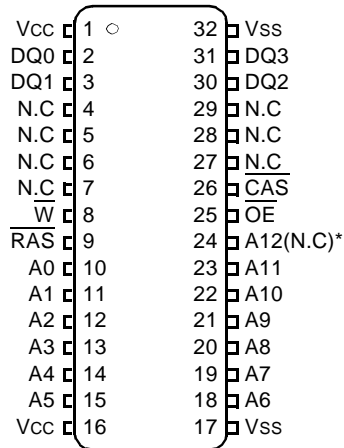
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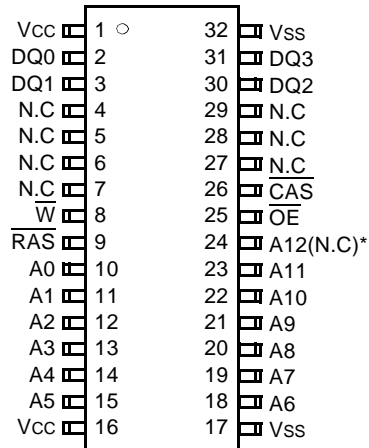
PIN CONFIGURATION (Top Views)

- K4E660411B-J
- K4E640411B-J

- K4E660411B-T
- K4E640411B-T



(J : 400mil SOJ)



(T : 400mil TSOP(II))

\* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	VIN,VOUT	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	1	W
Short Circuit Output Current	Ios Address	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, TA= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1.0*1	V
Input Low Voltage	VIL	-1.0*2	-	0.8	V

\*1 : Vcc+2.0V at pulse width≤20ns which is measured at Vcc

\*2 : -2.0 at pulse width≤20ns which is measured at Vss

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$ , all other pins not under test=0 Volt)	II(L)	-5	5	uA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$ )	Io(L)	-5	5	uA
Output High Voltage Level(IoH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level(IoL=4.2mA)	VOL	-	0.4	V



**DC AND OPERATING CHARACTERISTICS** (Continued)

Symbol	Power	Speed	Max		Units
			K4E660411B	K4E640411B	
I <sub>CC1</sub>	Don't care	-45	100	130	mA
		-50	90	120	mA
		-60	80	110	mA
I <sub>CC2</sub>	Normal	Don't care	2	2	mA
I <sub>CC3</sub>	Don't care	-45	100	130	mA
		-50	90	120	mA
		-60	80	110	mA
I <sub>CC4</sub>	Don't care	-45	110	120	mA
		-50	100	110	mA
		-60	90	100	mA
I <sub>CC5</sub>	Normal	Don't care	1	1	mA
I <sub>CC6</sub>	Don't care	-45	100	130	mA
		-50	90	120	mA
		-60	80	110	mA

I<sub>CC1</sub>\* : Operating Current ( $\overline{RAS}$  and  $\overline{CAS}$ , Address cycling @trc=min.)

I<sub>CC2</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub>\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$ , Address cycling @trc=min.)

I<sub>CC4</sub>\* : Extended Data Out Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$ , Address cycling @tHPC=min.)

I<sub>CC5</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub>\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min)

**\*Note** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub>, I<sub>CC3</sub> and I<sub>CC6</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one EDO mode cycle time, tHPC.



**K4E660411B, K4E640411B****CMOS DRAM****CAPACITANCE** ( $T_A=25^\circ\text{C}$ ,  $V_{CC}=5.0\text{V}$ ,  $f=1\text{MHz}$ )

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	CIN1	-	5	pF
Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{W}}$ , $\overline{\text{OE}}$ ]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ3]	CDQ	-	7	pF

**AC CHARACTERISTICS** ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , See note 1,2)Test condition :  $V_{CC}=5.0\text{V} \pm 10\%$ ,  $V_{ih}/V_{il}=2.4/0.8\text{V}$ ,  $V_{oh}/V_{ol}=2.0/0.8\text{V}$ 

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	74		84		104		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	101		116		138		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		12		13		15	ns	3,4,5
Access time from column address	t <sub>AA</sub>		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t <sub>CLZ</sub>	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	t <sub>CEZ</sub>	3	13	3	13	3	13	ns	6,14
$\overline{\text{OE}}$ to output in Low-Z	t <sub>OLZ</sub>	3		3		3		ns	3
Transition time (rise and fall)	t <sub>T</sub>	1	50	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	25		30		40		ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	8		13		15		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	35		38		45		ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	7	5K	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCD</sub>	11	33	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	9	22	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	5		5		5		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		ns	
Row address hold time	t <sub>RAH</sub>	7		10		10		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	7		8		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	23		25		30		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0		0		0		ns	
Write command hold time	t <sub>WCH</sub>	7		10		10		ns	
Write command pulse width	t <sub>WP</sub>	6		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t <sub>RWL</sub>	8		13		10		ns	
Write command to $\overline{\text{CAS}}$ lead time	t <sub>CWL</sub>	7		8		10		ns	
Data set-up time	t <sub>DS</sub>	0		0		0		ns	9



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## AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Data hold time	tdH	7		8		10		ns	9
Refresh period (4K, Normal)	tREF		64		64		64	ms	
Refresh period (8K, Normal)	tREF		64		64		64	ms	
Write command set-up time	twCS	0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	24		30		32		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	57		67		77		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	35		42		47		ns	7
$\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		24		28		35	ns	3
Hyper Page cycle time	tHPC	17		20		25		ns	13
Hyper Page read-modify-write cycle time	tHPRWC	47		47		56		ns	13
$\overline{\text{CAS}}$ precharge time (Hyper page cycle)	tCP	6.5		8		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	trASP	45	200K	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	24		30		35		ns	
$\overline{\text{OE}}$ access time	toEA		12		13		15	ns	
$\overline{\text{OE}}$ to data delay	toED	8		13		13		ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tcpWD	36		45		54		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	3	11	3	13	3	13	ns	6
$\overline{\text{OE}}$ command hold time	toEH	5		13		15		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	11
Write command hold time (Test mode in)	twTH	10		10		10		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	twRP	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	twRH	10		10		10		ns	
Output data hold time	tdOH	4		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	treZ	3	13	3	13	3	13	ns	6,14
Output buffer turn off delay from $\overline{\text{W}}$	twEZ	3	13	3	13	3	13	ns	6
$\overline{\text{W}}$ to data delay	twED	8		15		15		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	toCH	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	toEP	5		5		5		ns	
$\overline{\text{W}}$ pulse width (Hyper page Cycle)	twPE	5		5		5		ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	trASS	100		100		100		us	15,16,17
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	trPS	74		90		110		ns	15,16,17
$\overline{\text{CAS}}$ hold time ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	15,16,17

## TEST MODE CYCLE

( Note 11 )

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	79		89		109		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	110		121		145		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		50		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		17		18		20	ns	3,4,5,12
Access time from column address	t <sub>AA</sub>		28		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	50	10K	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	12	10K	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	18		18		20		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	39		43		50		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	28		30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	29		35		39		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	62		72		84		ns	7
Column Address to $\overline{\text{W}}$ delay time	t <sub>AWD</sub>	40		47		54		ns	7
Hyper Page cycle time	t <sub>HPC</sub>	22		25		30		ns	13
Hyper Page read-modify-write cycle time	t <sub>HPRWC</sub>	52		53		61		ns	13
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	t <sub>RASP</sub>	50	200K	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>		29		33		40	ns	3
$\overline{\text{OE}}$ access time	t <sub>OE A</sub>		17		18		20	ns	
$\overline{\text{OE}}$ to data delay	t <sub>OE D</sub>	13		18		20		ns	
$\overline{\text{OE}}$ command hold time	t <sub>OE H</sub>	13		18		20		ns	



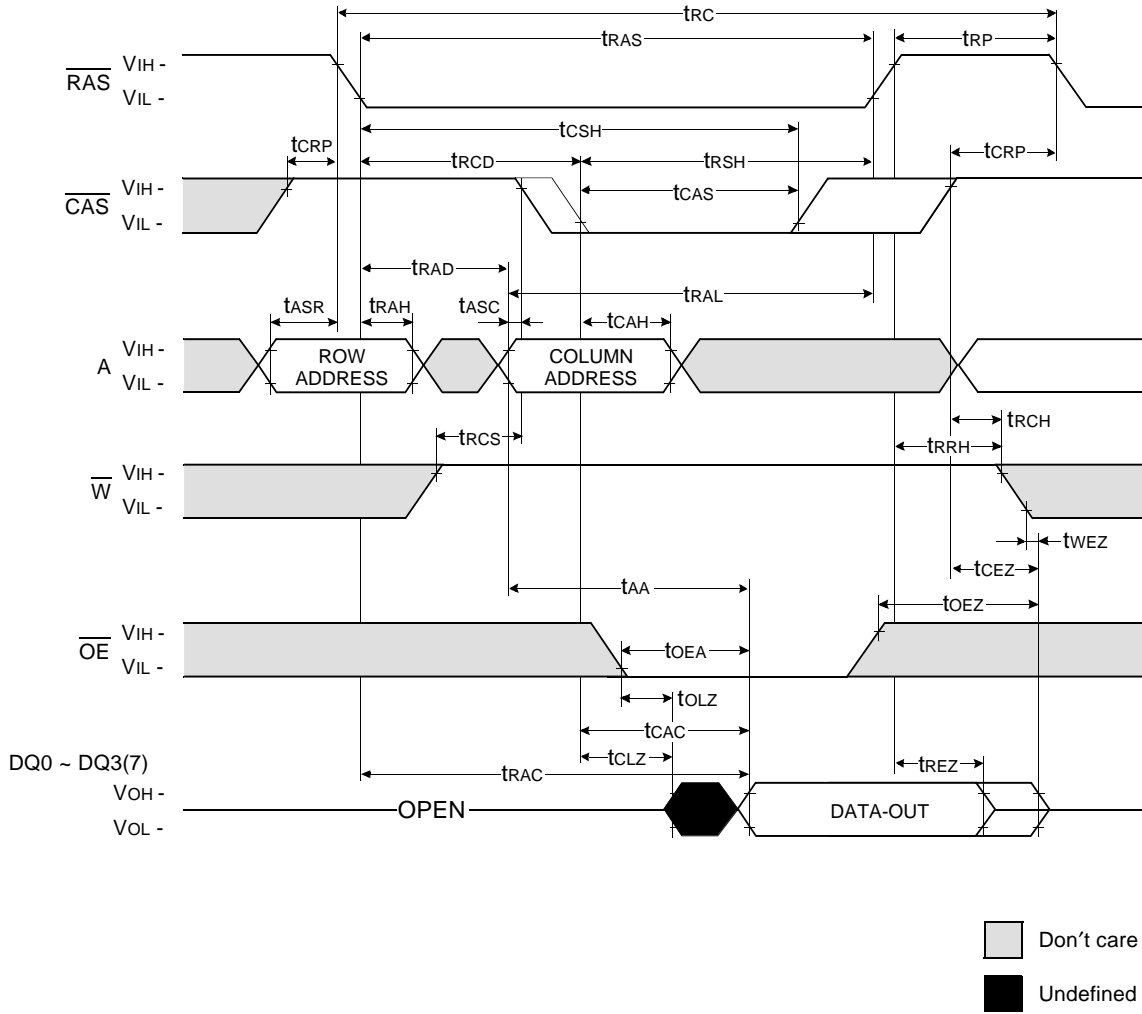
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## NOTES

1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL load and 100pF.
4. Operation within the  $t_{\text{RC}}(\text{max})$  limit insures that  $t_{\text{AC}}(\text{max})$  can be met.  $t_{\text{RC}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RC}}$  is greater than the specified  $t_{\text{RC}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. Assumes that  $t_{\text{RC}} \geq t_{\text{RC}}(\text{max})$ .
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$  and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
9. These parameters are referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{W}}$  falling edge in  $\overline{\text{OE}}$  controlled write cycle and read-modify-write cycles.
10. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{AC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of  $t_{\text{AC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13.  $t_{\text{ASC}} \geq 6\text{ns}$ , Assume  $t_{\text{T}} = 2.0\text{ns}$
14. If  $\overline{\text{RAS}}$  goes high before  $\overline{\text{CAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{CAS}}$  high going. If  $\overline{\text{CAS}}$  goes high before  $\overline{\text{RAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{RAS}}$  high going.
15. If  $t_{\text{RASS}} \geq 100\mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time must use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .
16. For  $\overline{\text{RAS}}$ -only refresh and burst  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh mode, 4096(4K/8K) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
17. For distributed  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  with 15.6us interval  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

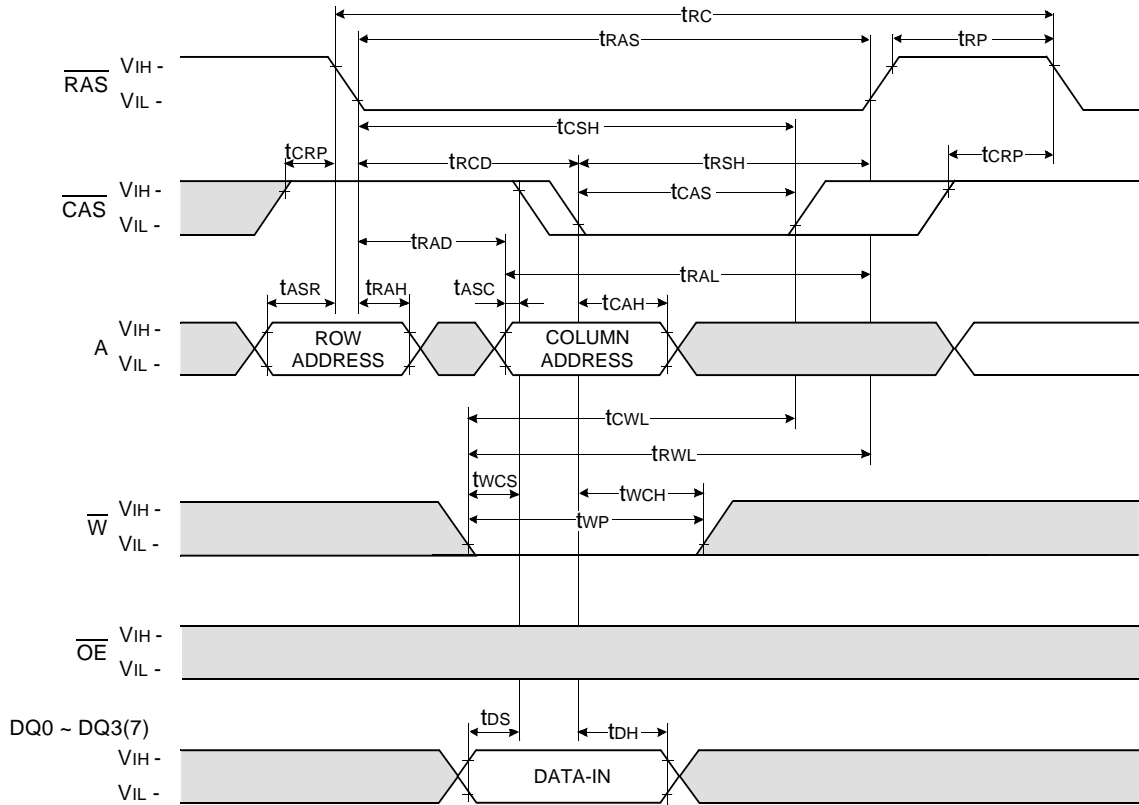


READ CYCLE



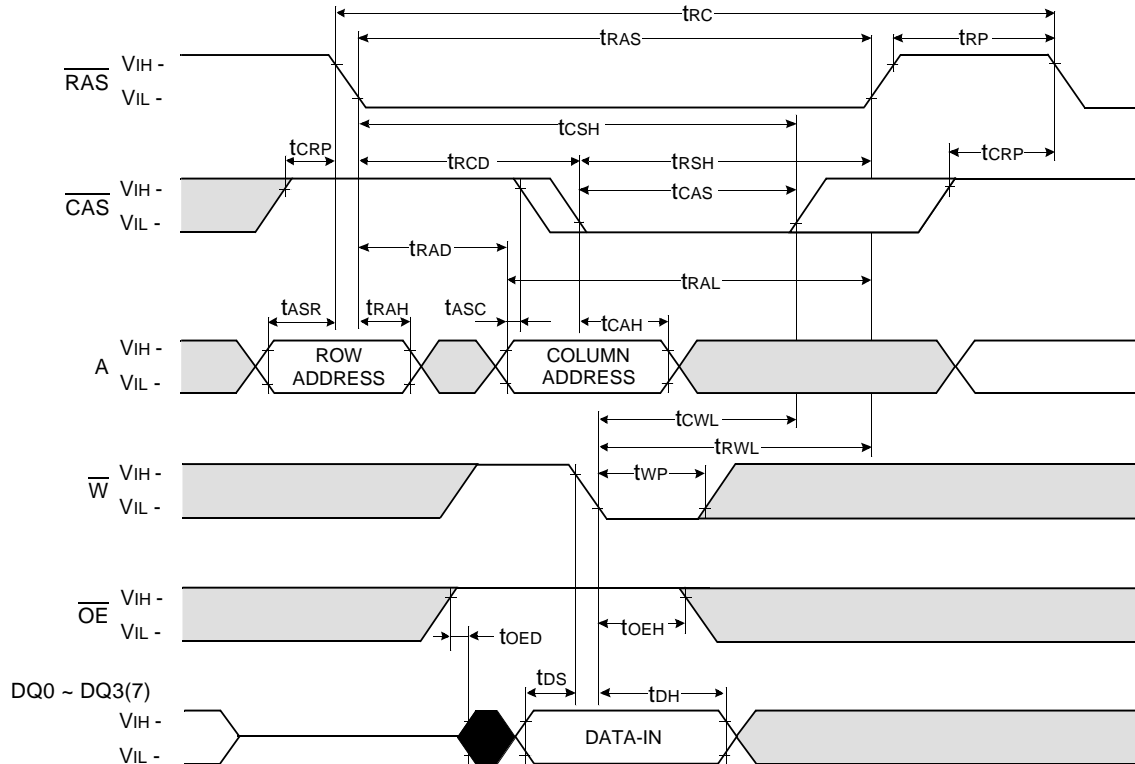
WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



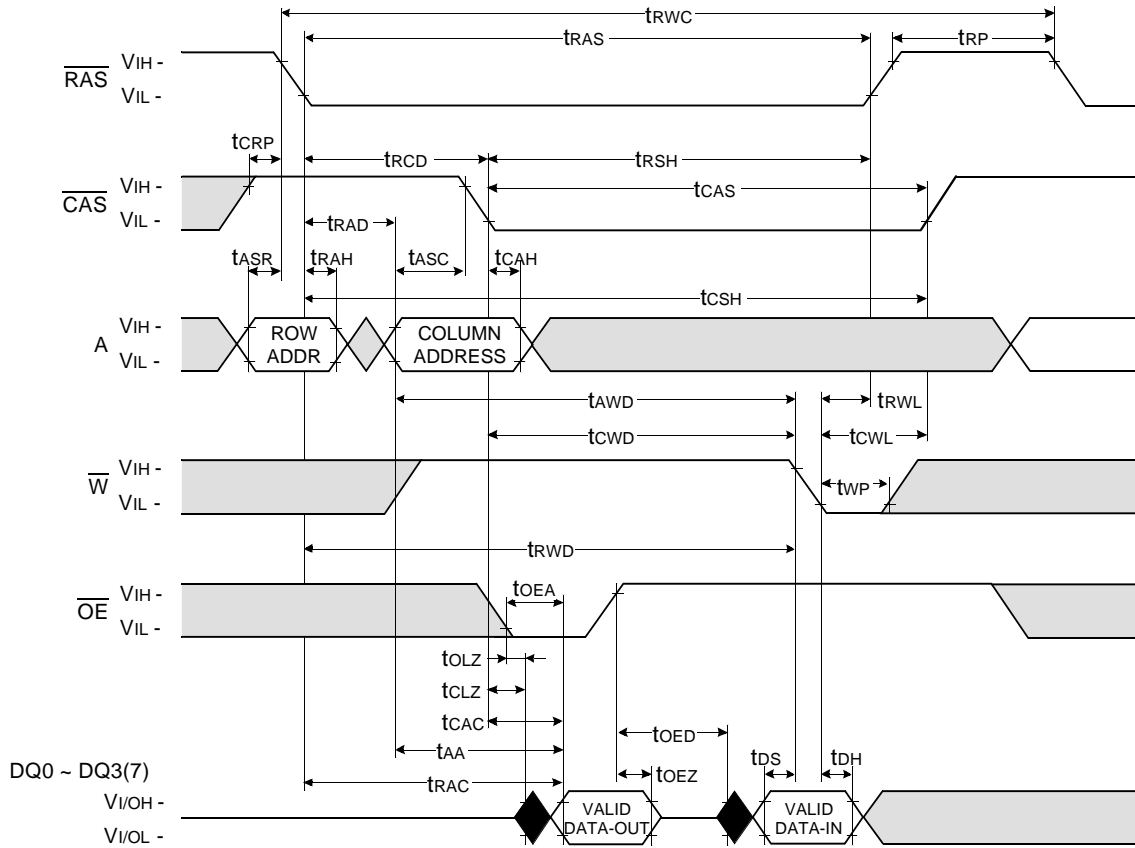
WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN



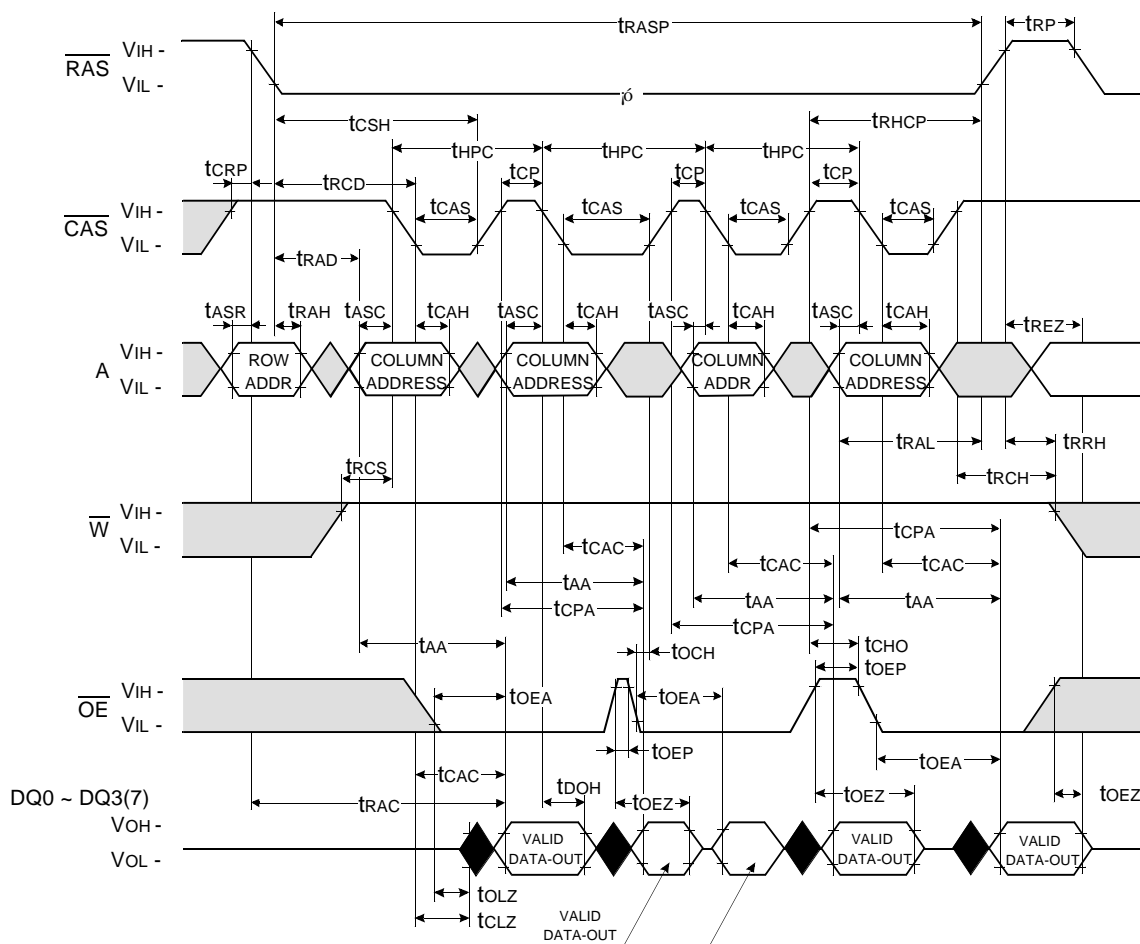
Don't care  
 Undefined

READ - MODIFY - WRITE CYCLE



Don't care  
 Undefined

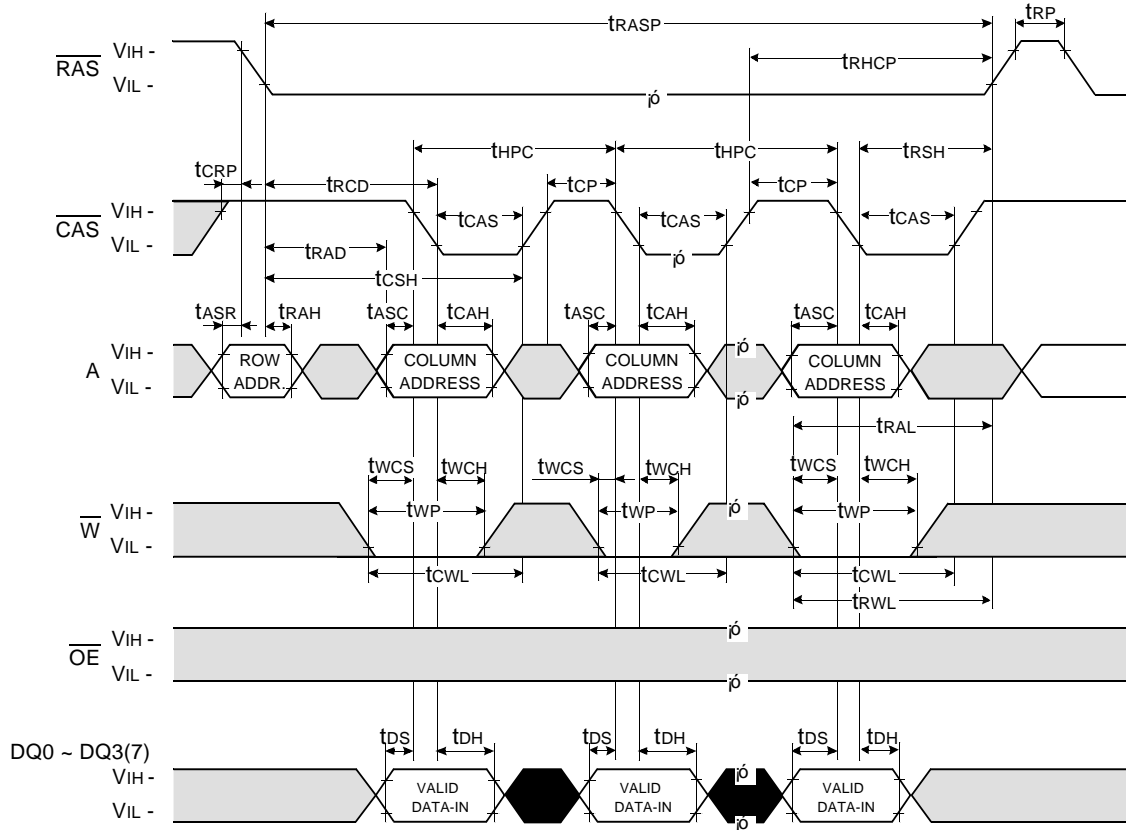
**HYPER PAGE READ CYCLE**



Don't care  
 Undefined

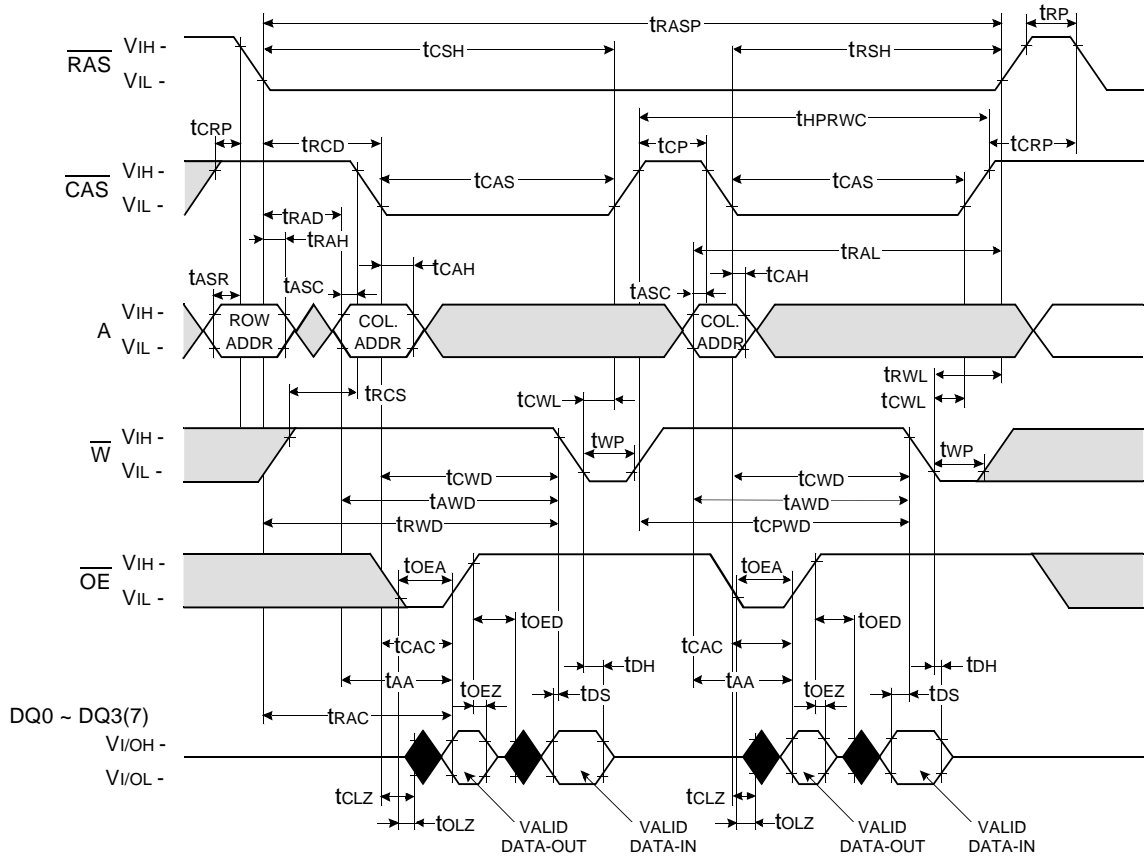
**HYPER PAGE WRITE CYCLE ( EARLY WRITE )**

NOTE : DOUT = OPEN



Don't care  
 Undefined

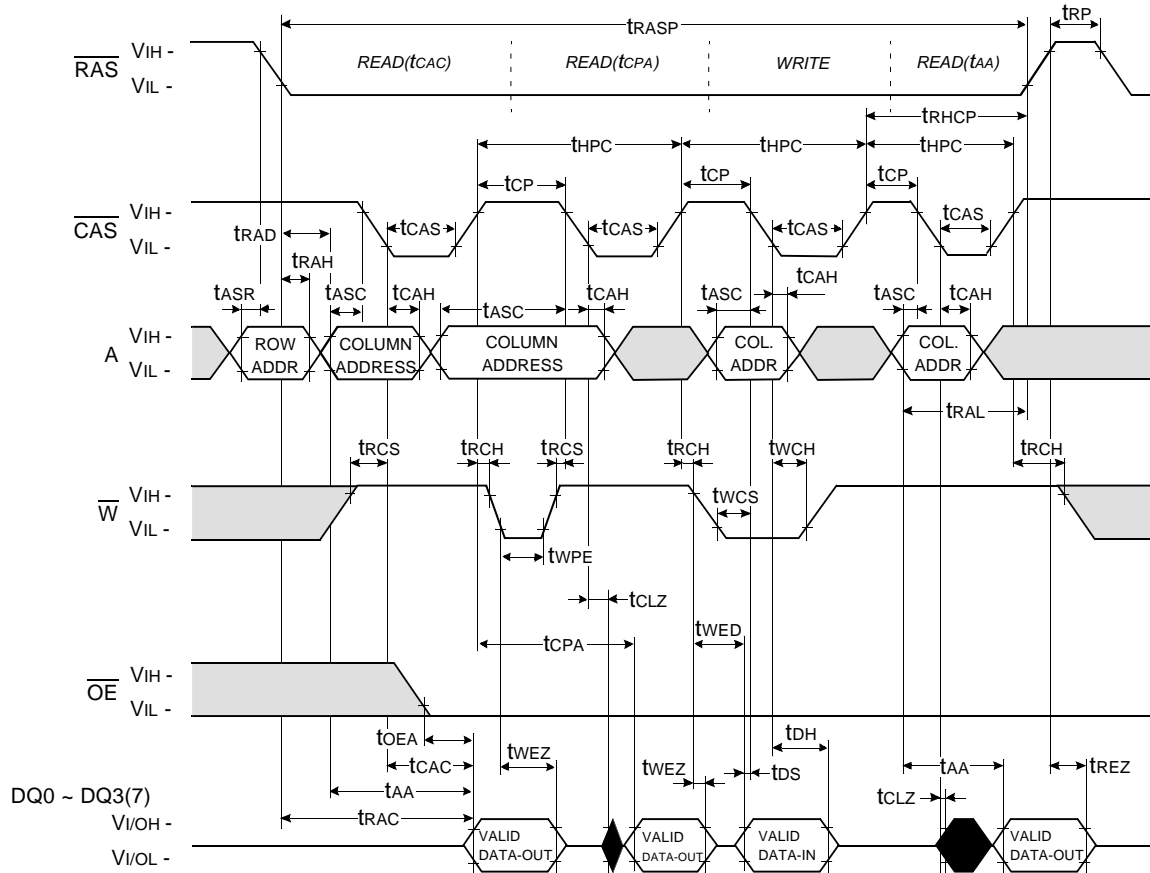
HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care  
Undefined



HYPER PAGE READ AND WRITE MIXED CYCLE



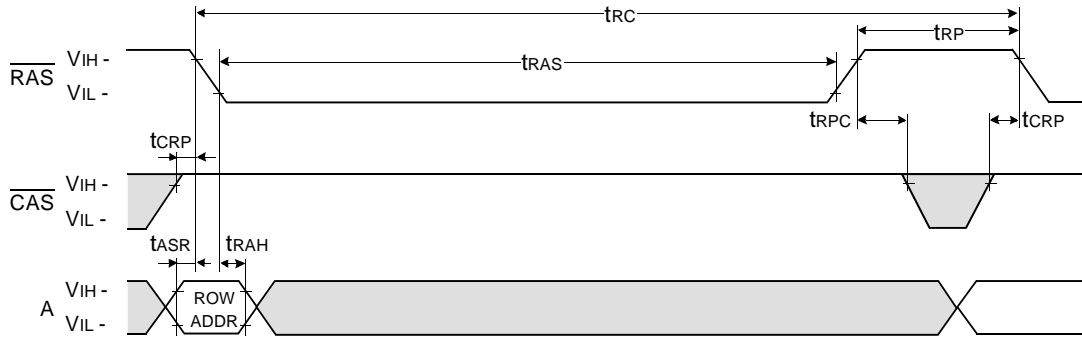
Don't care  
Undefined



**RAS - ONLY REFRESH CYCLE\***

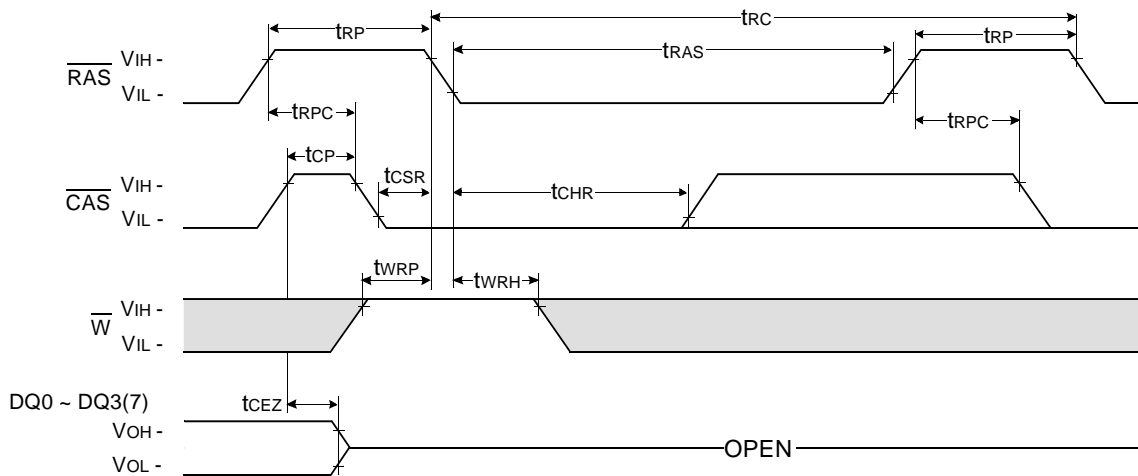
NOTE :  $\overline{W}$ ,  $\overline{OE}$ ,  $DIN$  = Don't care

DOUT = OPEN



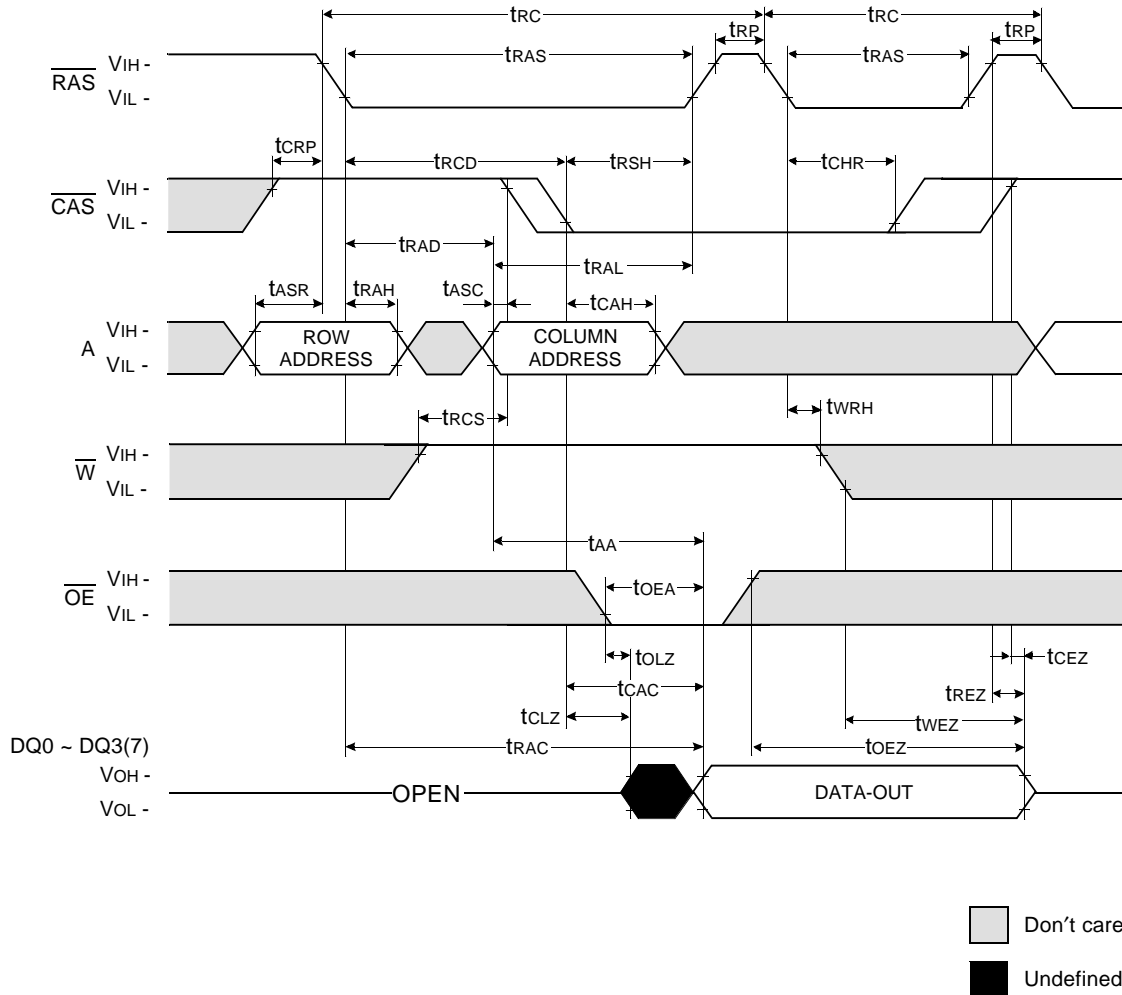
**CAS - BEFORE - RAS REFRESH CYCLE**

NOTE :  $\overline{OE}$ ,  $A$  = Don't care



Don't care  
 Undefined

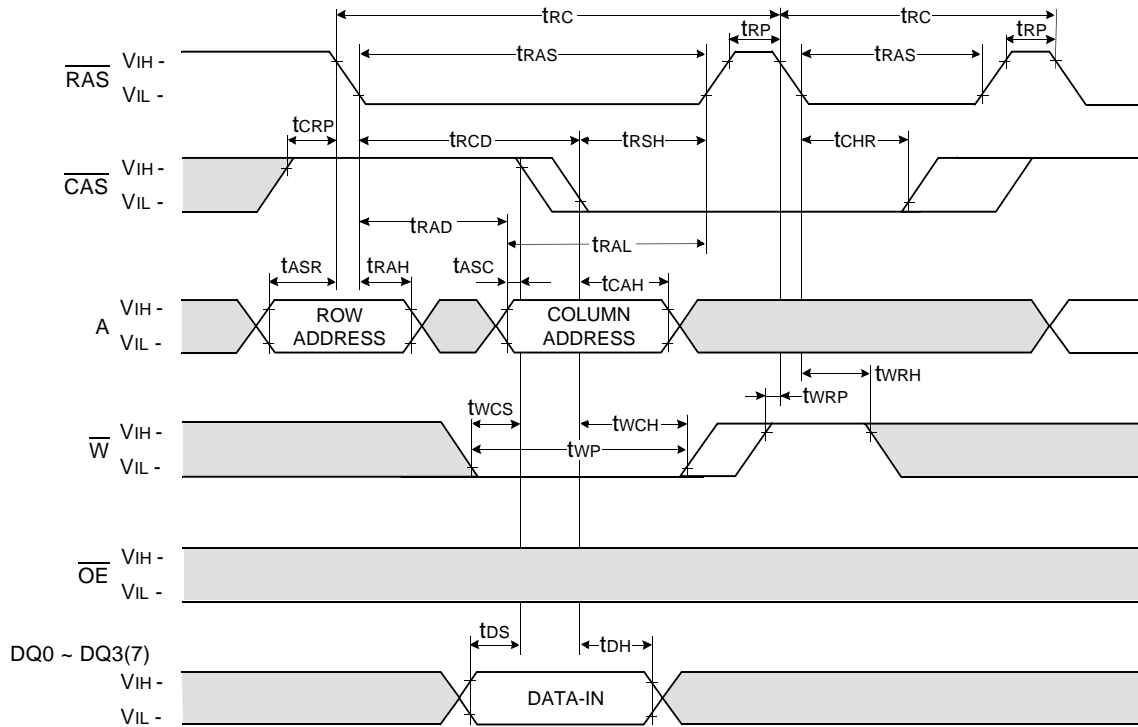
HIDDEN REFRESH CYCLE ( READ )



\* In Hidden refresh cycle of 64Mb A-die & B-die, when  $\overline{\text{CAS}}$  signal transits from Low to High, the valid data may be cut off.

**HIDDEN REFRESH CYCLE ( WRITE )**

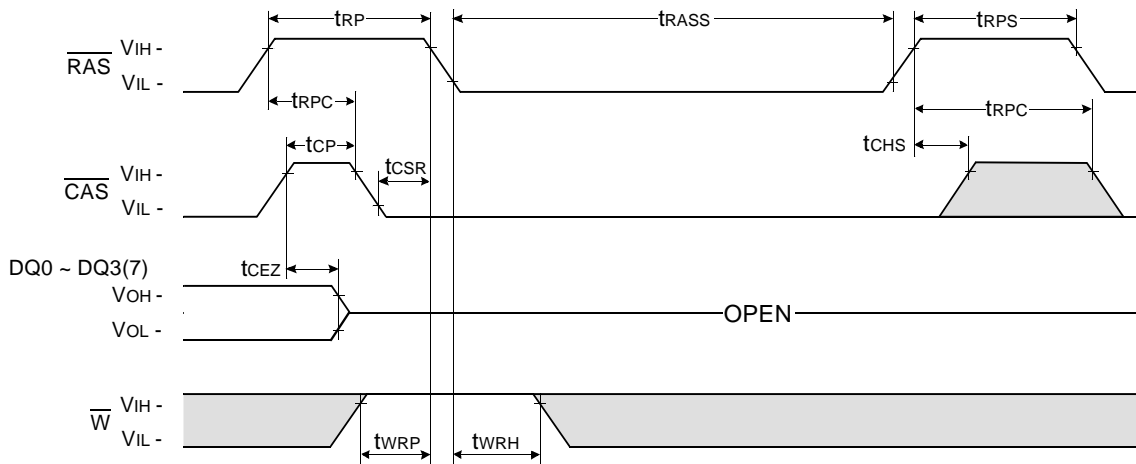
NOTE : DOUT = OPEN



Don't care  
 Undefined

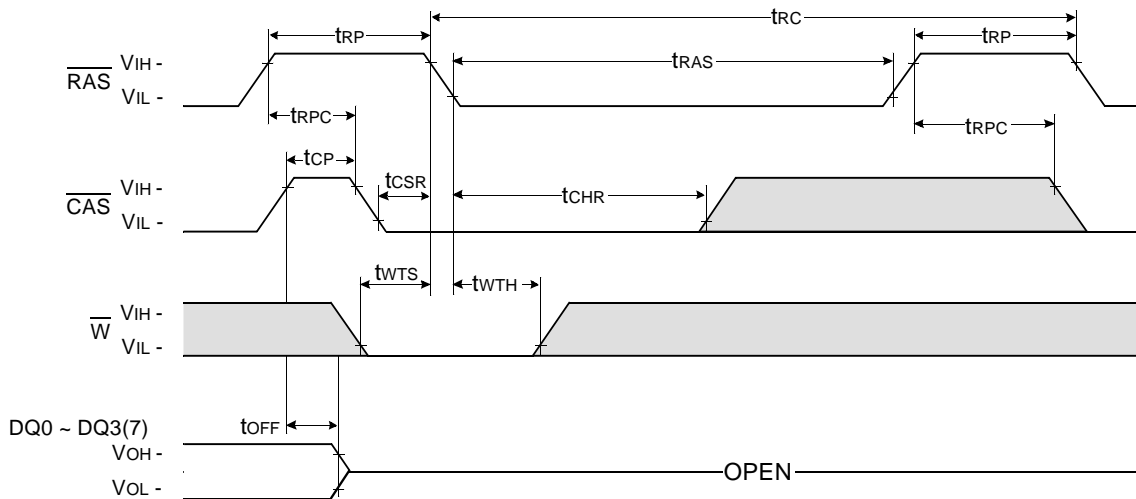
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



Don't care  
 Undefined

PACKAGE DIMENSION

