

16M x 4bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 16,777,216 x 4 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-50, or -60), package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. This 16Mx4 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

• **Part Identification**

- K4E660411C-JC(5.0V, 8K Ref., SOJ)
- K4E640411C-JC(5.0V, 4K Ref., SOJ)
- K4E660411C-TC(5.0V, 8K Ref., TSOP)
- K4E640411C-TC(5.0V, 4K Ref., TSOP)

• **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-50	495	660
-60	440	605

- Extended Data Out Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5.0V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +5.0V±10% power supply

• **Refresh Cycles**

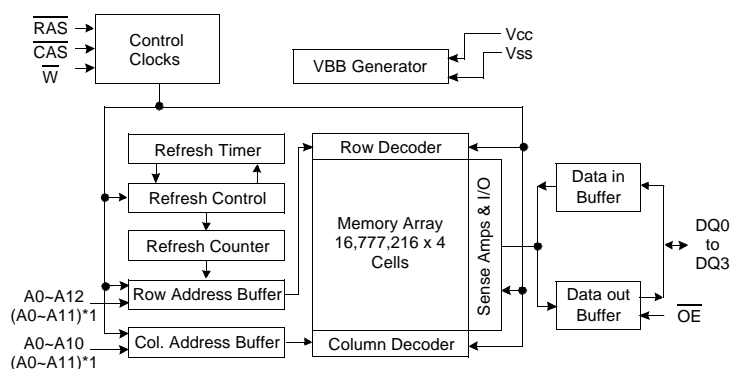
Part NO.	Refresh cycle	Refresh time
		Normal
K4E660411C*	8K	64ms
K4E640411C	4K	

* Access mode & $\overline{\text{RAS}}$ only refresh mode
 : 8K cycle/64ms
 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ & Hidden refresh mode
 : 4K cycle/64ms

• **Performance Range**

Speed	t _{TRAC}	t _{CAC}	t _{RC}	t _{PC}
-50	50ns	13ns	84ns	20ns
-60	60ns	15ns	104ns	25ns

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

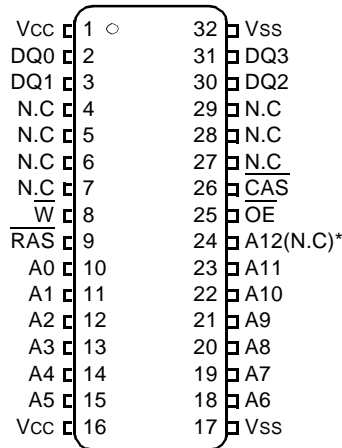
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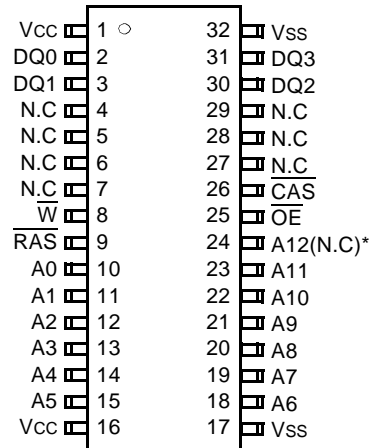
PIN CONFIGURATION (Top Views)

- K4E660411C-J
- K4E640411C-J

- K4E660411C-T
- K4E640411C-T



(J : 400mil SOJ)



(T : 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{os} Address	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.6	-	V _{CC} +1.0 ^{*1}	V
Input Low Voltage	V _{IL}	-1.0 ^{*2}	-	0.7	V

*1 : V_{CC}+2.0V at pulse width≤20ns which is measured at V_{CC}

*2 : -2.0 at pulse width≤20ns which is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.5V, all other pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V



DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4E660411C	K4E640411C	
I _{CC1}	Don't care	-50 -60	90 80	120 110	mA mA
I _{CC2}	Normal	Don't care	2	2	mA
I _{CC3}	Don't care	-50 -60	90 80	120 110	mA mA
I _{CC4}	Don't care	-50 -60	100 90	110 100	mA mA
I _{CC5}	Normal	Don't care	1	1	mA
I _{CC6}	Don't care	-50 -60	120 110	120 110	mA mA

I_{CC1}* : Operating Current (\overline{RAS} and \overline{CAS} , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} -only Refresh Current ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address cycling @t_{RC}=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current (\overline{RAS} and \overline{CAS} cycling @t_{RC}=min)

***Note** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.



K4E660411C, K4E640411C

CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ3]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 1,2)

Test condition : VCC=5.0V±10%, Vih/Vil=2.6/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Read-modify-write cycle time	tRWC	116		138		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	ns	6,14
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		ns	3
Transition time (rise and fall)	tT	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	38		45		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	8
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		10		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		ns	
Data set-up time	tDS	0		0		ns	9



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
Data hold time	tdH	8		10		ns	9
Refresh period (4K, Normal)	tREF		64		64	ms	
Refresh period (8K, Normal)	tREF		64		64	ms	
Write command set-up time	twCS	0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	30		32		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	67		77		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	42		47		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		28		35	ns	3
Hyper Page cycle time	tHPC	20		25		ns	13
Hyper Page read-modify-write cycle time	tHPRWC	47		56		ns	13
$\overline{\text{CAS}}$ precharge time (Hyper page cycle)	tCP	8		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	trASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	30		35		ns	
$\overline{\text{OE}}$ access time	toEA		13		15	ns	
$\overline{\text{OE}}$ to data delay	toED	13		13		ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tcpWD	45		54		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	3	13	3	13	ns	6
$\overline{\text{OE}}$ command hold time	toEH	13		15		ns	
Write command set-up time (Test mode in)	twTS	10		10		ns	11
Write command hold time (Test mode in)	twTH	10		10		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRP	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	treZ	3	13	3	13	ns	6,14
Output buffer turn off delay from $\overline{\text{W}}$	tweZ	3	13	3	13	ns	6
$\overline{\text{W}}$ to data delay	twED	15		15		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	toCH	5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		ns	
$\overline{\text{OE}}$ precharge time	toEP	5		5		ns	
$\overline{\text{W}}$ pulse width (Hyper page Cycle)	twPE	5		5		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	trASS	100		100		us	15,16,17
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	trPS	90		110		ns	15,16,17
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tchs	-50		-50		ns	15,16,17

TEST MODE CYCLE

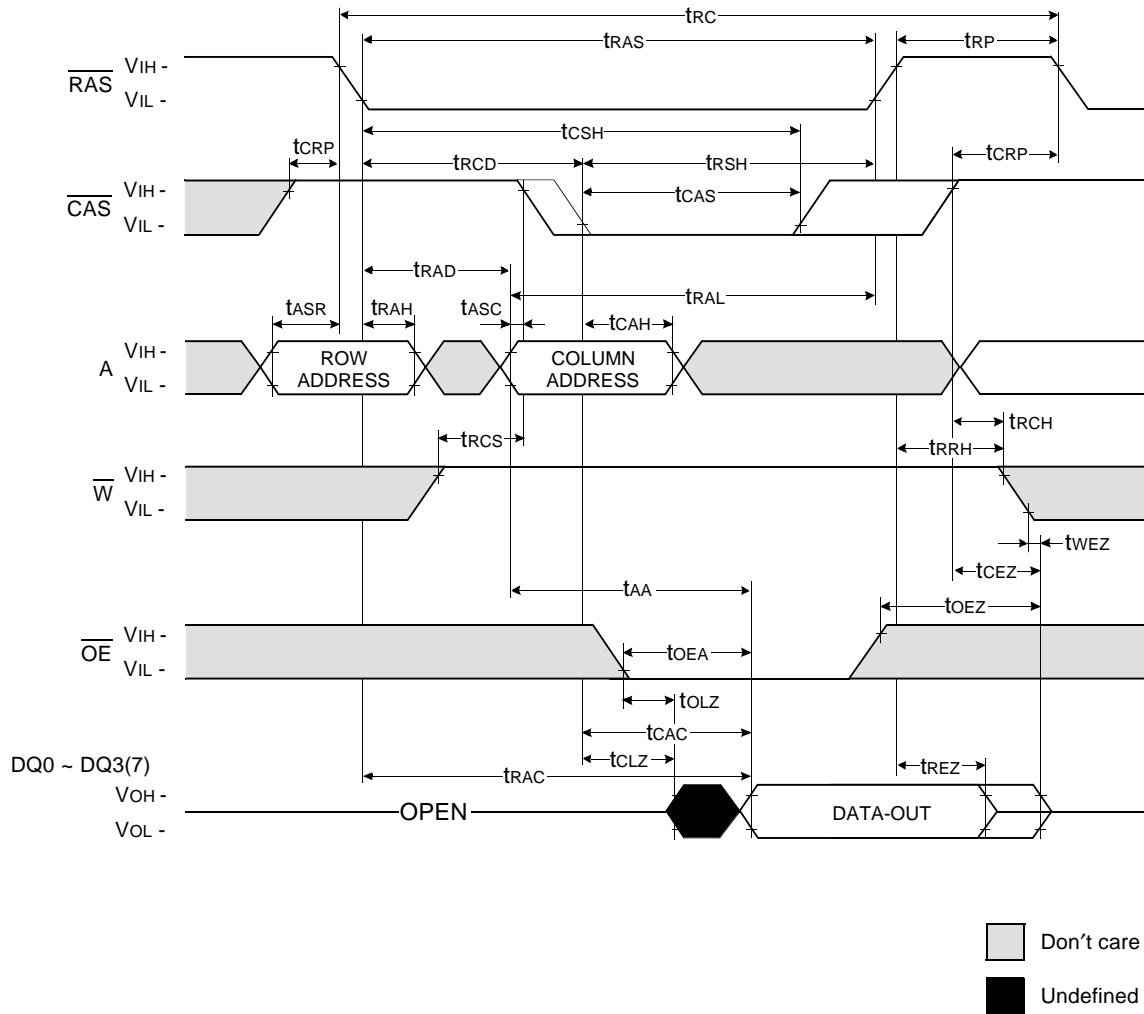
(Note 11)

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	89		109		ns	
Read-modify-write cycle time	t _{RWC}	121		145		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t _{CAC}		18		20	ns	3,4,5,12
Access time from column address	t _{AA}		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t _{RAS}	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	18		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	43		50		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	35		39		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	72		84		ns	7
Column Address to $\overline{\text{W}}$ delay time	t _{AWD}	47		54		ns	7
Hyper Page cycle time	t _{HPC}	25		30		ns	13
Hyper Page read-modify-write cycle time	t _{HPRWC}	53		61		ns	13
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	t _{RASP}	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		33		40	ns	3
$\overline{\text{OE}}$ access time	t _{OE}		18		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OE}	18		20		ns	
$\overline{\text{OE}}$ command hold time	t _{OE}	18		20		ns	

NOTES

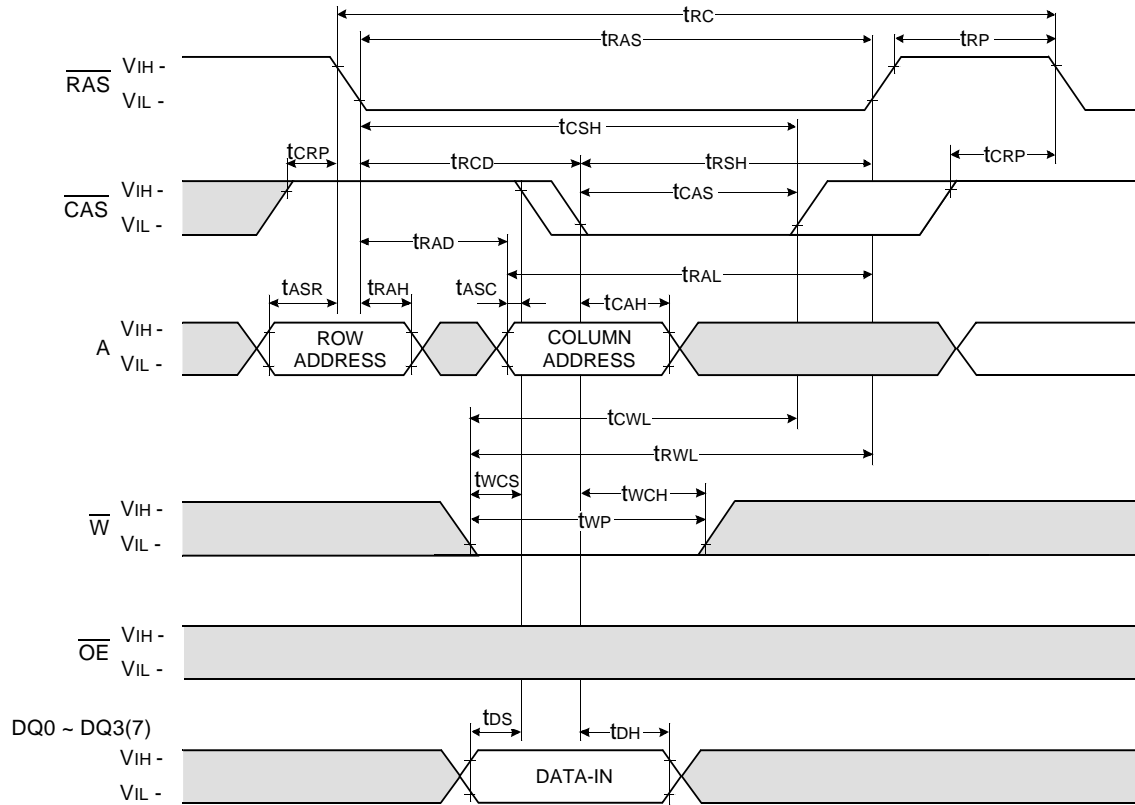
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL load and 100pF.
4. Operation within the $t_{\text{RC}}(\text{max})$ limit insures that $t_{\text{AC}}(\text{max})$ can be met. $t_{\text{RC}}(\text{max})$ is specified as a reference point only. If t_{RC} is greater than the specified $t_{\text{RC}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RC}} \geq t_{\text{RC}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{AC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{AC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. $t_{\text{ASC}} \geq 6\text{ns}$, Assume $t_{\text{T}} = 2.0\text{ns}$
14. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
15. If $t_{\text{RASS}} \geq 100\mu\text{s}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
16. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096(4K/8K) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
17. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

READ CYCLE



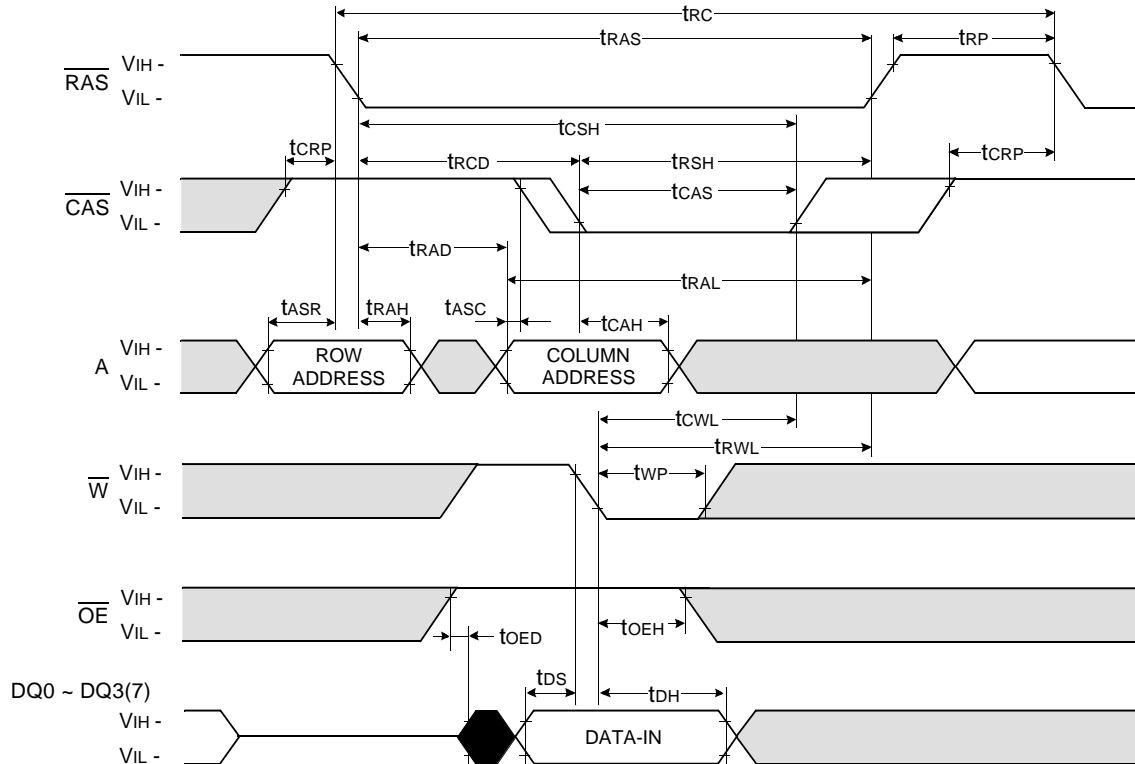
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



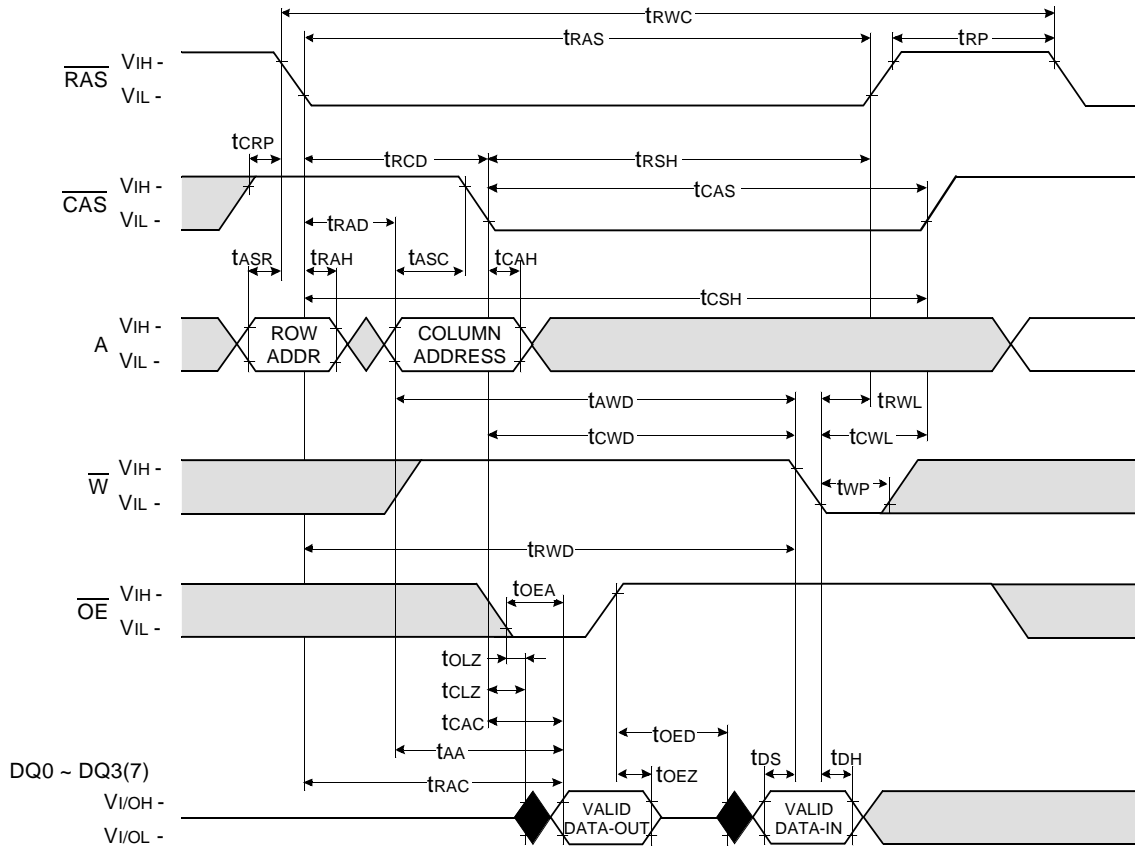
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



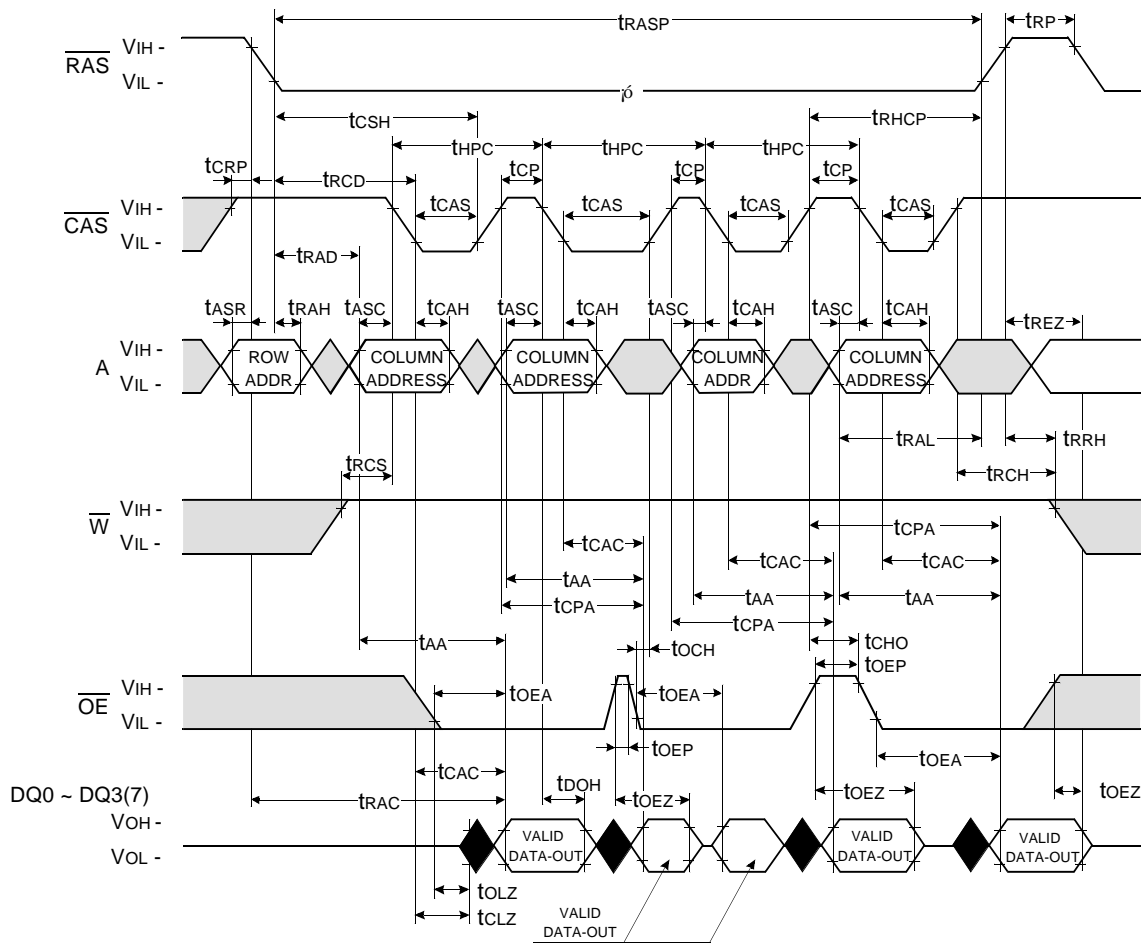
Don't care
 Undefined

READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

HYPER PAGE READ CYCLE

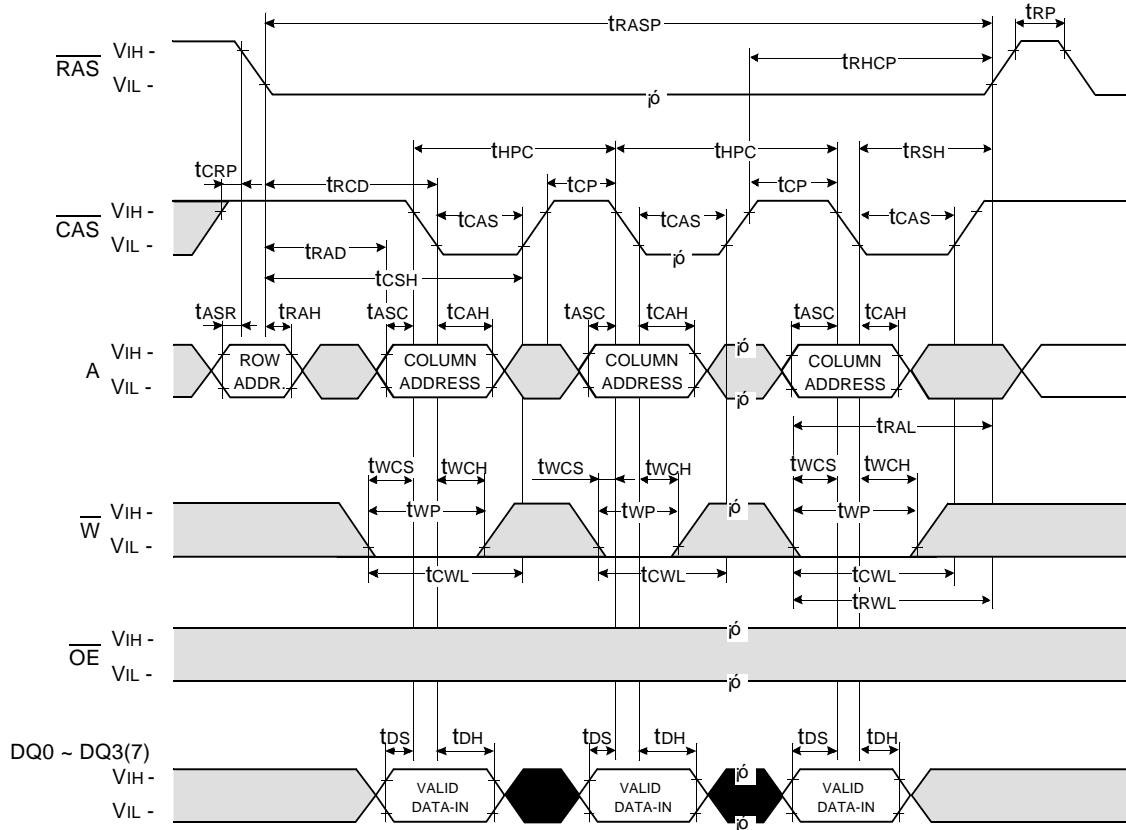


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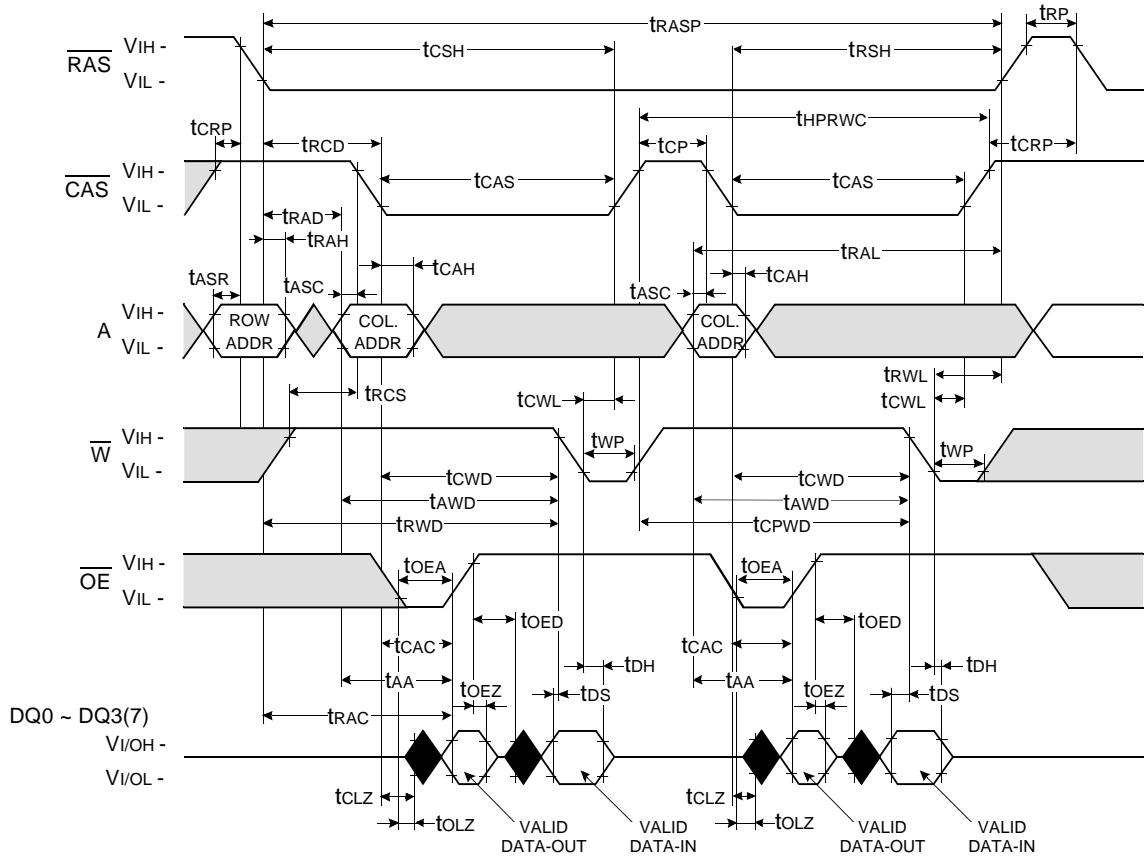
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

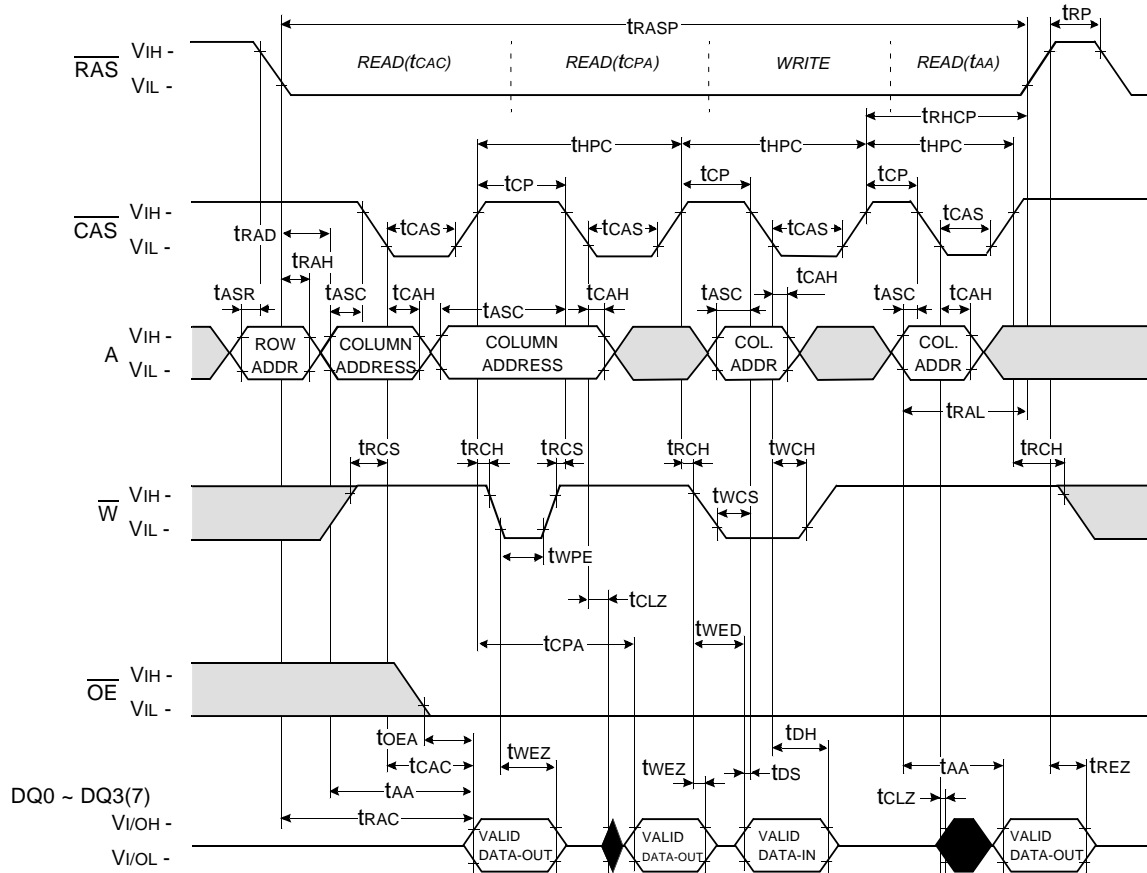


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HYPER PAGE READ-MODIFY-WRITE CYCLE



HYPER PAGE READ AND WRITE MIXED CYCLE

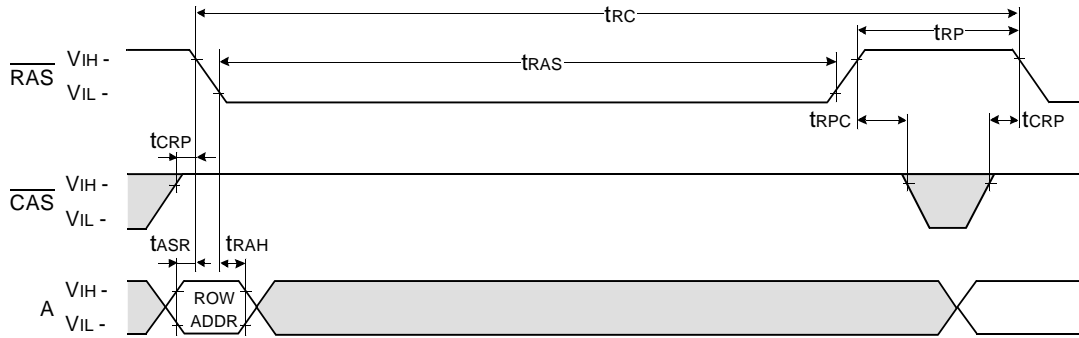


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RAS - ONLY REFRESH CYCLE*

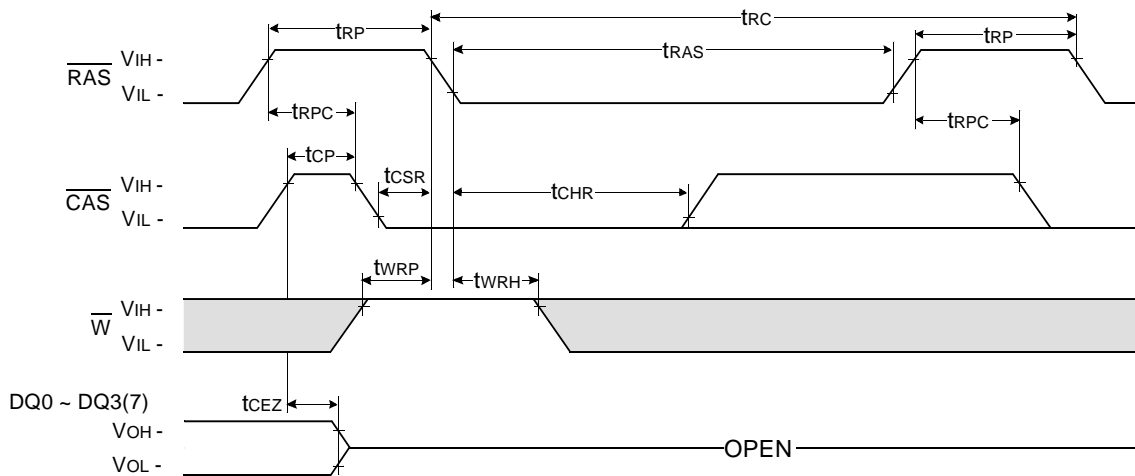
NOTE : \overline{W} , \overline{OE} , DIN = Don't care

DOUT = OPEN



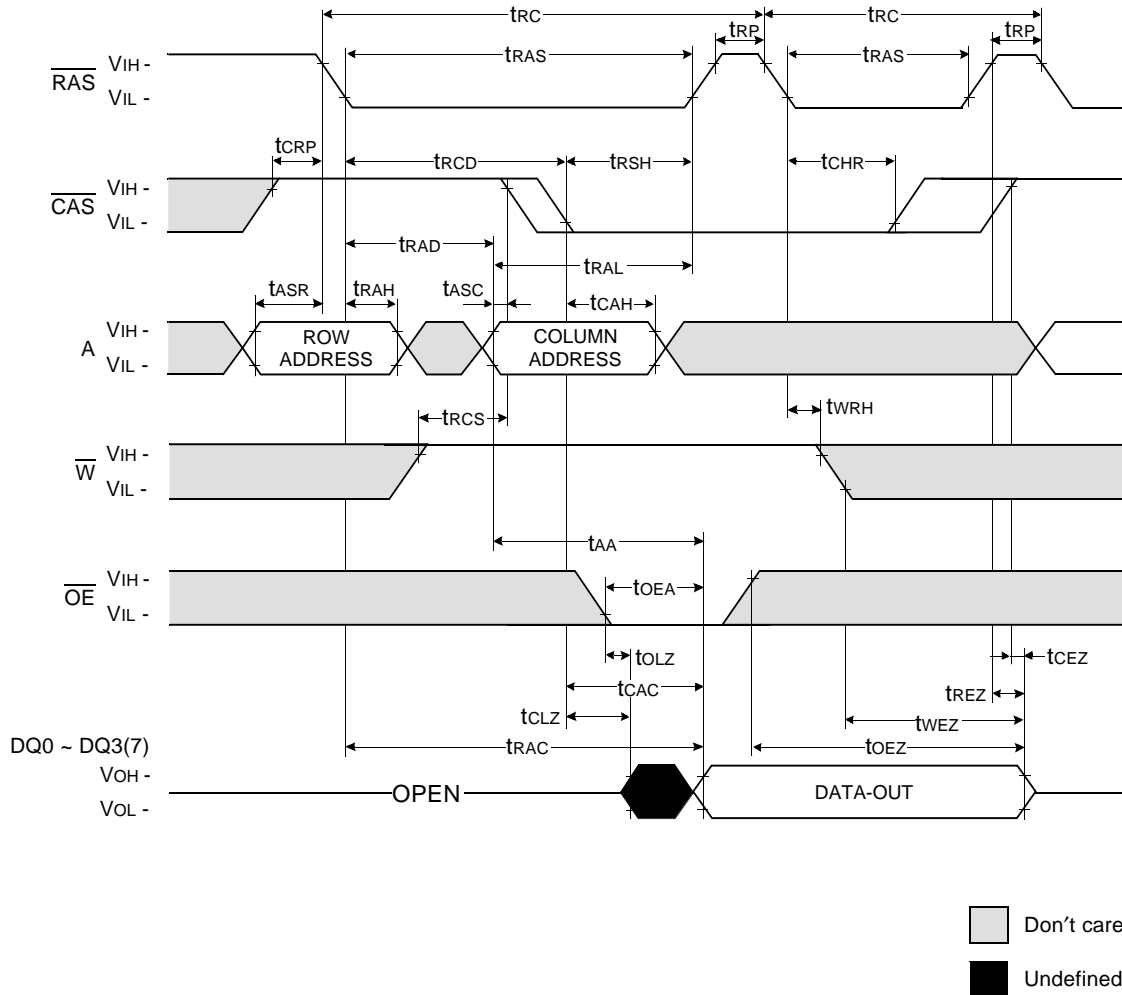
CAS - BEFORE - RAS REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



Don't care
 Undefined

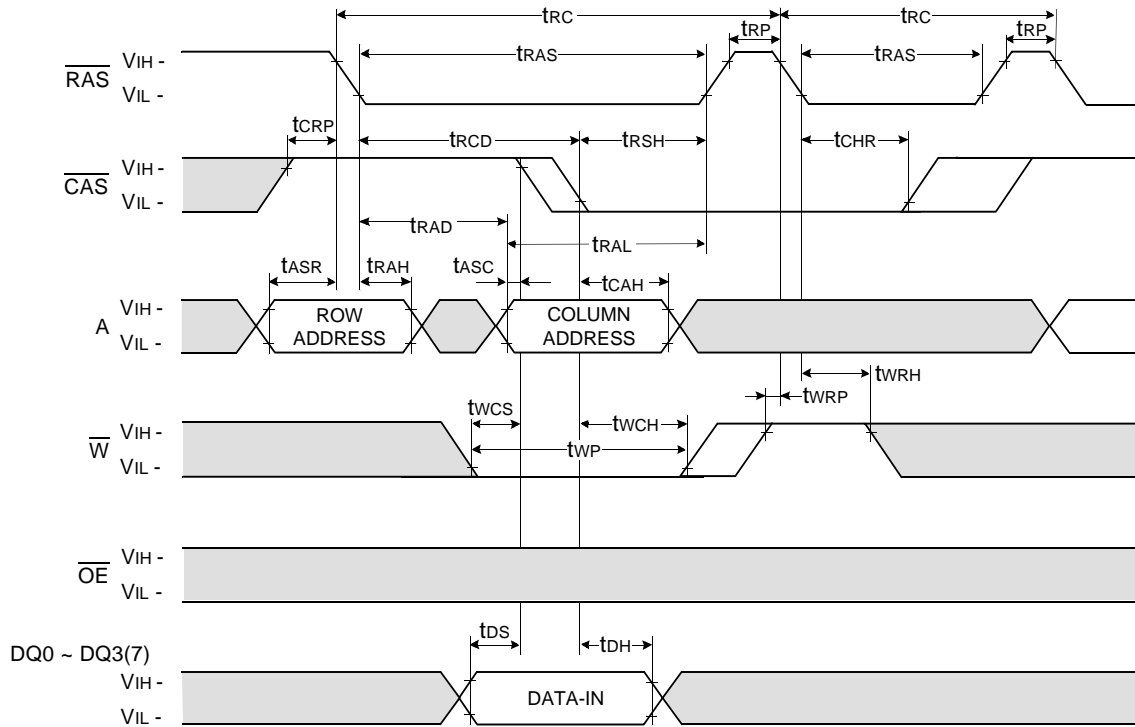
HIDDEN REFRESH CYCLE (READ)



* In Hidden refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (WRITE)

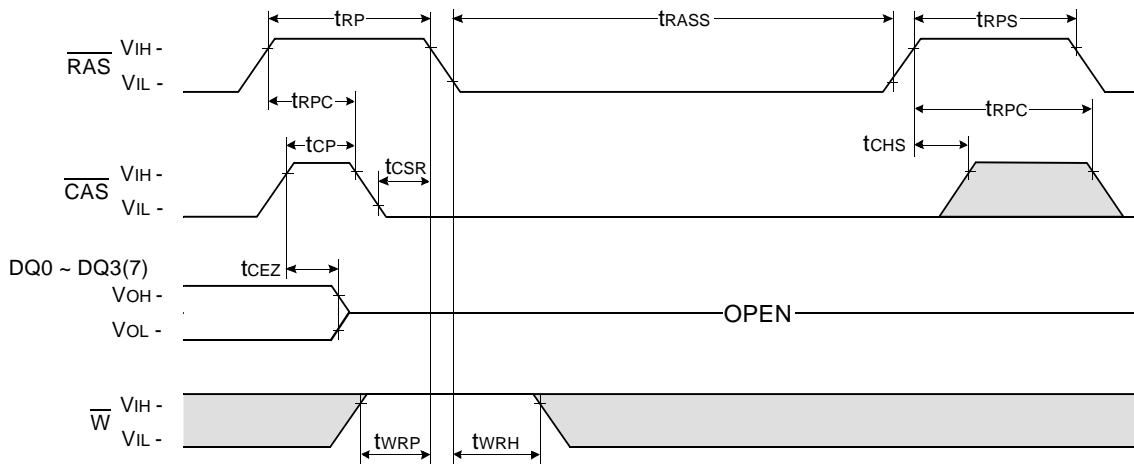
NOTE : DOUT = OPEN



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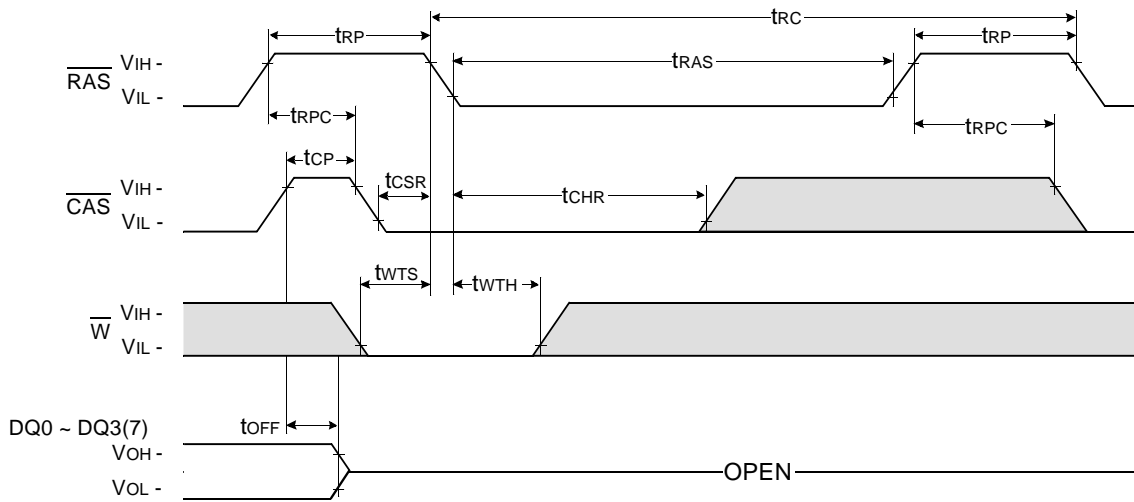
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



Don't care
 Undefined

PACKAGE DIMENSION

