

*4M x 16bit CMOS Dynamic RAM with Extended Data Out*

**DESCRIPTION**

This is a family of 4,194,304 x 16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

**FEATURES**

• **Part Identification**

- K4E661612C-TC/L(3.3V, 8K Ref.)
- K4E641612C-TC/L(3.3V, 4K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	324	468
-50	288	432
-60	252	396

• **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
K4E661612C*	8K	64ms	128ms
K4E641612C	4K		

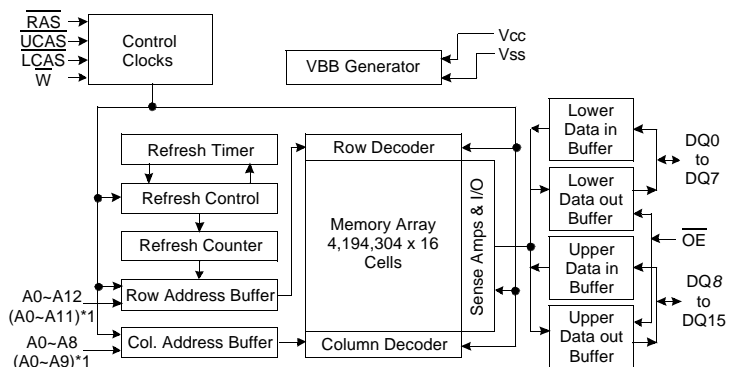
\* Access mode & RAS only refresh mode  
 : 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)  
 CAS-before-RAS & Hidden refresh mode  
 : 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

• **Performance Range**

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>HPC</sub>
-45	45ns	12ns	74ns	17ns
-50	50ns	13ns	84ns	20ns
-60	60ns	15ns	104ns	25ns

- Extended Data Out Mode operation
- 2  $\overline{\text{CAS}}$  Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Fast parallel test mode capability
- Self-refresh capability (L-ver only)
- LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) packages
- +3.3V±0.3V power supply

**FUNCTIONAL BLOCK DIAGRAM**



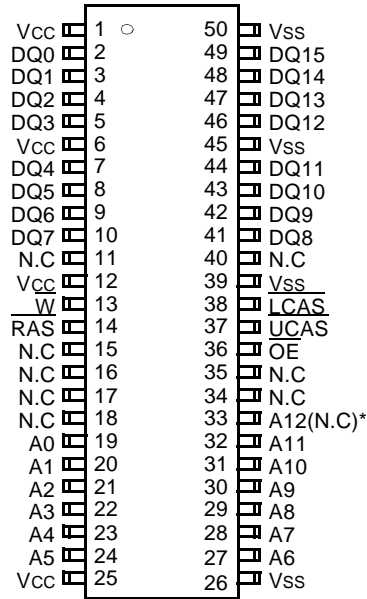
Note) \*1 : 4K Refresh

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PIN CONFIGURATION (Top Views)

- K4E661612C-T
- K4E641612C-T



(400mil TSOP(II))

\*(N.C) : N.C for 4K Refresh Product

Pin Name	Pin function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+3.3V)
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	1	W
Short Circuit Output Current	Ios Address	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, TA= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.0	-	Vcc+0.3*1	V
Input Low Voltage	VIL	-0.3*2	-	0.8	V

\*1 : Vcc+1.3V at pulse width≤15ns which is measured at Vcc

\*2 : -1.3 at pulse width≤15ns which is measured at Vss

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤VIN≤VCC+0.3V, all other pins not under test=0 Volt)	Ii(L)	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤VOUT≤VCC)	Io(L)	-5	5	uA
Output High Voltage Level(IoH=-2mA)	VOH	2.4	-	V
Output Low Voltage Level(IoL=2mA)	VOL	-	0.4	V



**DC AND OPERATING CHARACTERISTICS** (Continued)

Symbol	Power	Speed	Max		Units
			K4E661612C	K4E641612C	
I <sub>CC1</sub>	Don't care	-45	90	130	mA
		-50	80	120	mA
		-60	70	110	mA
I <sub>CC2</sub>	Normal L	Don't care	1	1	mA
			1	1	mA
I <sub>CC3</sub>	Don't care	-45	90	130	mA
		-50	80	120	mA
		-60	70	110	mA
I <sub>CC4</sub>	Don't care	-45	100	100	mA
		-50	90	90	mA
		-60	80	80	mA
I <sub>CC5</sub>	Normal L	Don't care	0.5	0.5	mA
			200	200	uA
I <sub>CC6</sub>	Don't care	-45	130	130	mA
		-50	120	120	mA
		-60	110	110	mA
I <sub>CC7</sub>	L	Don't care	350	350	uA
I <sub>CCS</sub>	L	Don't care	350	350	uA

I<sub>CC1</sub>\* : Operating Current ( $\overline{RAS}$  and  $\overline{UCAS}$ ,  $\overline{LCAS}$ , Address cycling @t<sub>RC</sub>=min.)

I<sub>CC2</sub> : Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub>\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{UCAS}=\overline{LCAS}=V_{IH}$ ,  $\overline{RAS}$ , Address cycling @t<sub>RC</sub>=min.)

I<sub>CC4</sub>\* : Extended Data Out Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{UCAS}$  or  $\overline{LCAS}$ , Address cycling @t<sub>HPC</sub>=min.)

I<sub>CC5</sub> : Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub>\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$  and  $\overline{UCAS}$  or  $\overline{LCAS}$  cycling @t<sub>RC</sub>=min)

I<sub>CC7</sub> : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V<sub>IH</sub>)=V<sub>CC</sub>-0.2V, Input low voltage(V<sub>IL</sub>)=0.2V,  $\overline{UCAS}$ ,  $\overline{LCAS}=\overline{CAS}$ -before- $\overline{RAS}$  cycling or 0.2V

$\overline{W}$ ,  $\overline{OE}=V_{IH}$ , Address=Don't care, DQ=Open, T<sub>RC</sub>=31.25us

I<sub>CCS</sub> : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=0.2V$ ,  $\overline{W}=\overline{OE}=A_0 \sim A_{12}(A_{11})=V_{CC}-0.2V$  or 0.2V, DQ0 ~ DQ15=V<sub>CC</sub>-0.2V, 0.2V or Open

**\*Note :** I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub>, I<sub>CC3</sub> and I<sub>CC6</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one EDO mode cycle time, t<sub>HPC</sub>.



# K4E661612C, K4E641612C

# CMOS DRAM

## CAPACITANCE (TA=25°C, VCC=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	CIN1	-	5	pF
Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{W}}$ , $\overline{\text{OE}}$ ]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

## AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 2)

Test condition : VCC=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	74		84		104		ns	
Read-modify-write cycle time	tRWC	101		113		138		ns	
Access time from $\overline{\text{RAS}}$	tRAC		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		12		13		15	ns	3,4,5
Access time from column address	tAA		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	3	13	ns	6,20
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	1	50	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	25		30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	8		8		10		ns	
$\overline{\text{CAS}}$ hold time	tCSH	35		38		40		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	7	5K	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	11	33	11	37	14	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	9	22	9	25	12	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	7		7		10		ns	
Column address set-up time	tASC	0		0		0		ns	13
Column address hold time	tCAH	7		7		10		ns	13
Column address to $\overline{\text{RAS}}$ lead time	tRAL	23		25		30		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	7		7		10		ns	
Write command pulse width	tWP	6		7		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	8		8		10		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	7		7		10		ns	16
Data set-up time	tDS	0		0		0		ns	9,19



## AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Data hold time	t <sub>DH</sub>	7		7		10		ns	9,19
Refresh period (Normal)	t <sub>REF</sub>		64		64		64	ms	
Refresh period (L-ver)	t <sub>REF</sub>		128		128		128	ms	
Write command set-up time	t <sub>WCS</sub>	0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	24		27		32		ns	7,15
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	57		64		77		ns	7
Column address to $\overline{\text{W}}$ delay time	t <sub>AWD</sub>	35		39		47		ns	7
$\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t <sub>CSR</sub>	5		5		5		ns	17
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t <sub>CHR</sub>	10		10		10		ns	18
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t <sub>RPC</sub>	5		5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>		24		28		35	ns	3
Hyper Page cycle time	t <sub>HPC</sub>	17		20		25		ns	21
Hyper Page read-modify-write cycle time	t <sub>HPRWC</sub>	47		47		56		ns	21
$\overline{\text{CAS}}$ precharge time (Hyper page cycle)	t <sub>CP</sub>	6.5		7		10		ns	14
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	t <sub>RASP</sub>	45	200K	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t <sub>RHCP</sub>	24		30		35		ns	
$\overline{\text{OE}}$ access time	t <sub>OEA</sub>		12		13		15	ns	3
$\overline{\text{OE}}$ to data delay	t <sub>OED</sub>	8		10		13		ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t <sub>CPWD</sub>	36		41		52		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	t <sub>OEZ</sub>	3	11	3	13	3	13	ns	6
$\overline{\text{OE}}$ command hold time	t <sub>OEH</sub>	5		5		5		ns	
Write command set-up time (Test mode in)	t <sub>WTS</sub>	10		10		10		ns	11
Write command hold time (Test mode in)	t <sub>WTH</sub>	10		10		10		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time (C-B-R refresh)	t <sub>WRP</sub>	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time (C-B-R refresh)	t <sub>WRH</sub>	10		10		10		ns	
Output data hold time	t <sub>DOH</sub>	4		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	t <sub>REZ</sub>	3	13	3	13	3	13	ns	6,20
Output buffer turn off delay from $\overline{\text{W}}$	t <sub>WEZ</sub>	3	13	3	13	3	13	ns	6
$\overline{\text{W}}$ to data delay	t <sub>WED</sub>	8		15		15		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t <sub>OCH</sub>	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	t <sub>CHO</sub>	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	t <sub>OEP</sub>	5		5		5		ns	
$\overline{\text{W}}$ pulse width (Hyper Page Cycle)	t <sub>WPE</sub>	5		5		5		ns	
$\overline{\text{RAS}}$ pulse width (C-B-R self refresh)	t <sub>RASS</sub>	100		100		100		us	22,23,24
$\overline{\text{RAS}}$ precharge time (C-B-R self refresh)	t <sub>RPS</sub>	74		90		110		ns	22,23,24
$\overline{\text{CAS}}$ hold time (C-B-R self refresh)	t <sub>CHS</sub>	-50		-50		-50		ns	22,23,24

## TEST MODE CYCLE

( Note 11 )

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	79		89		109		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	110		121		145		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		50		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		17		18		20	ns	3,4,5,12
Access time from column address	t <sub>AA</sub>		28		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	50	10K	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	12	10K	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	18		18		20		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	39		43		50		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	28		30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	29		35		39		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	62		72		84		ns	7
Column Address to $\overline{\text{W}}$ delay time	t <sub>AWD</sub>	40		47		54		ns	7
Hyper Page cycle time	t <sub>HPC</sub>	22		25		30		ns	21
Hyper Page read-modify-write cycle time	t <sub>HPRWC</sub>	52		53		61		ns	21
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	t <sub>RASP</sub>	50	200K	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>		29		33		40	ns	3
$\overline{\text{OE}}$ access time	t <sub>OEa</sub>		17		18		20	ns	3
$\overline{\text{OE}}$ to data delay	t <sub>OEED</sub>	13		18		20		ns	
$\overline{\text{OE}}$ command hold time	t <sub>OEh</sub>	13		18		20		ns	

**NOTES**

1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2. Input voltage levels are  $V_{ih}/V_{il}$ .  $V_{ih}(\text{min})$  and  $V_{il}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{ih}(\text{min})$  and  $V_{il}(\text{max})$  and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the  $t_{\text{RC}}(\text{max})$  limit insures that  $t_{\text{AC}}(\text{max})$  can be met.  $t_{\text{RC}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RC}}$  is greater than the specified  $t_{\text{RC}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. Assumes that  $t_{\text{RC}} \geq t_{\text{RC}}(\text{max})$ .
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{oh}$  or  $V_{ol}$ .
7.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$  and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
9. This parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles and to the  $\overline{\text{W}}$  falling edge in  $\overline{\text{OE}}$  controlled write cycle and read-modify-write cycles.
10. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{AC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of  $t_{\text{AC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13.  $t_{\text{ASC}}$ ,  $t_{\text{CAH}}$  are referenced to the earlier  $\overline{\text{CAS}}$  falling edge.
14.  $t_{\text{CP}}$  is specified from the last  $\overline{\text{CAS}}$  rising edge in the previous cycle to the first  $\overline{\text{CAS}}$  falling edge in the next cycle.
15.  $t_{\text{CWD}}$  is referenced to the later  $\overline{\text{CAS}}$  falling edge at word read-modify-write cycle.

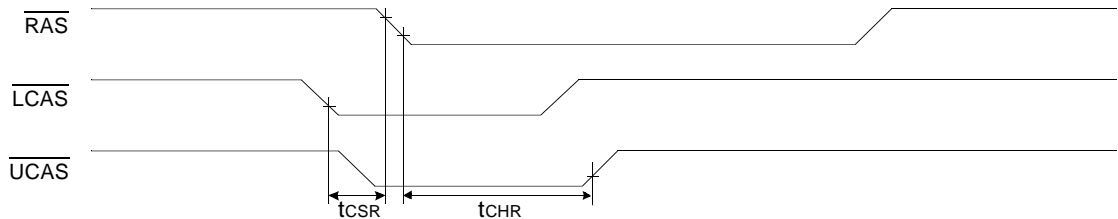
**K4E64(6)1612C Truth Table**

RAS	LCAS	UCAS	W	OE	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

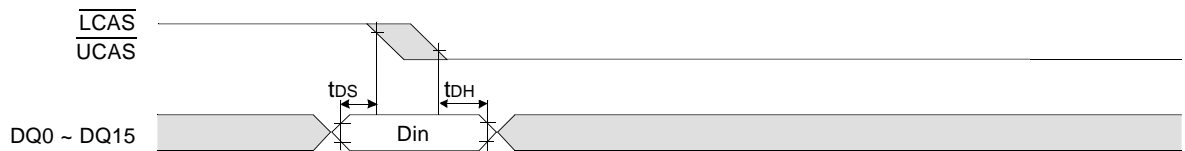




- 16. tcWL is specified from  $\overline{W}$  falling edge to the earlier  $\overline{CAS}$  rising edge.
- 17. tCSR is referenced to earlier  $\overline{CAS}$  falling before  $\overline{RAS}$  transition low.
- 18. tCHR is referenced to the later  $\overline{CAS}$  rising high after  $\overline{RAS}$  transition low.

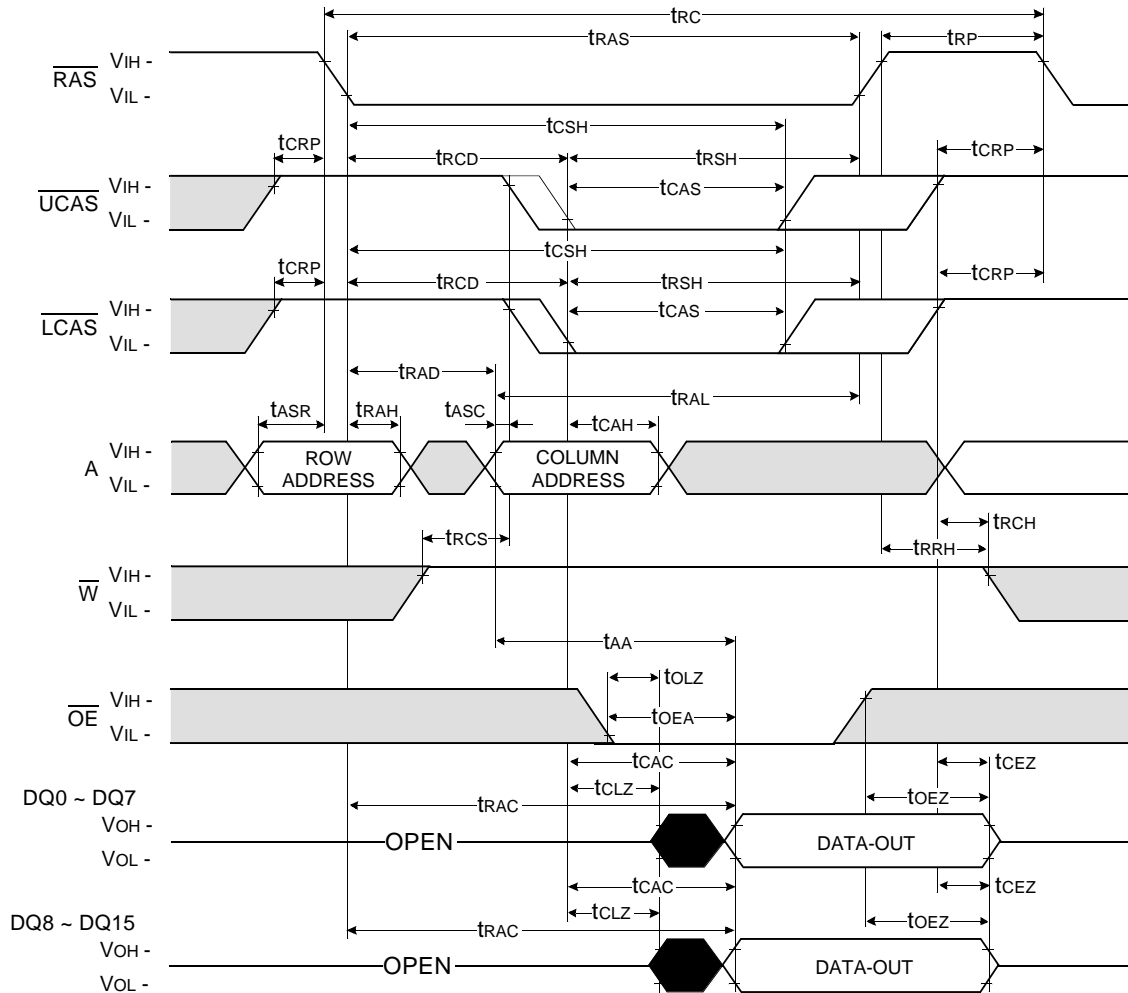


- 19. tds is specified for the earlier  $\overline{CAS}$  falling edge and tDH is specified by the later  $\overline{CAS}$  falling edge in early write cycle.



- 20. If  $\overline{RAS}$  goes high before  $\overline{CAS}$  high going, the open circuit condition of the output is achieved by  $\overline{CAS}$  high going.
- 21.  $t_{ASC} \geq 6ns$ , Assume  $t_T = 2.0ns$ , if  $t_{ASC} \leq 6ns$ , then  $t_{HPC}(min)$  and  $t_{CAS}(min)$  must be increased by the value of "6ns-tASC".
- 22. If  $t_{RAS} \geq 100us$ , then  $\overline{RAS}$  precharge time must use  $t_{RPS}$  instead of  $t_{RP}$ .
- 23. For  $\overline{RAS}$ -only-Refresh and Burst  $\overline{CAS}$ -before- $\overline{RAS}$  refresh mode, 4096 cycles(4K/8K) of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
- 24. For distributed  $\overline{CAS}$ -before- $\overline{RAS}$  with 15.6us interval, CBR refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

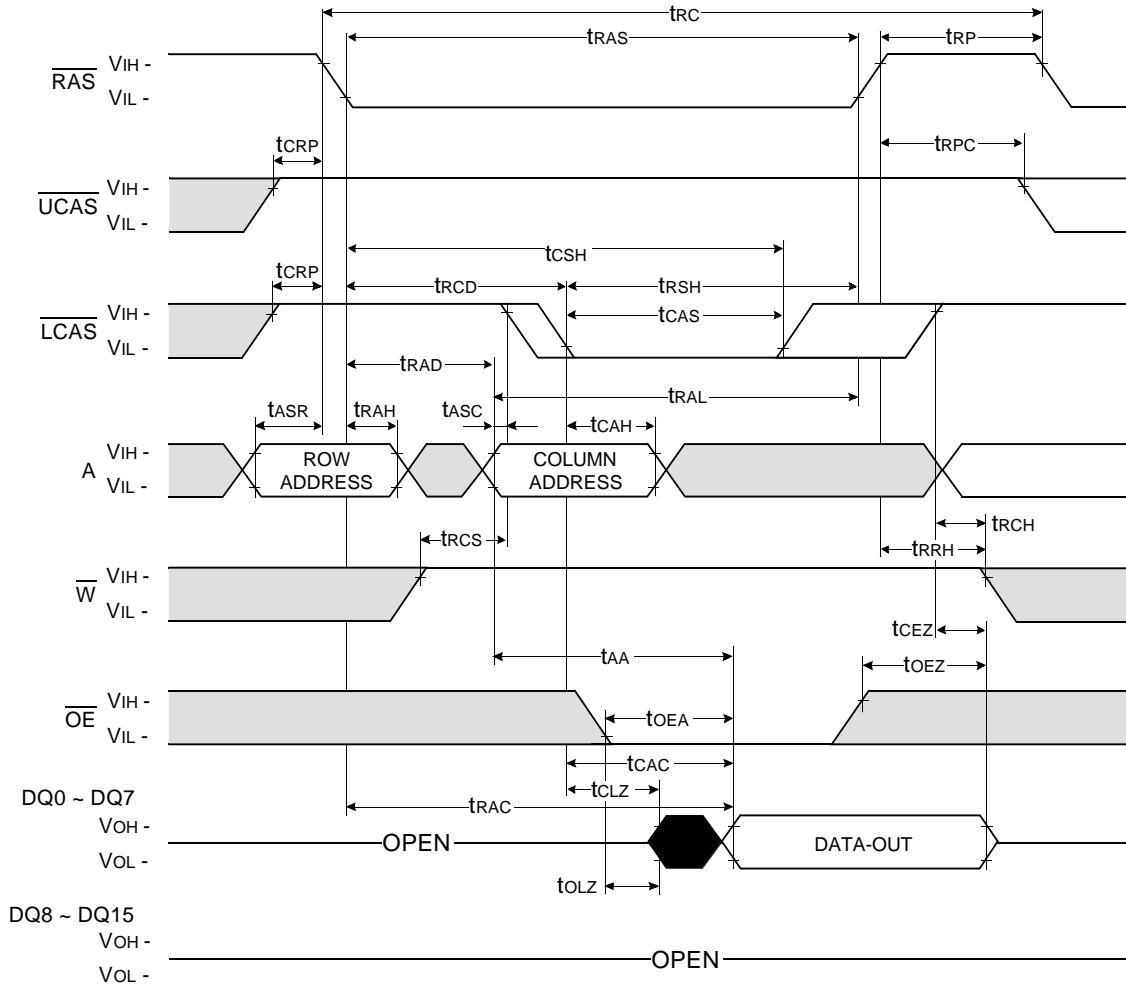
WORD READ CYCLE



Don't care  
 Undefined

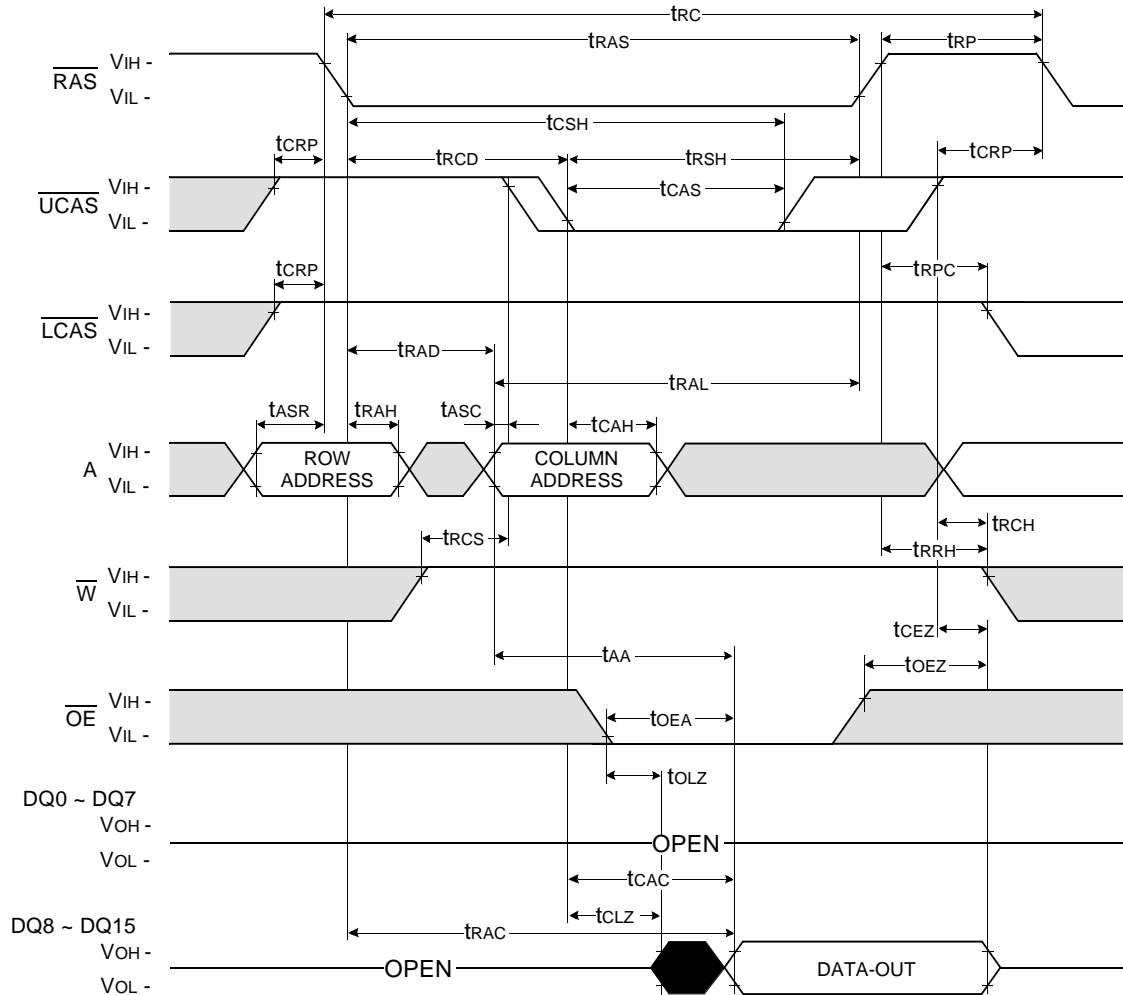
LOWER BYTE READ CYCLE

NOTE : DIN = OPEN



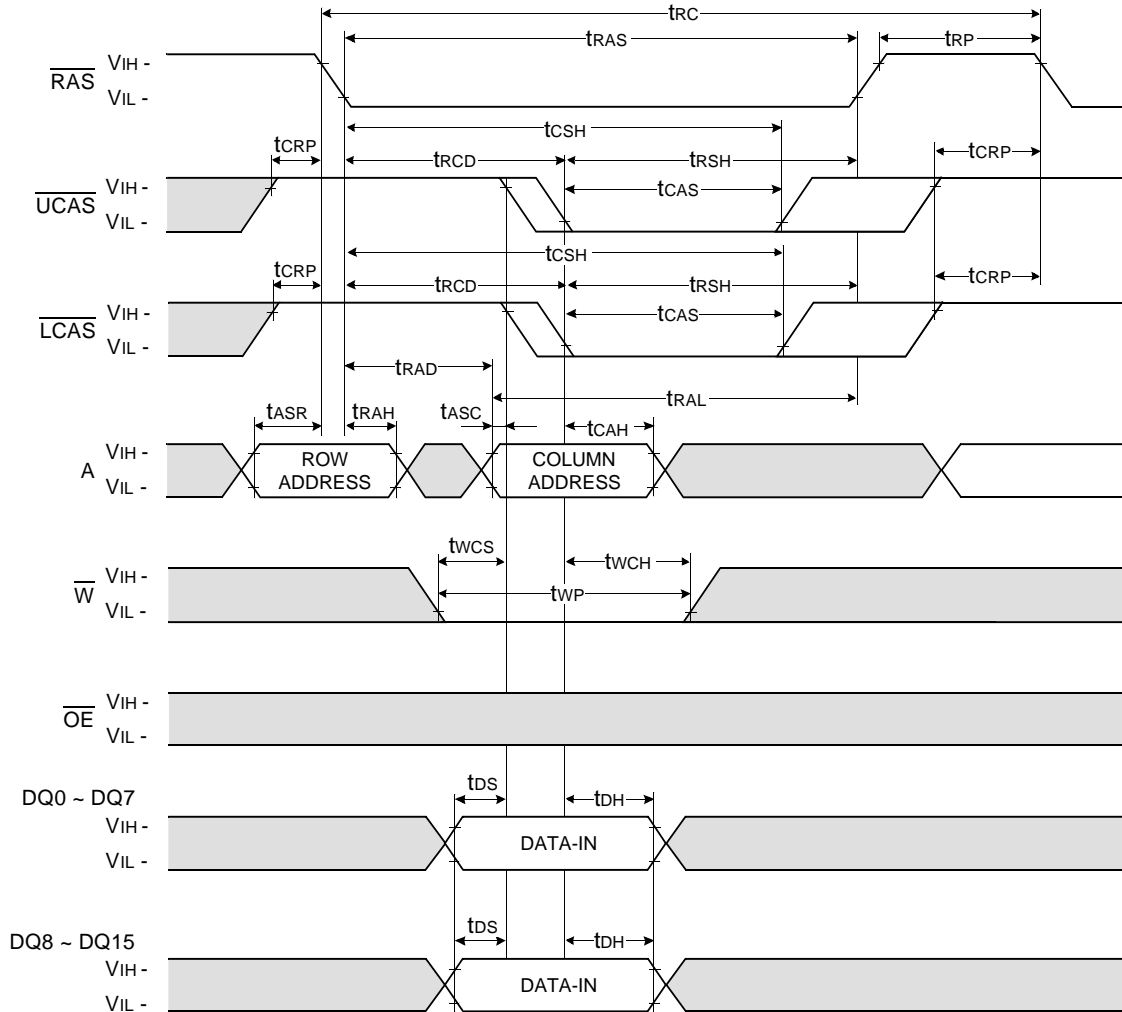
UPPER BYTE READ CYCLE

NOTE : DIN = OPEN



WORD WRITE CYCLE ( EARLY WRITE )

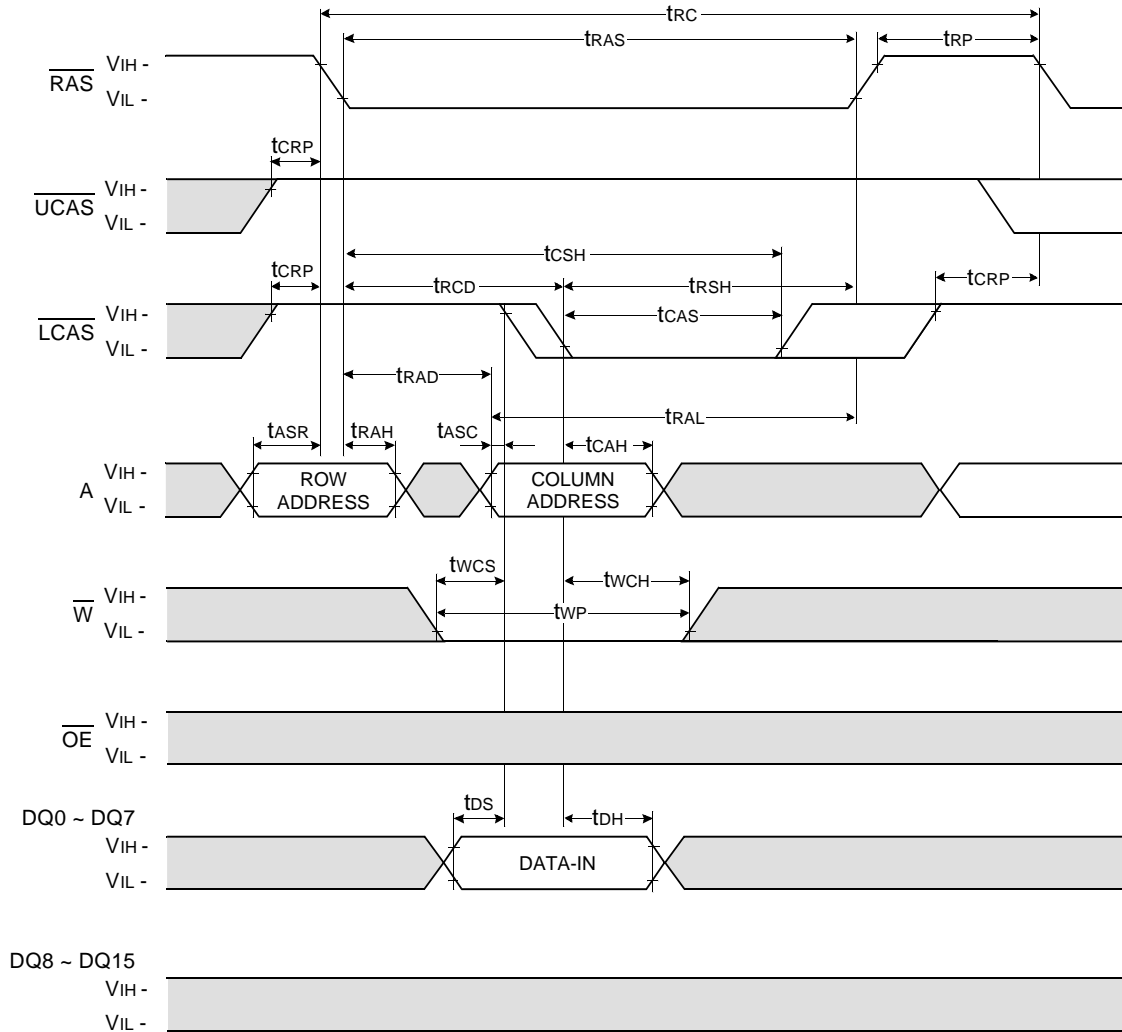
NOTE : DOUT = OPEN



Don't care  
 Undefined

LOWER BYTE WRITE CYCLE ( EARLY WRITE )

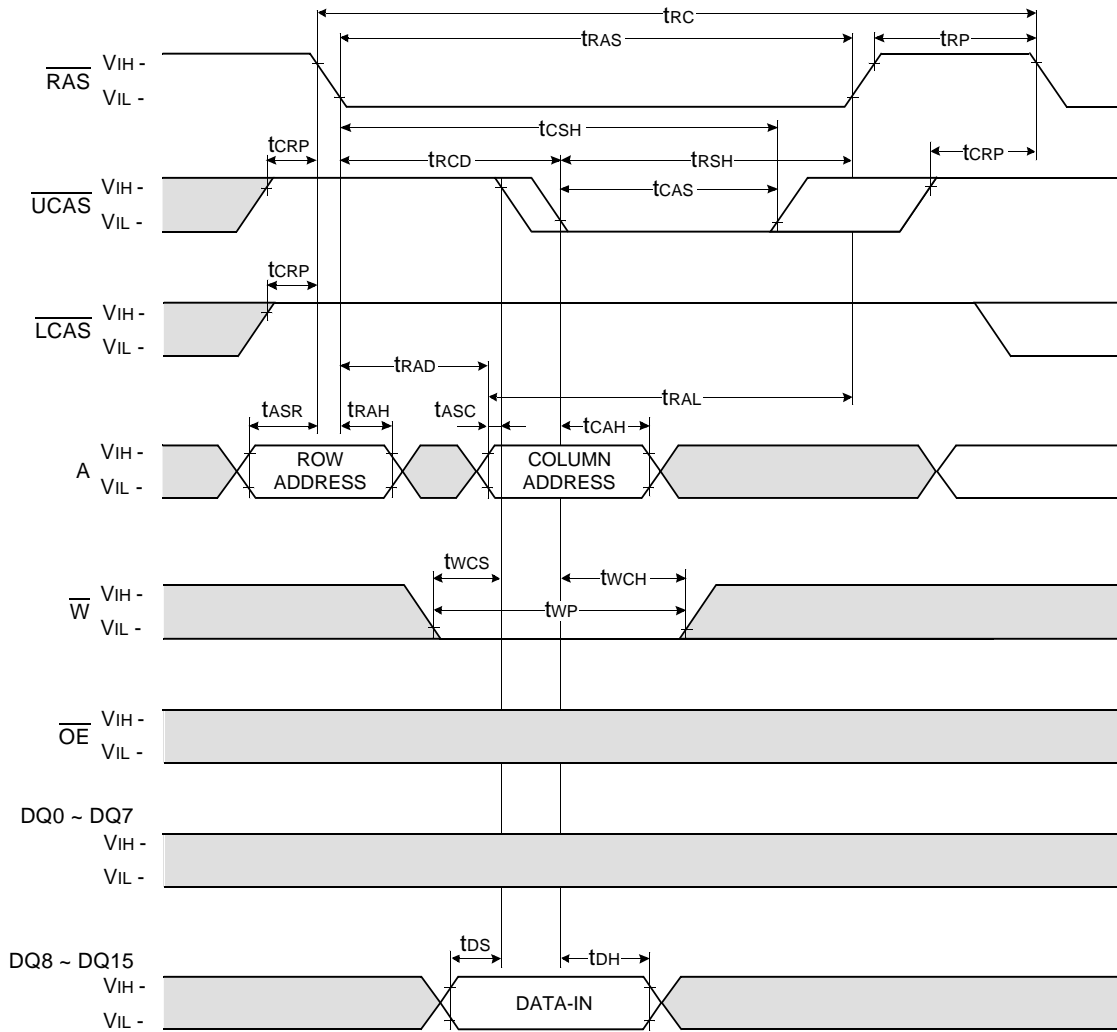
NOTE : DOUT = OPEN



Don't care  
 Undefined

UPPER BYTE WRITE CYCLE ( EARLY WRITE )

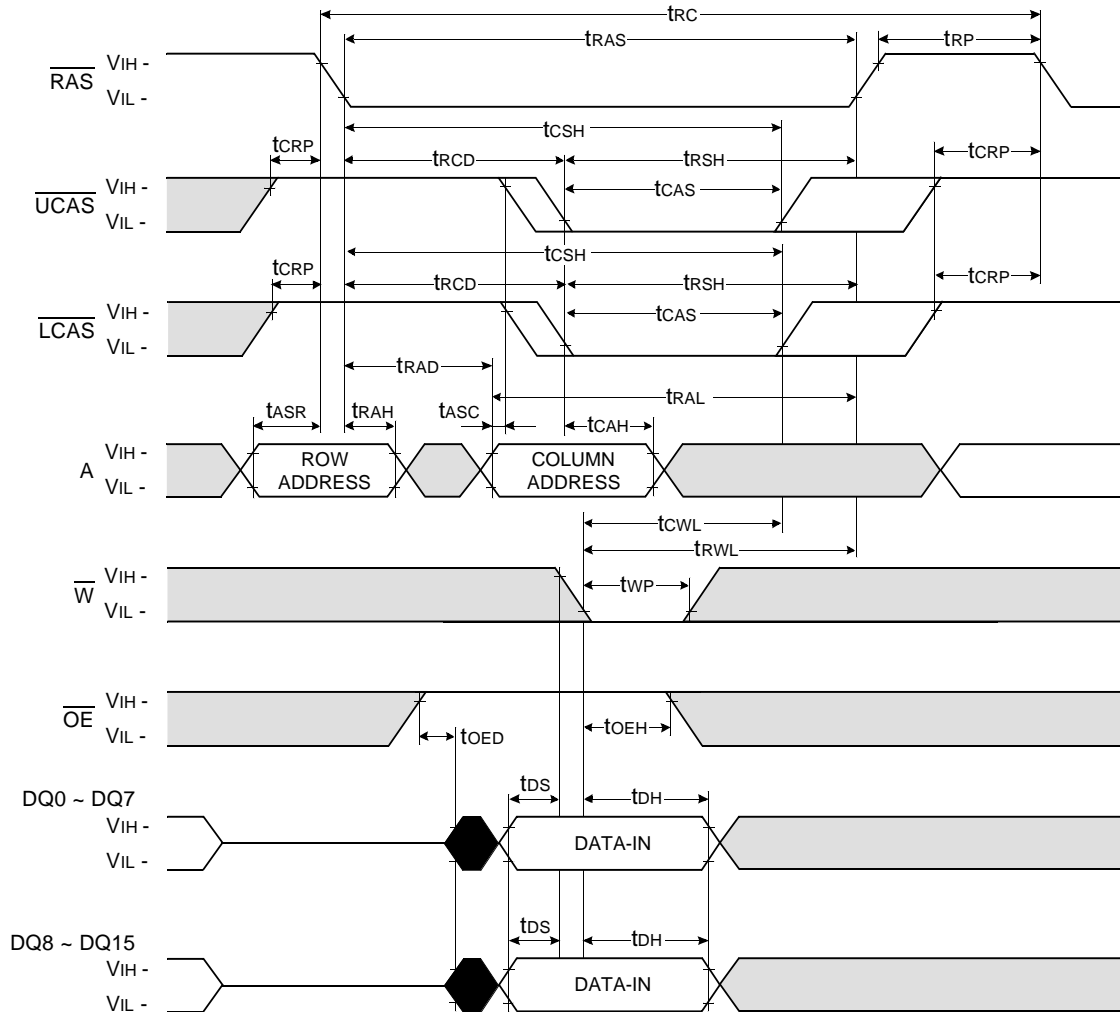
NOTE : DOUT = OPEN



Don't care  
 Undefined

WORD WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN

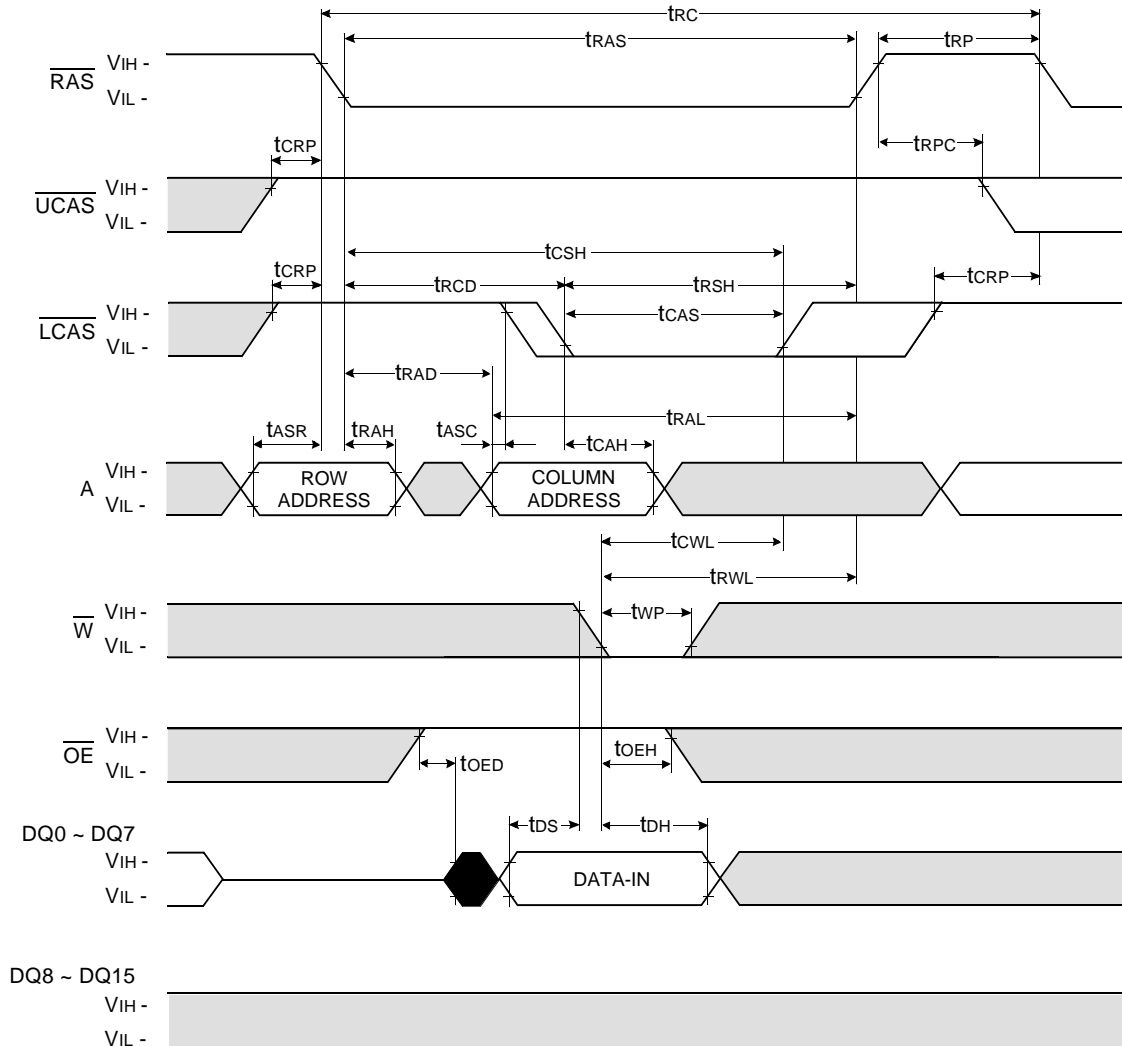


Don't care  
 Undefined



LOWER BYTE WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

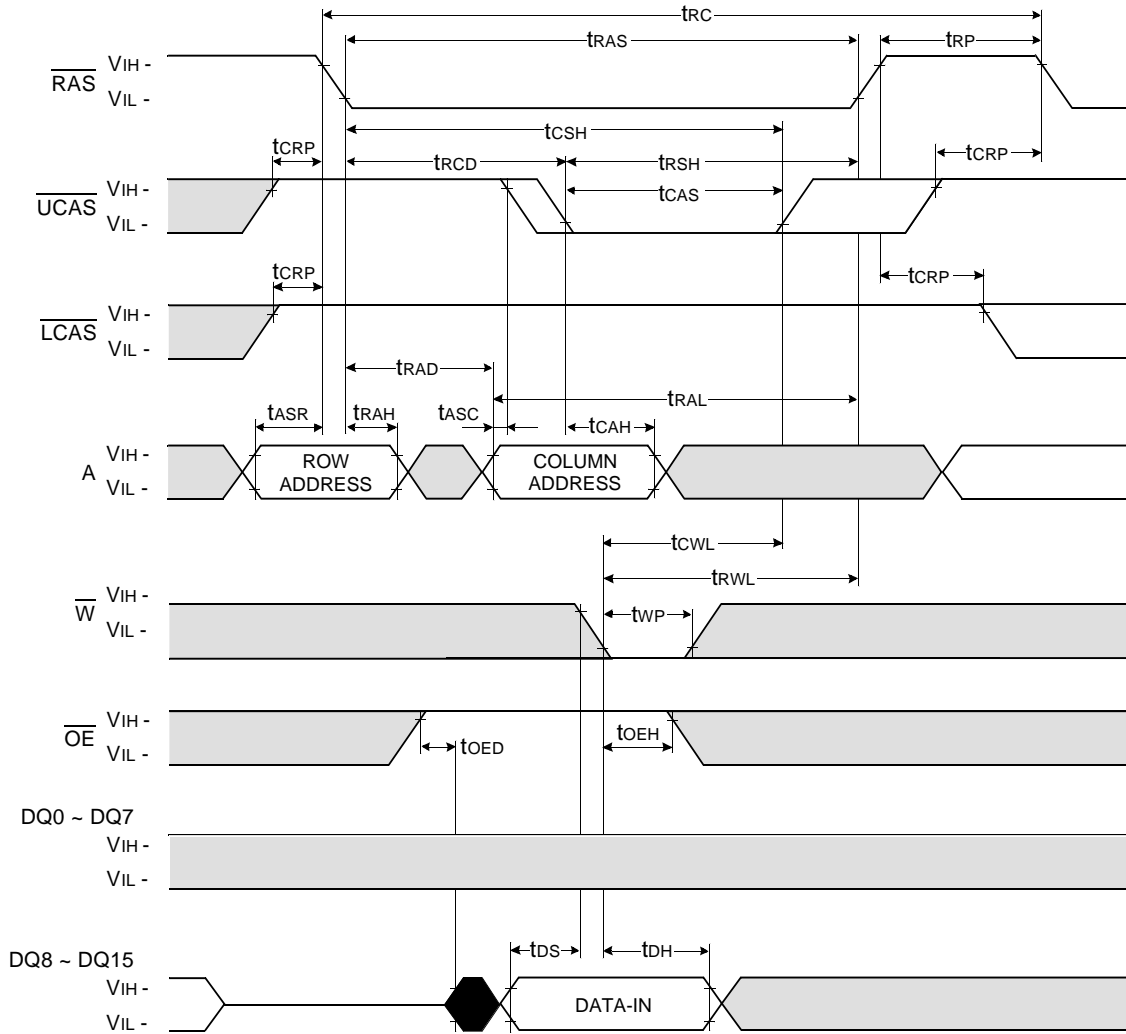
NOTE : DOUT = OPEN



Don't care  
 Undefined

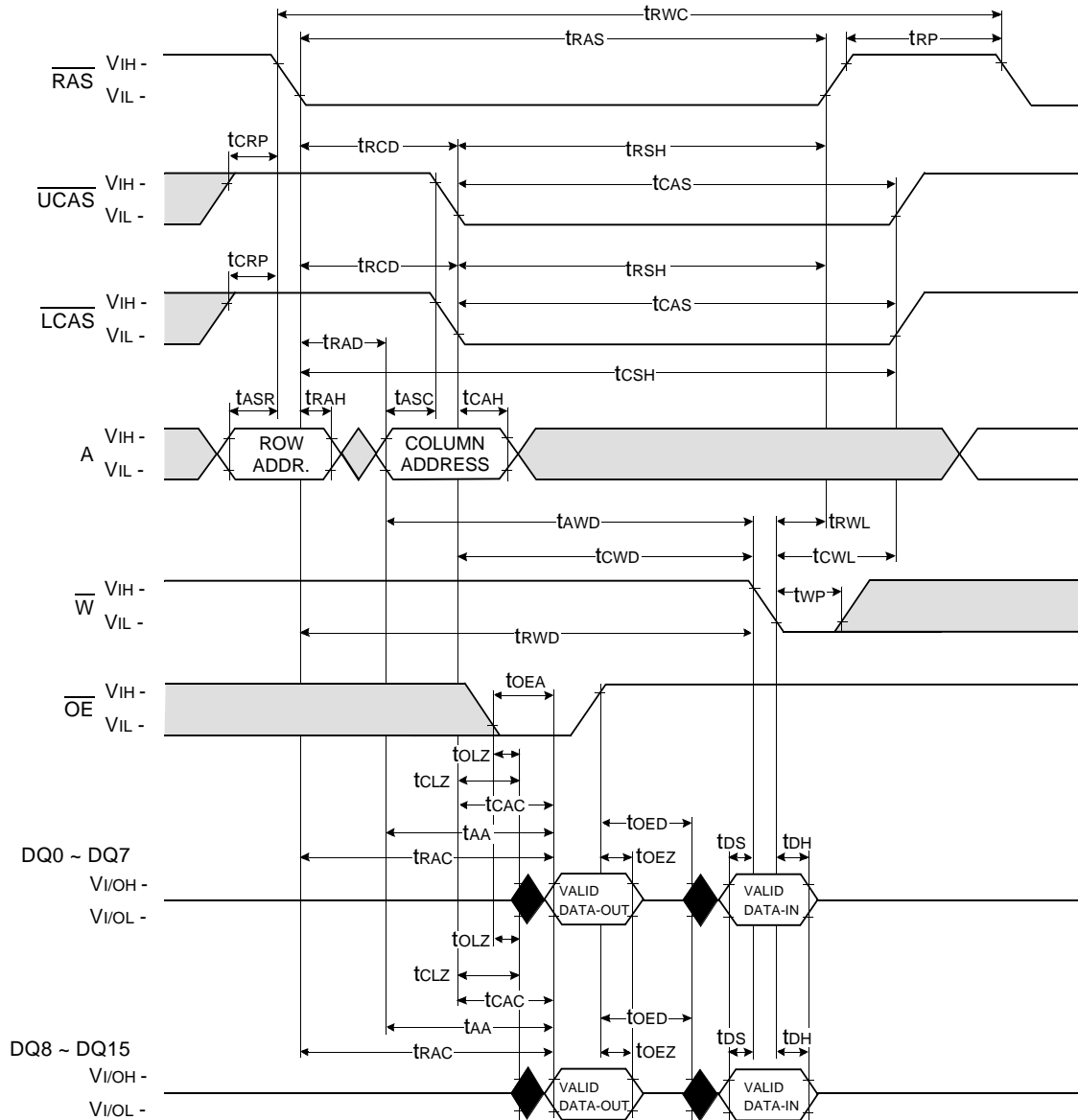
UPPER BYTE WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN



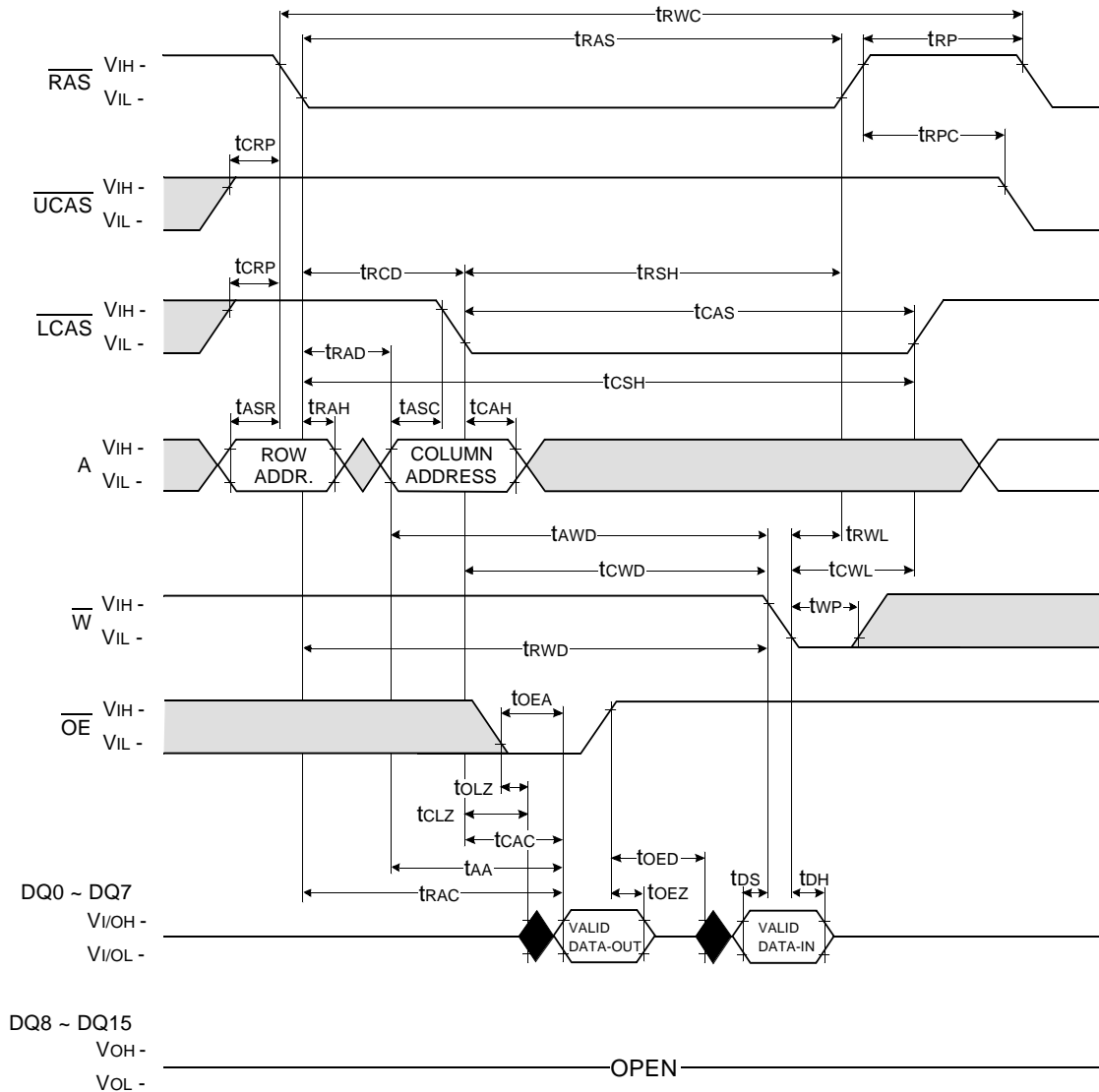
Don't care  
 Undefined

WORD READ - MODIFY - WRITE CYCLE



Don't care  
 Undefined

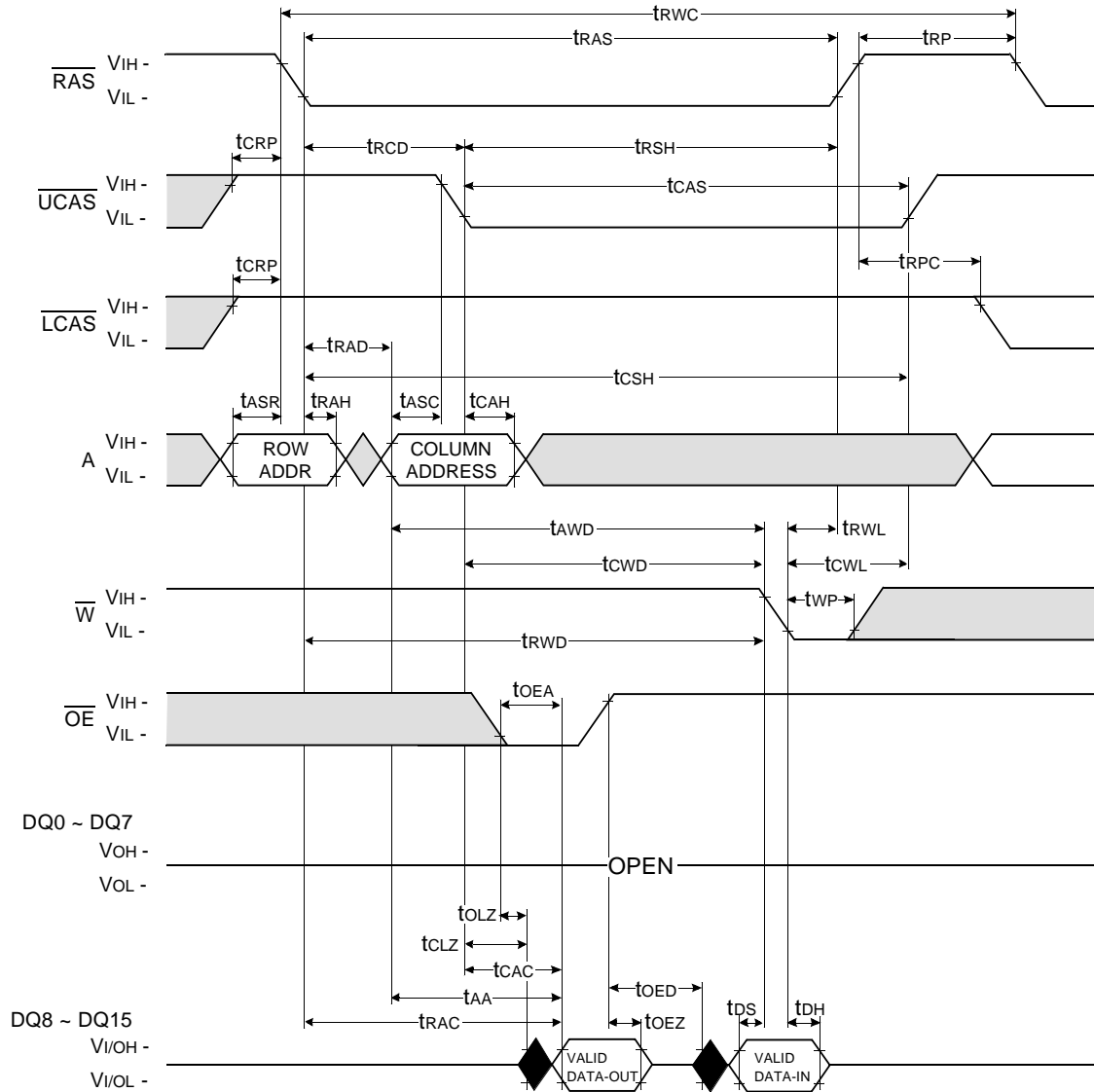
LOWER-BYTE READ - MODIFY - WRITE CYCLE



Don't care  
 Undefined



UPPER-BYTE READ - MODIFY - WRITE CYCLE



Don't care  
 Undefined



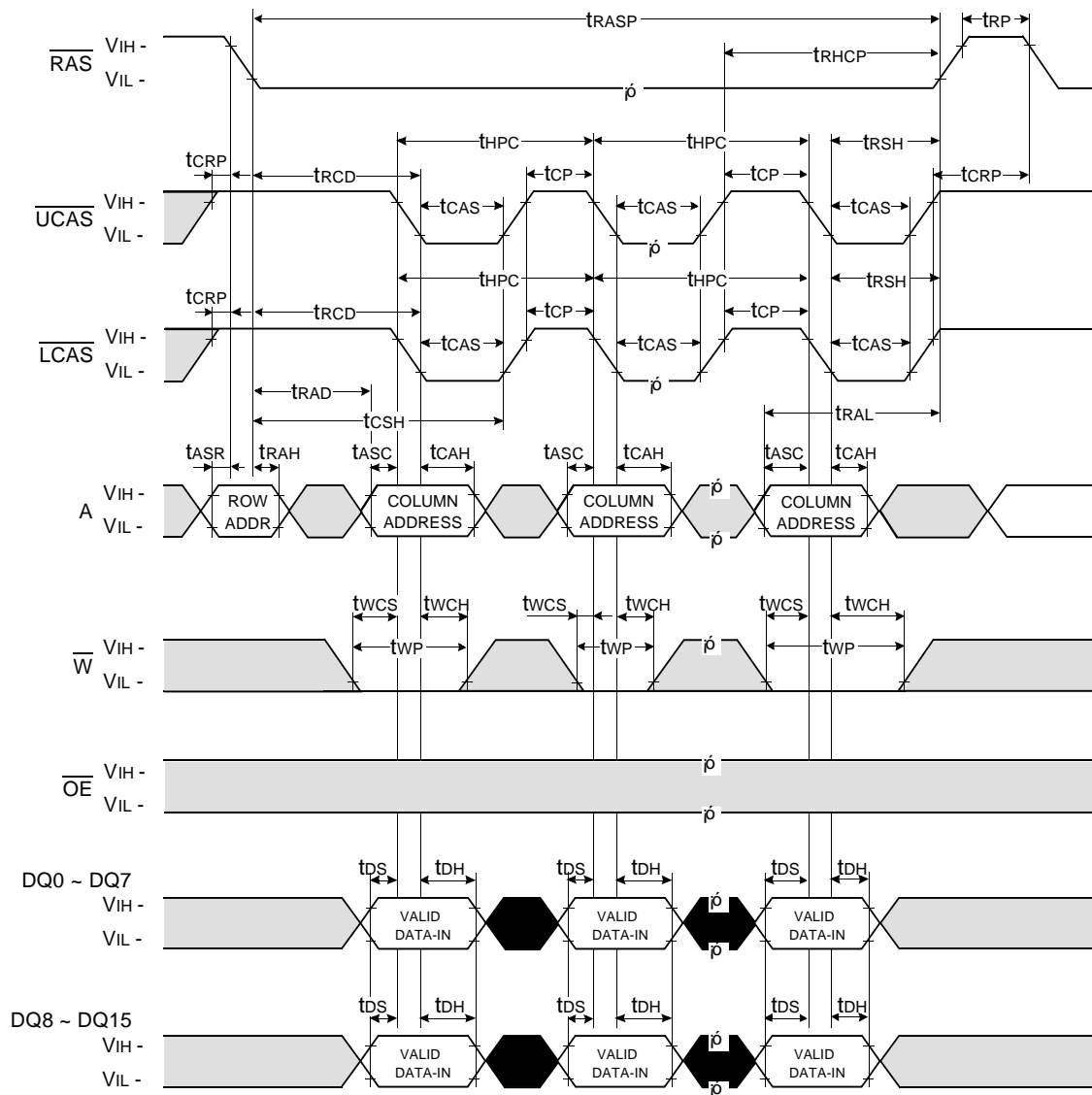






HYPER PAGE MODE WORD WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

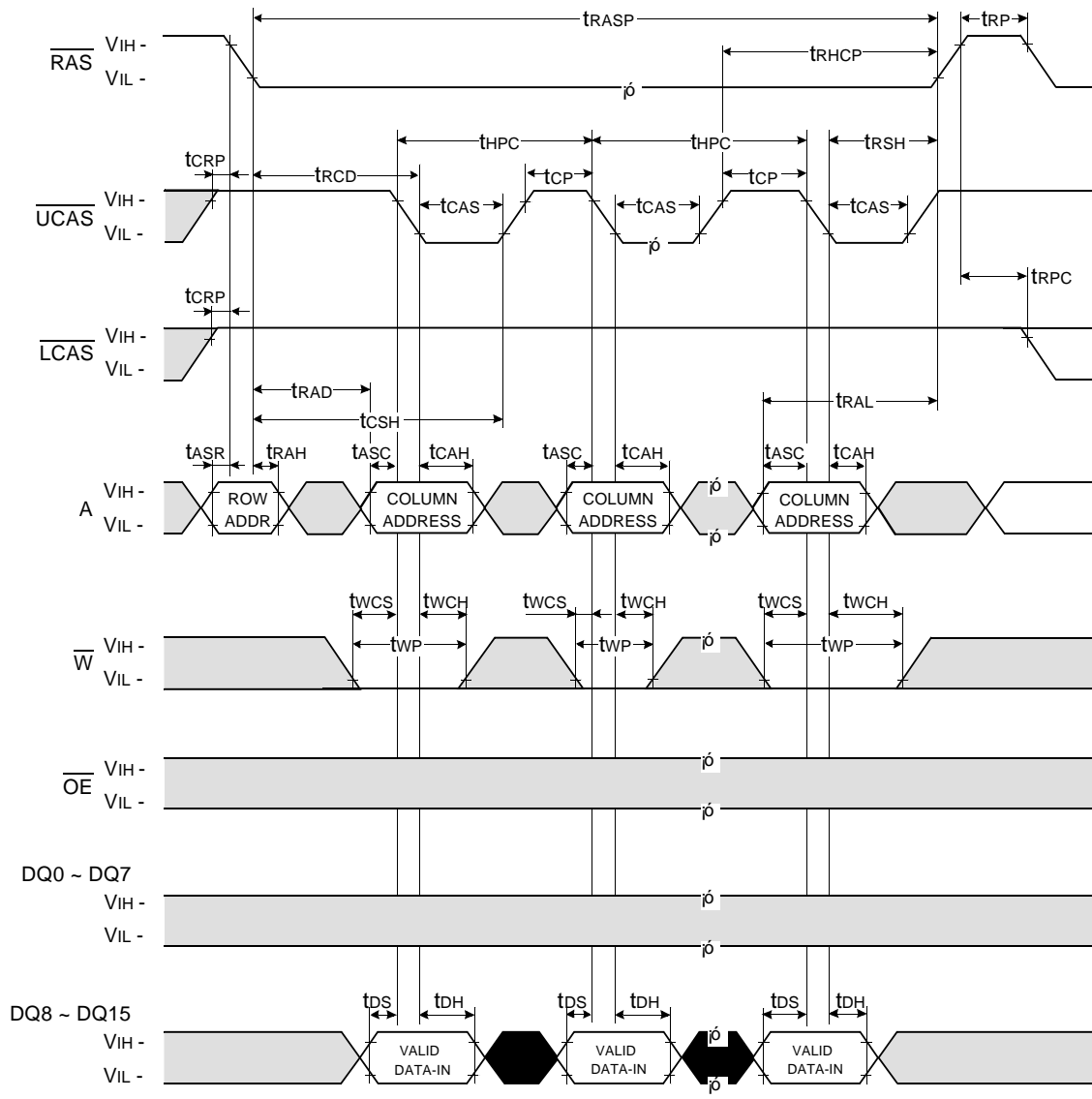


Don't care  
 Undefined



HYPER PAGE MODE UPPER BYTE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



Don't care  
 Undefined

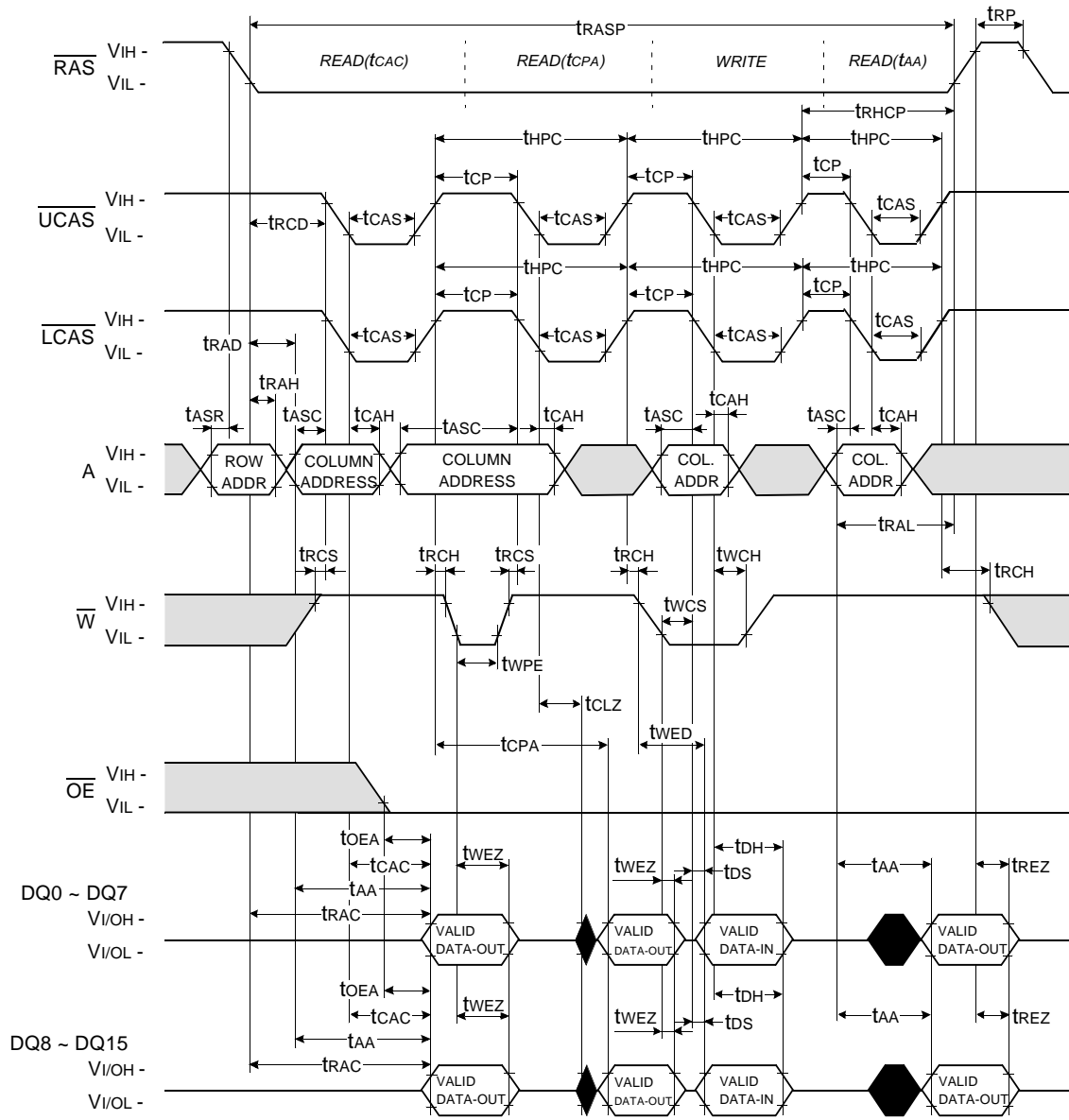








HYPER PAGE READ AND WRITE MIXED CYCLE



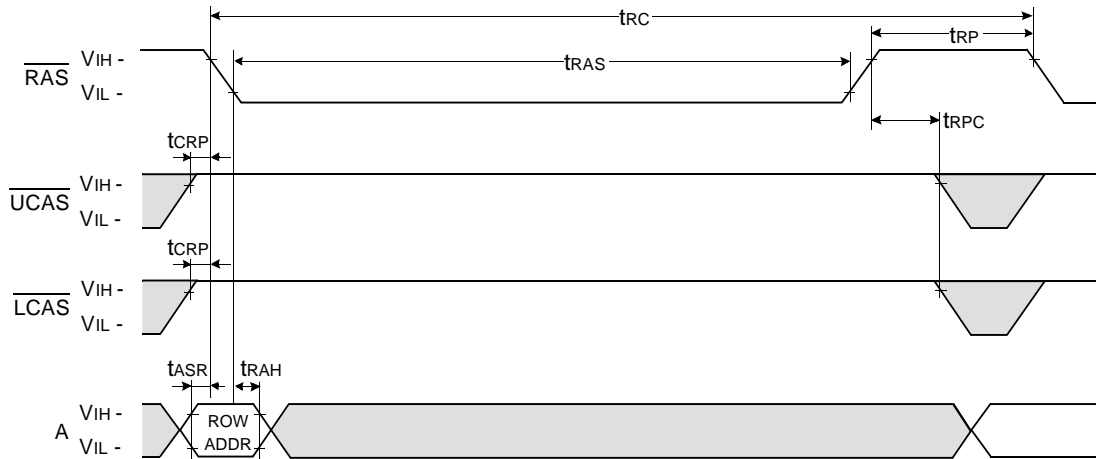
Don't care  
 Undefined



**RAS - ONLY REFRESH CYCLE**

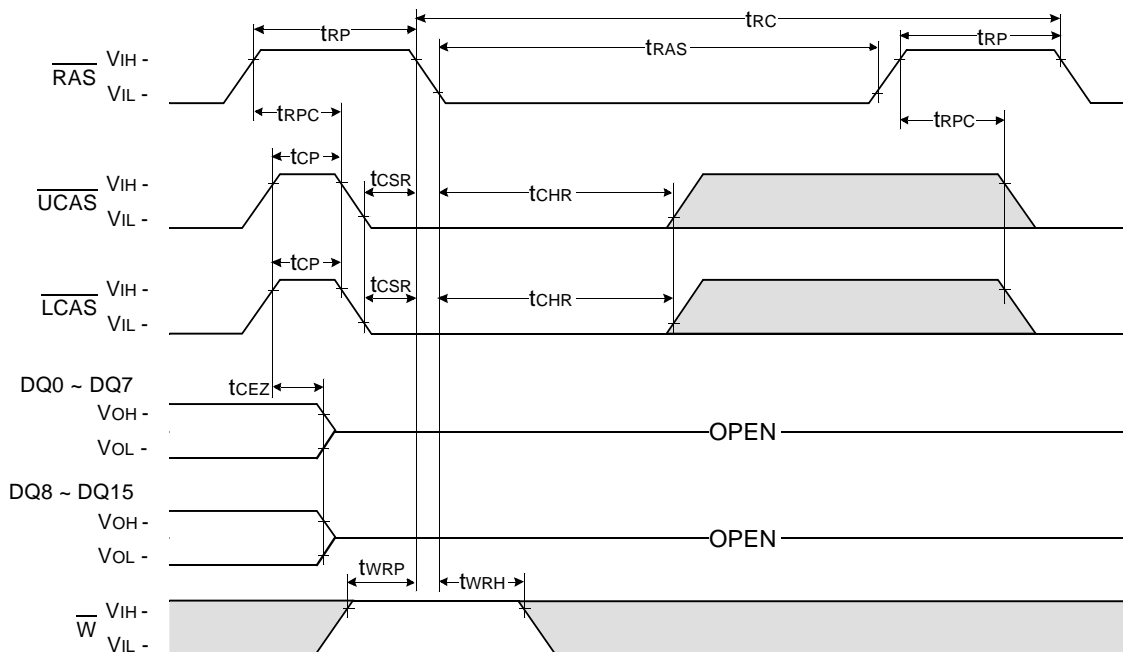
NOTE :  $\overline{W}$ ,  $\overline{OE}$ ,  $D_{IN}$  = Don't care

DOUT = OPEN



**CAS - BEFORE - RAS REFRESH CYCLE**

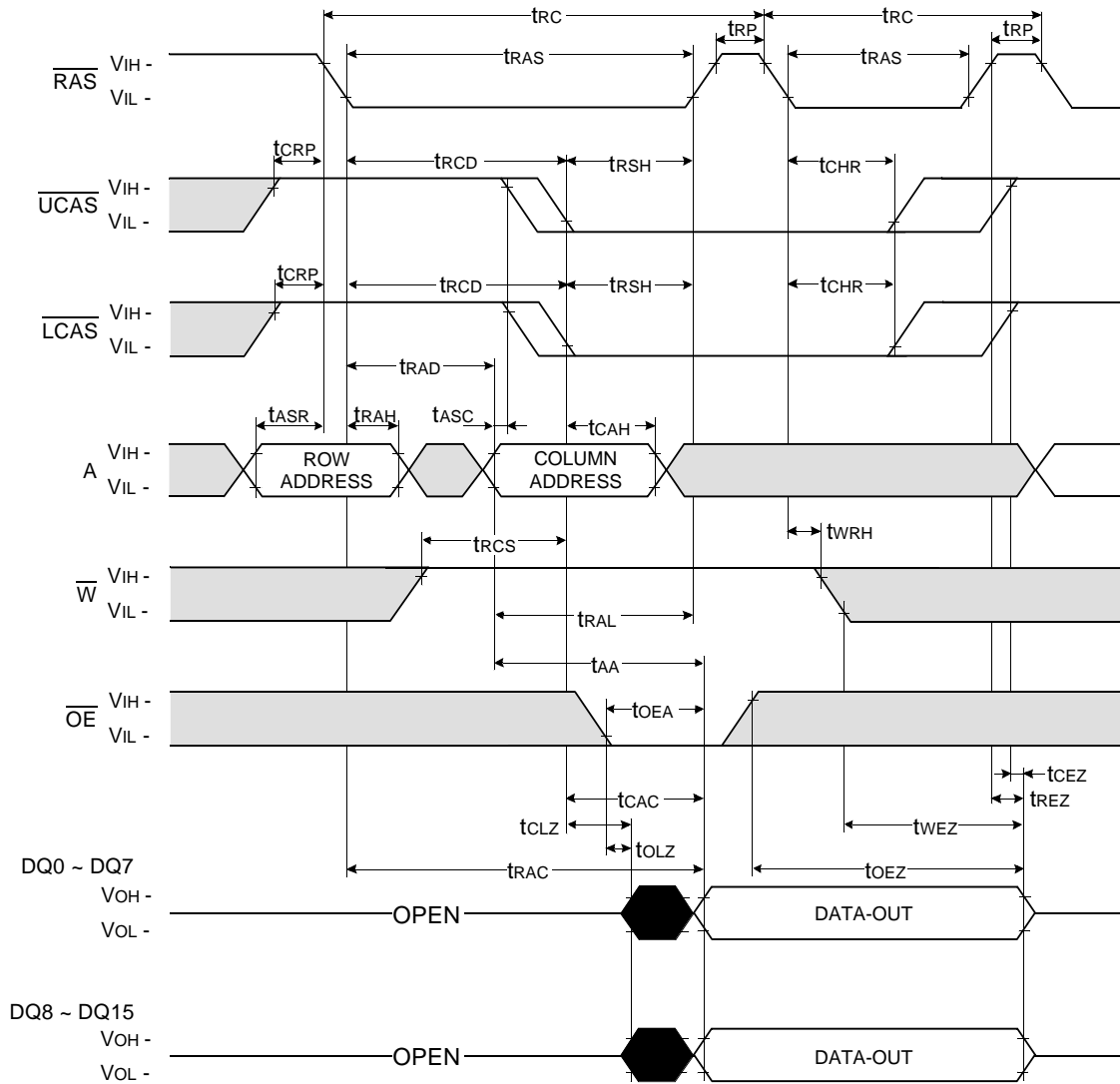
NOTE :  $\overline{OE}$ , A = Don't care



□ Don't care  
 ■ Undefined



HIDDEN REFRESH CYCLE ( READ )



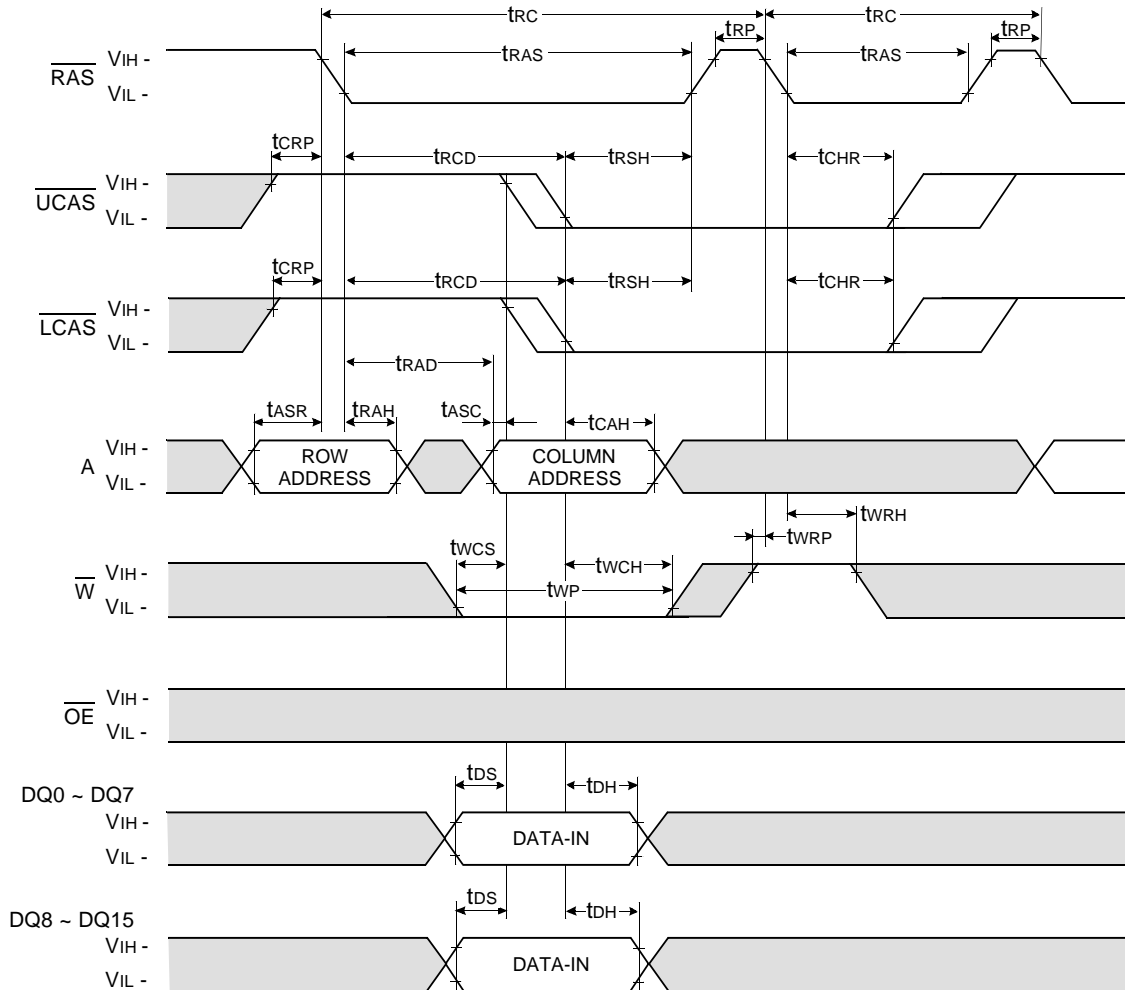
Don't care  
 Undefined

\* In Hidden refresh cycle of 64Mb A-die & B-die, when  $\overline{CAS}$  signal transits from Low to High, the valid data may be cut off.



HIDDEN REFRESH CYCLE ( WRITE )

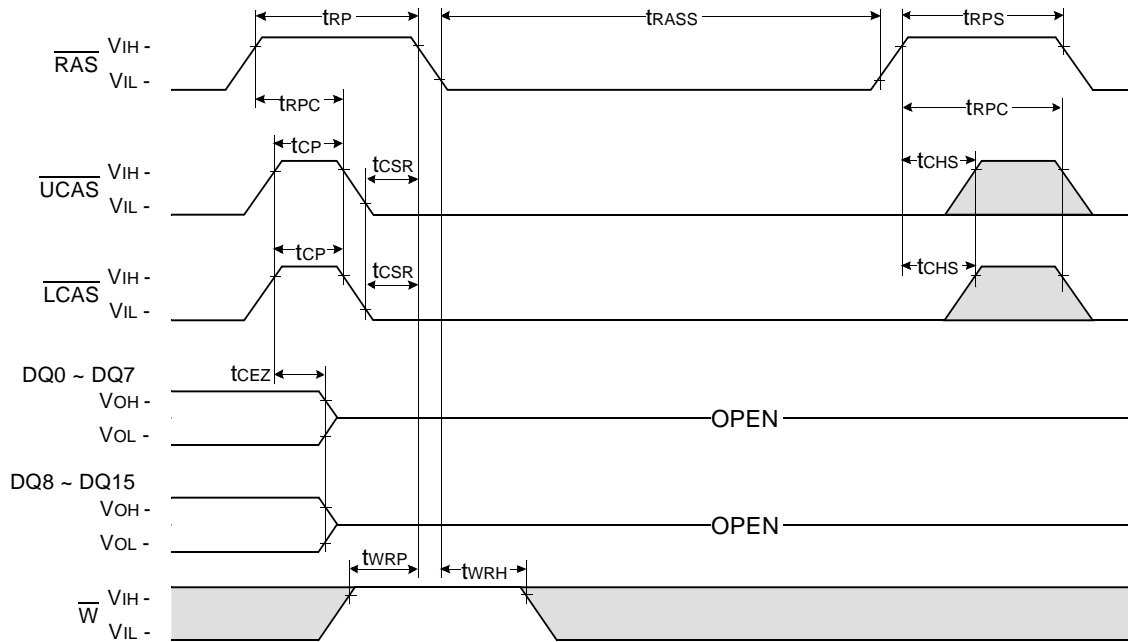
NOTE : DOUT = OPEN



Don't care  
 Undefined

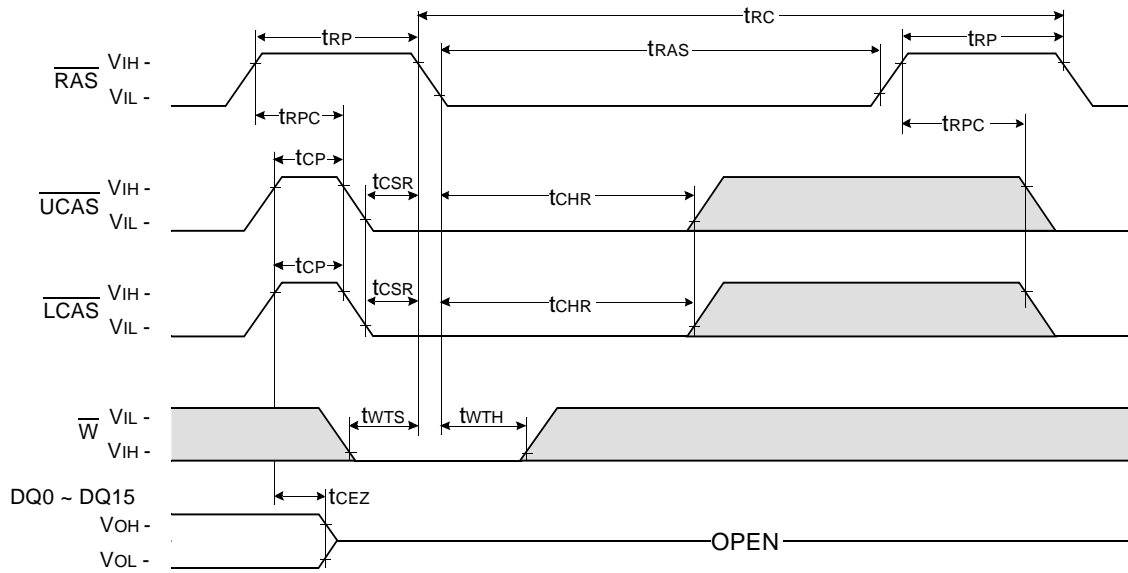
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



Don't care  
 Undefined

PACKAGE DIMENSION

