DDR SDRAM Specification
Version 0.2

Stacked 512Mb(x4) DDR SDRAM

Revision History

Version 0 (October, 2001)

- First version for internal review

Version 0.1(November,2001)

- Deleted tHZ/tLZ of DQS

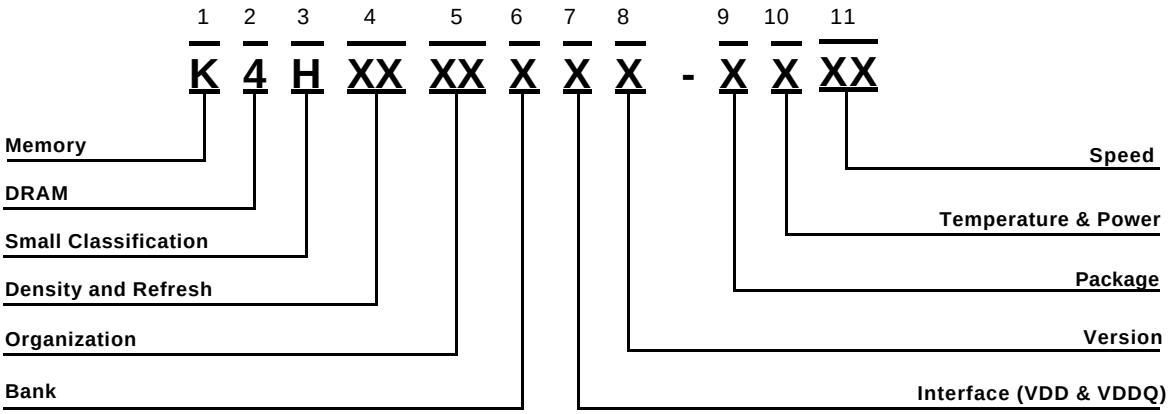
Version 0.2(November,2001)

- Updated DDR333 test specification
- Deleted typical current in IDD spec. table
- Included address and control input setup/hold time(tIS/tIH) at slow slew rate in DDR200/266 AC specification
- Deleted Exit self refresh to write command(tXSW) in DDR200/266 AC specification
- Changed unit of tMRD from tCK to ns at DDR333
- Rename tXSA(exit self refresh to bank active command) to tXSNR(exit self refresh to non read command) at DDR200/266
- Rename tXSR(exit self refresh to read command) to tXSRD at DDR200/266
- Rename tWPREH(DQS in hold time) to tWPRE at DDR200/266
- Rename tREF(Refresh interval time) to tREFI at DDR200/266
- Changed tWR value from 2tCK to 15ns.
- Added tDAL(tWR+tRP)
- Updated current value

Stacked 512Mb(x4) DDR SDRAM

General Information

Organization	166Mhz w/ CL=2.5	133Mhz w/ CL=2	133Mhz w/ CL=2.5	100Mhz w/ CL=2
128Mx4	K4H510638C-TCB3	K4H510638C-TCA2	K4H510638C-TCB0	K4H510638C-TCA0



1. SAMSUNG Memory : K

2. DRAM : 4

3. Small Classification

H : DDR SDRAM

4. Density & Refresh

64 : 64M 4K/64ms
28 : 128M 4K/64ms
56 : 256M 8K/64ms
51 : 512M 8K/64ms
1G : 1G 16K/32ms

5. Organization

04 : x4
08 : x8
16 : x16
32 : x32
06 : stacked x4

6. Bank

3 : 4 Bank

7. Interface (VDD & VDDQ)

8: SSTL-2(2.5V, 2.5V)

8. Version

M : 1st Generation
A : 2nd Generation
B : 3rd Generation
C : 4th Generation
D : 5th Generation
E : 6th Generation

9. Package

T : TSOP2 (400mil x 875mil)

10. Temperature & Power

C : (Commercial, Normal)
L : (Commercial, Low)

11. Speed

A0 : 10ns@CL2
A2 : 7.5ns@CL2
B0 : 7.5ns@CL2.5

Stacked 512Mb(x4) DDR SDRAM

Key Features

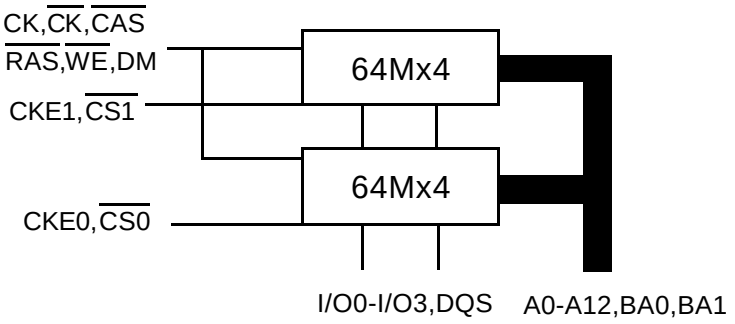
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
  - -. Read latency 2, 2.5 (clock)
  - -. Burst length (2, 4, 8)
  - -. Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe
- Edge aligned data output, center aligned data input
- LDM,UDM/DM for write masking only
- Auto & Self refresh
- 7.8us refresh interval(8K/64ms refresh)
- Maximum burst refresh cycle : 8
- 66pin TSOP II package

Operating Frequencies

	- B3(DDR333)	- A2(DDR266A)	- B0(DDR266B)	- A0(DDR200)
Speed @CL2	133MHz	133MHz	100MHz	100MHz
Speed @CL2.5	166MHz	133MHz	133MHz	-
DLL jitter	±0.7ns	±0.75ns	±0.75ns	±0.8ns

*CL : Cas Latency

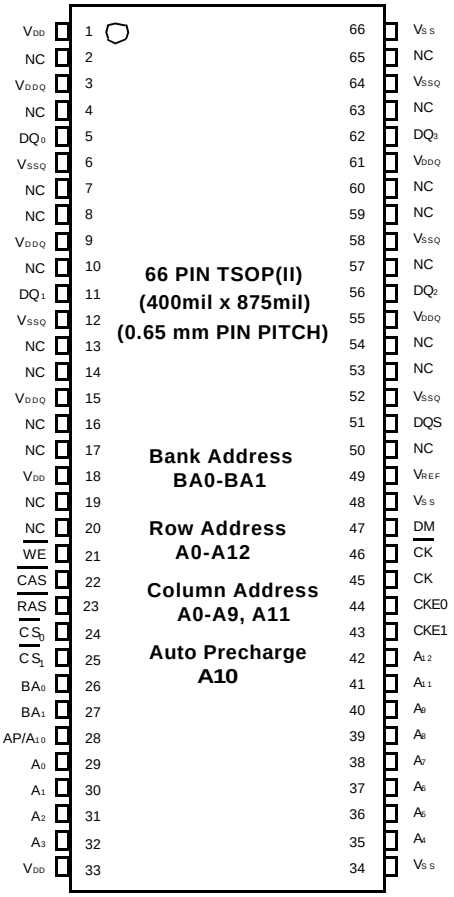
Functional Block Diagram



*Statek' s stacking technology is Samsung' s stacking technology of choice.

Stacked 512Mb(x4) DDR SDRAM

Package Pinout



Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/$\overline{CK}$.
CKE0,CKE1	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up.
$\overline{CS0}$, $\overline{CS1}$	Input	Chip Select : $\overline{CS}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
LDM,(U)DM	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM correspons to the data on DQ8-DQ15.
BA0, BA1	Input	Bank Addres Inputs : BA0 and BA1 define to which bank ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs : Provide the row address for ACTIVE commands, the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Data Input/Output : Data bus
(L)DQS,UDQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
NC	-	No Connect : No internal electrical connection is present.
$V_{DD}Q$	Supply	DQ Power Supply : +2.5V ± 0.2V.
$V_{SS}Q$	Supply	DQ Ground.
V_{DD}	Supply	Power Supply : +2.5V ± 0.2V (device specific).
V_{SS}	Supply	Ground.
V_{REF}	Input	SSTL_2 reference voltage.

3. Functional Description

3.1 Simplified State Diagram

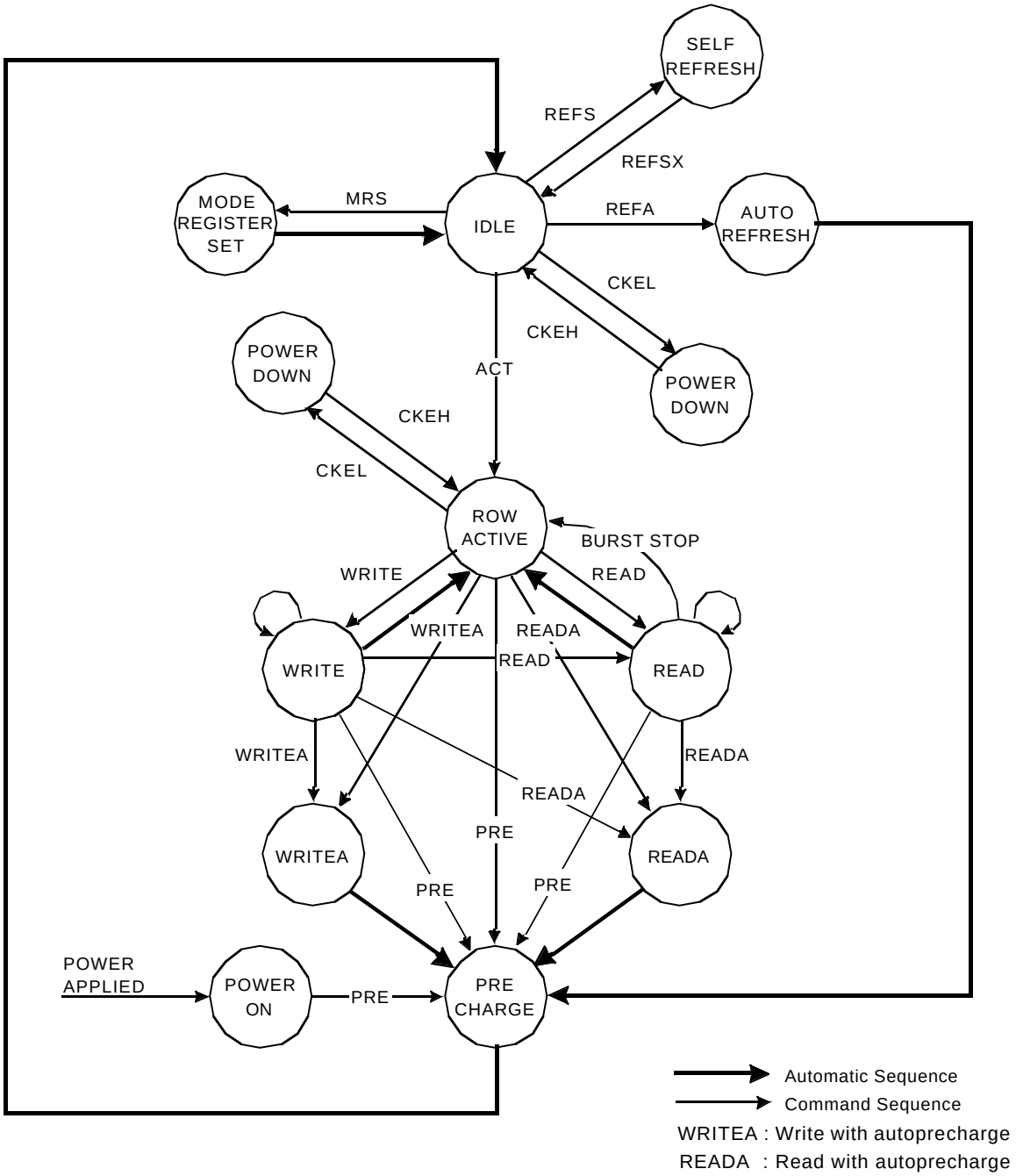


Figure 3. State diagram

3.2 Basic Functionality

3.2.1 Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE at a low state(all other inputs may be undefined.)
   - Apply V_{DD} before or at the same time as $V_{DD}Q$.
   - Apply $V_{DD}Q$ before or at the same time as V_{TT} & Vref.

No power sequencing is specified during power up or power down given the following criteria:

- V_{DD} and $V_{DD}Q$ are driven from a single power converter output, and
- V_{TT} is limited to 1.44V (reflecting $V_{DD}Q$(max)/2 + 50mV V_{REF} variation +40m V V_{TT} variation), and
- V_{REF} tracks $V_{DD}Q$/2, and
- A minimum resistance of 42 ohms(22 ohm series resistor + 22 ohm parallel resistor 5% tolerance) limits the input current from the V_{TT} supply into any pin.

If the above criteria cannot be met by the system design, the following table must be adhered to during power up:

Voltage Description	Sequencing	Voltage Relationship to avoid latch-up
VDDQ	After or with VDD	<VDD + 0.3V
VTT	After or with VDDQ	< VDDQ +0.3V
VREF	After or with VDDQ	<VDDQ +0.3V

2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock(CK, $\overline{CK}$), apply NOP & take CKE high.
4. Issue precharge commands for all banks of the device.
5. Issue EMRS to enable DLL.(To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0)

*1 7. Issue precharge commands for all banks of the device.

8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command with low to A8 to initialize device operation.

*1 Sequence of 6 & 7 is regardless of the order.

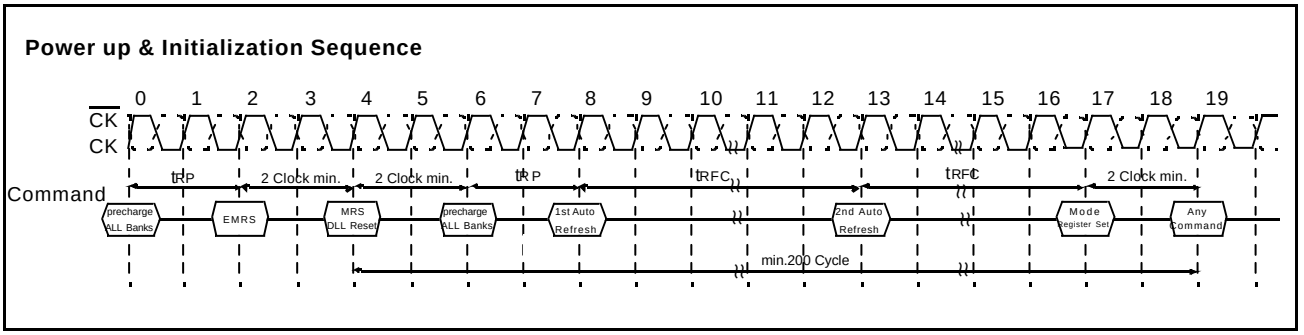
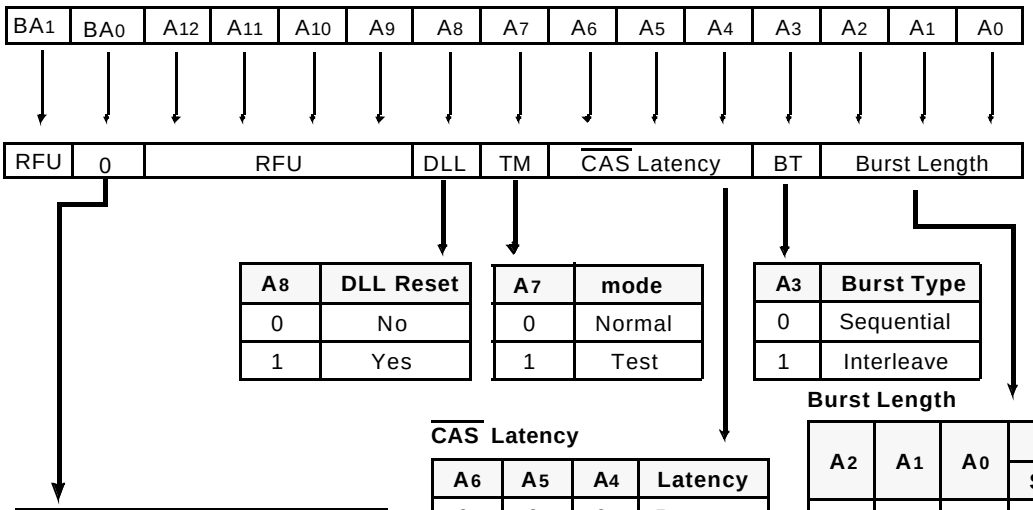


Figure 4. Power up and initialization sequence

3.2.2 Mode Register Definition

3.2.2.1 Mode Register Set(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on CS, RAS, CAS, WE and BA0(The DDR SDRAM should be in all bank pre-charge with CKE already high prior to writing into the mode register). The states of address pins A0 ~ A12 in the same cycle as CS, RAS, CAS, WE and BA0 going low are written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst lengths, addressing modes and CAS latencies.



BA0	An ~ A0
0	(Existing)MRS Cycle
1	Extended Funtions(EMRS)

* RFU(Reserved for future use) should stay "0" during MRS cycle.

A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	(3)
1	0	0	Reserve
1	0	1	(1.5)
1	1	0	2.5
1	1	1	Reserve

Burst Length

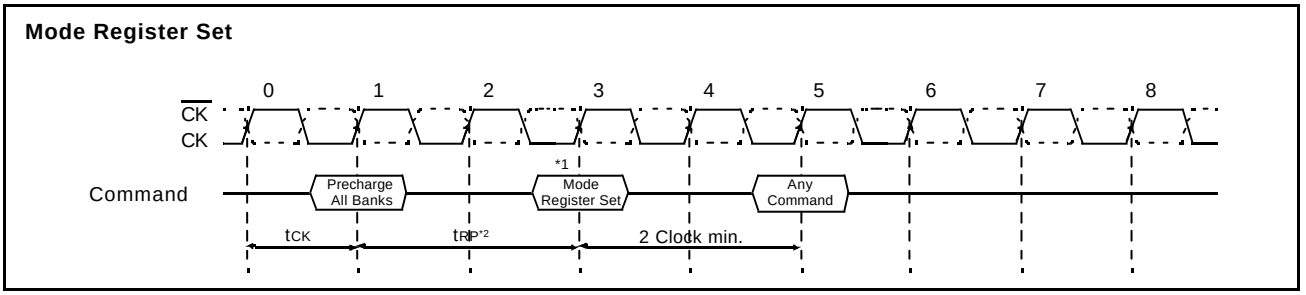
A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

Figure 5. Mode Register Set

Burst Address Ordering for Burst Length

Burst Length	Starting Address(A2, A1, A0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Table 4. Burst address ordering for burst length



*1 : MRS can be issued only at all bank precharge state.
*2 : Minimum t_{RP} is required to issue MRS command.

Figure 6. Mode Register Set sequence

3.2.2.2 Extended Mode Register Set(EMRS)

The extended mode register stores the data for enabling or disabling DLL, $\overline{QFC}$ and selecting output driver size. The default value of the extended mode register is not defined, therefore the extened mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11 and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.

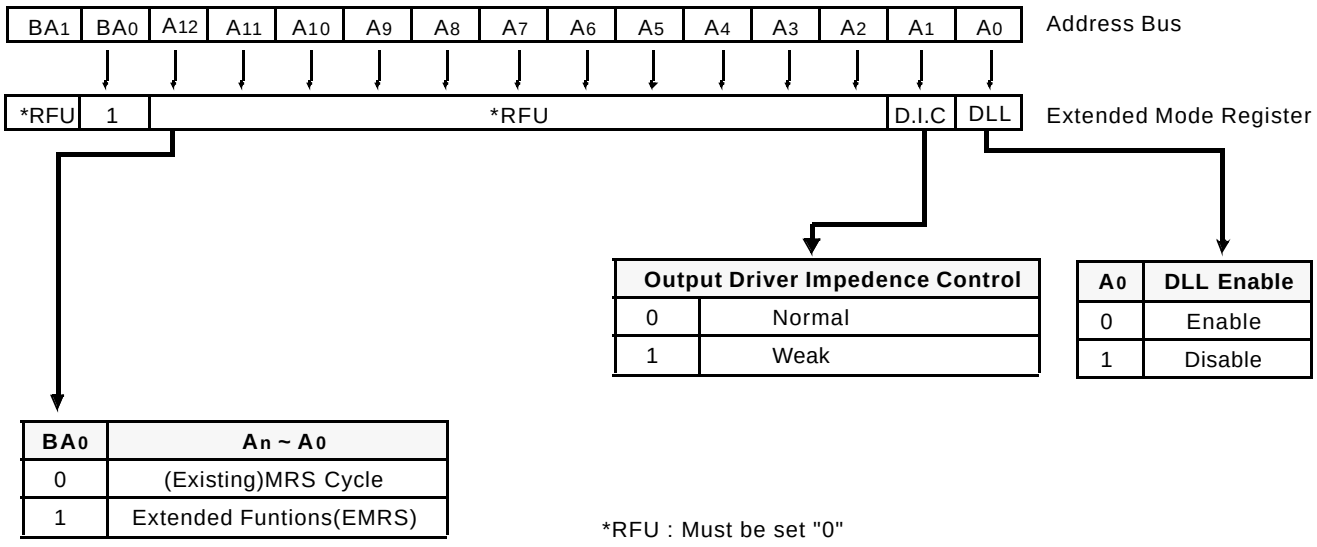


Figure 7. Extend Mode Register set

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returing to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Samsung supports a weak driver strength option, intended for lighter load and/or point-to-point environments. I-V curves for the normal drive strength and weak drive strength are included in 11.1~2 of this document.

3.2.3 Precharge

The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses(BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied until the precharge command can be issued. After tRP from the precharge, an active command to the same bank can be initiated.

Bank Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

Table 5. Bank selection for precharge by Bank address bits

3.2.4 No Operation(NOP) & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode DDR SDRAM should ignore all the control inputs. The DDR SDRAMs are put in NOP mode when $\overline{CS}$ is active and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP the device should finish the current operation when this command is issued.

3.2.5 Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock(CK). The DDR SDRAM has four independent banks, so two Bank Select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time(tRCD min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(tRRD min).

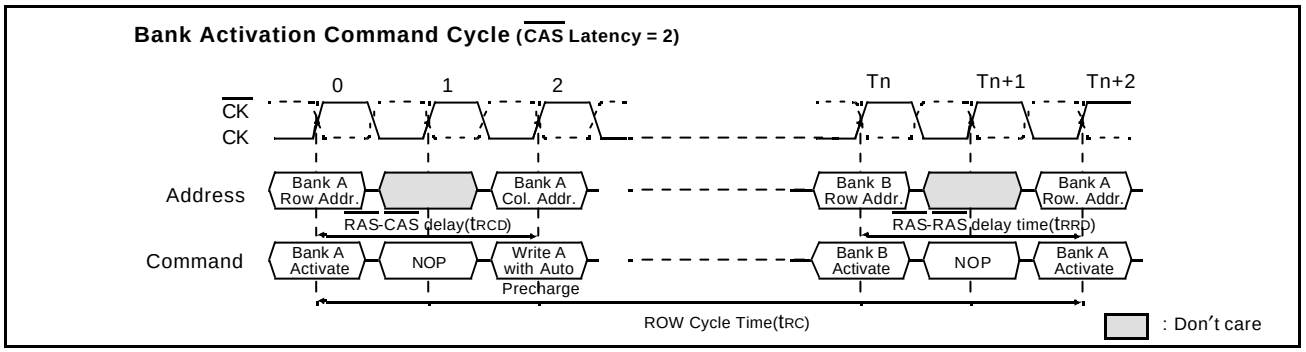


Figure 8. Bank activation command cycle timing

3.2.6 Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

3.2.7 Write Bank

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

3.3 Essential Functionality for DDR SDRAM

The essential functionality that is required for the DDR SDRAM device is described in this chapter

3.3.1 Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock(CK) after tRCD from the bank activation. The address inputs (A0~A9) determine the starting address for the Burst. The Mode Register sets type of burst(Sequential or interleave) and burst length(2, 4, 8). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe(DQS) adopted by DDR SDRAM until the burst length is completed.

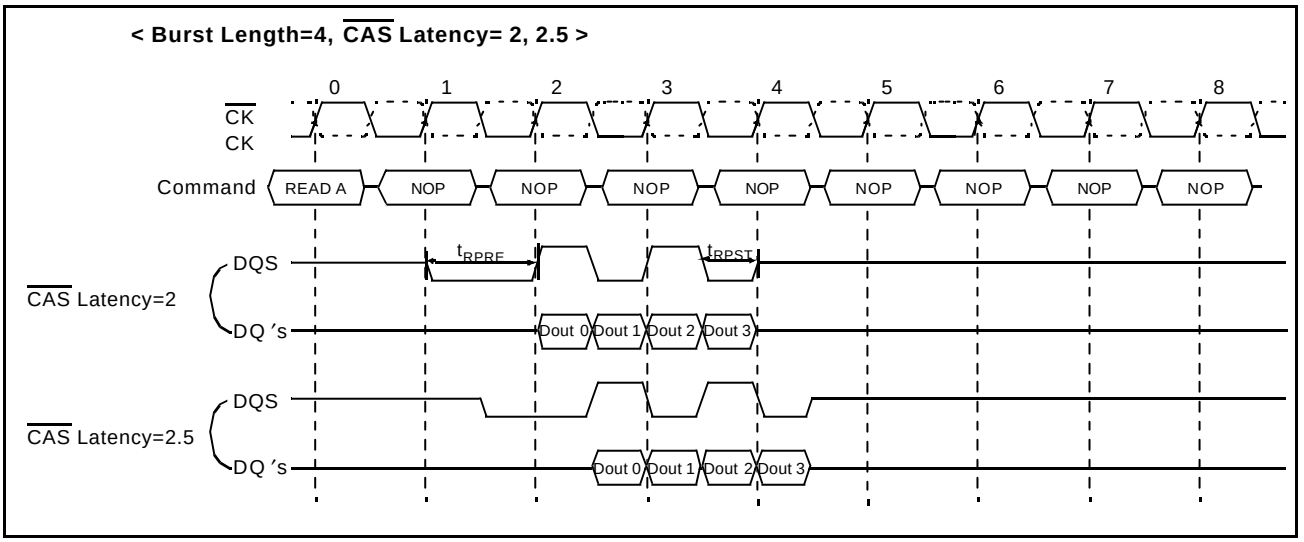


Figure 9. Burst read operation timing

3.3.2 Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock(CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS(Data-in setup time) prior to data strobe edge enabled after tDQSS from the rising edge of the clock(CK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

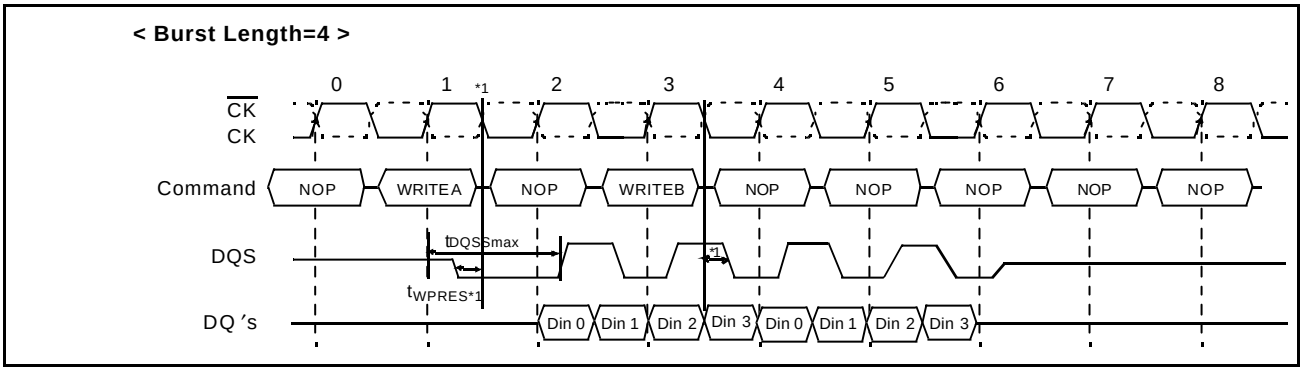


Figure 10. Burst write operation timing

1. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

3.3.3 Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.

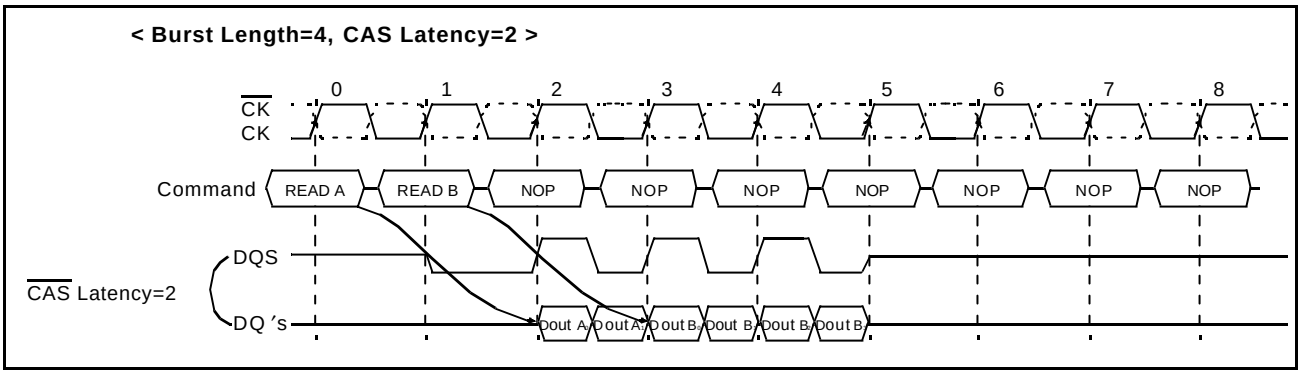


Figure 11. Read interrupted by a read timing

3.3.4 Read Interrupted by a Write & Burst Stop

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burst stop command must be applied at least 2 clock cycles for CL=2 and at least 3 clock cycles for CL=2.5 before the Write command.

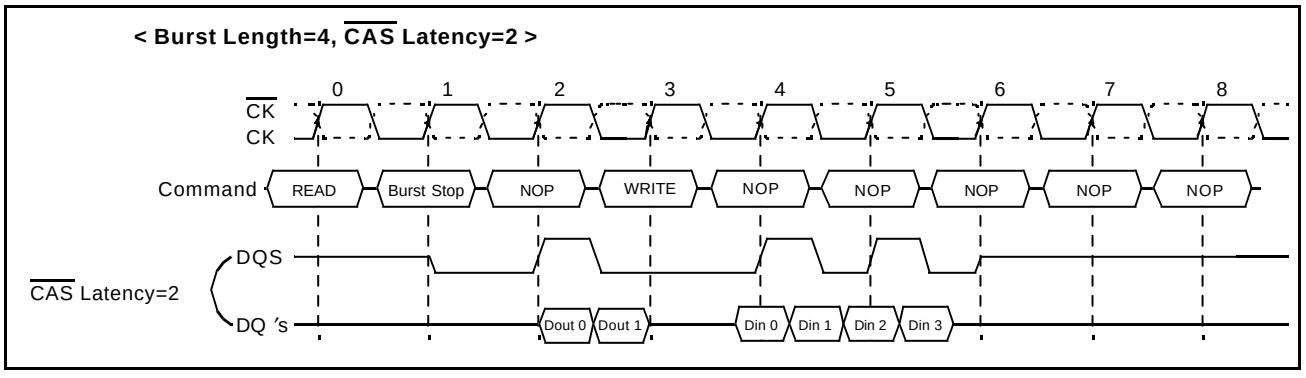


Figure 12. Read interrupted by a write and burst stop timing.

The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU(CL) [CL is the CAS Latency and RU means round up to the nearest integer].
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

3.3.5 Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the CAS latency.

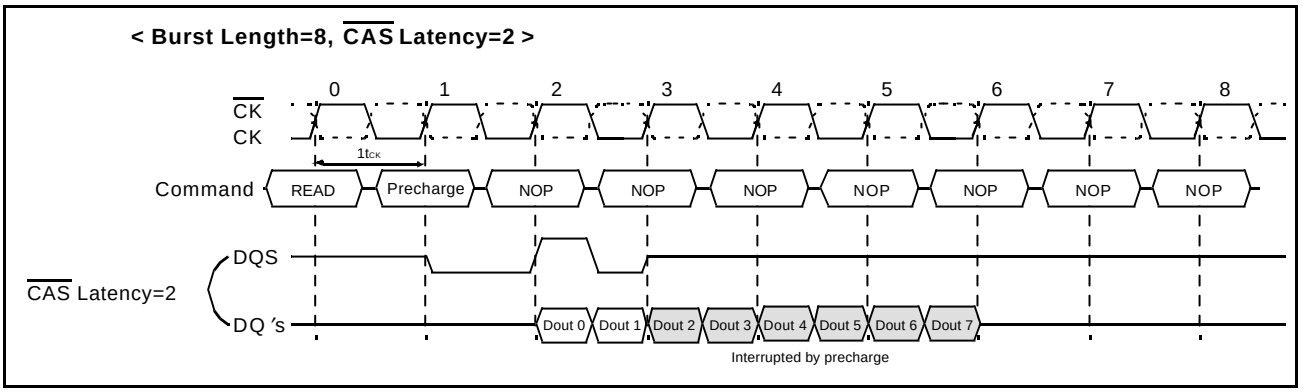


Figure 13. Read interrupted by a precharge timing

When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.
3. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP where tRP begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.
4. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a *rising* clock edge).

In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

3.3.6 Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

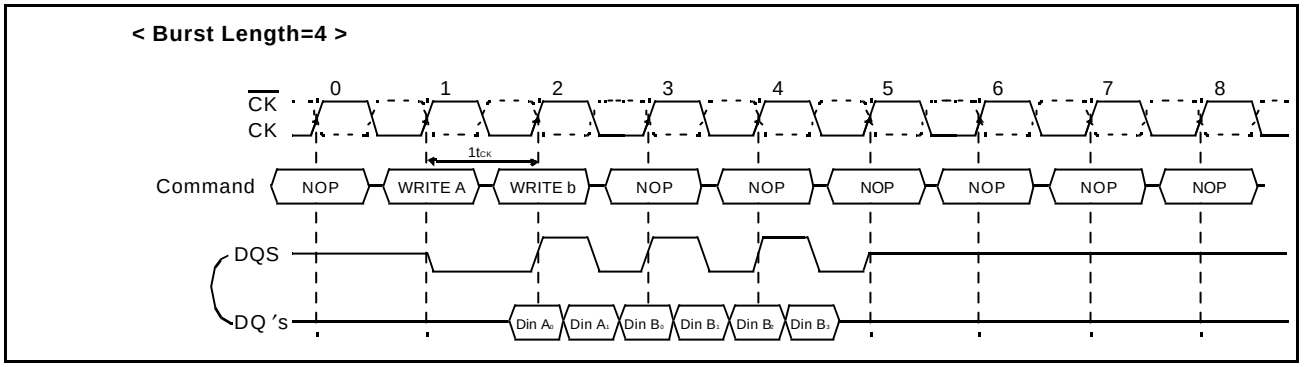


Figure 14. Write interrupted by a write timing

3.3.7 Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

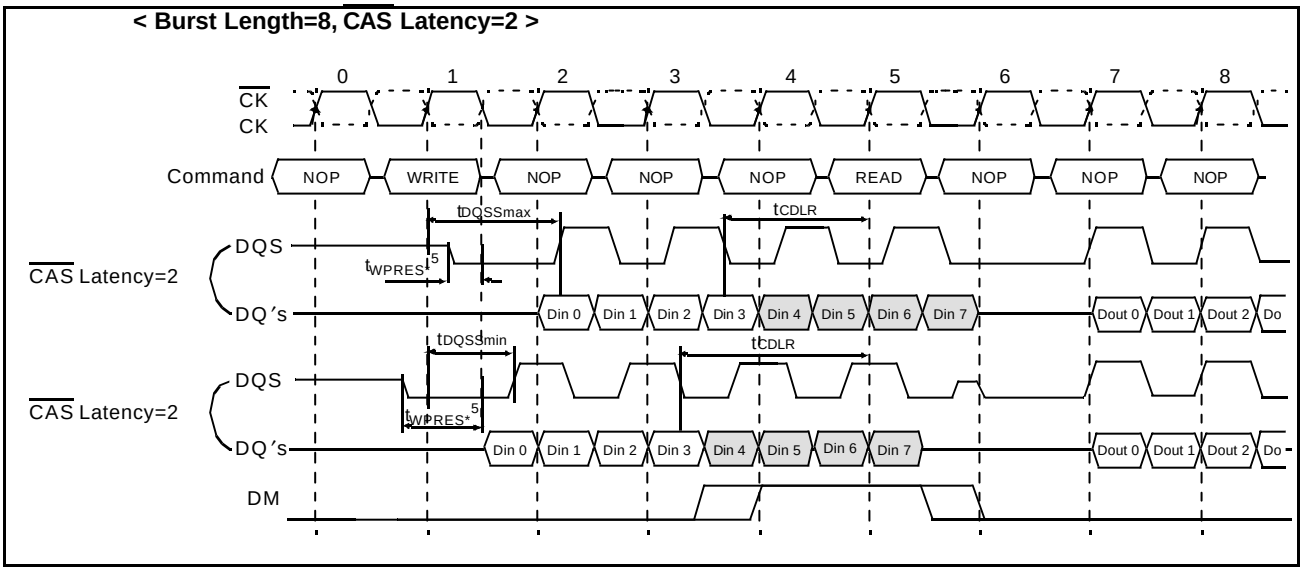


Figure 15. Write interrupted by a read and DM timing

The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words whcich immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the DDR SDRAM.
5. Refer to "3.3.2 Burst write operation"

3.3.8 Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time(tWR) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

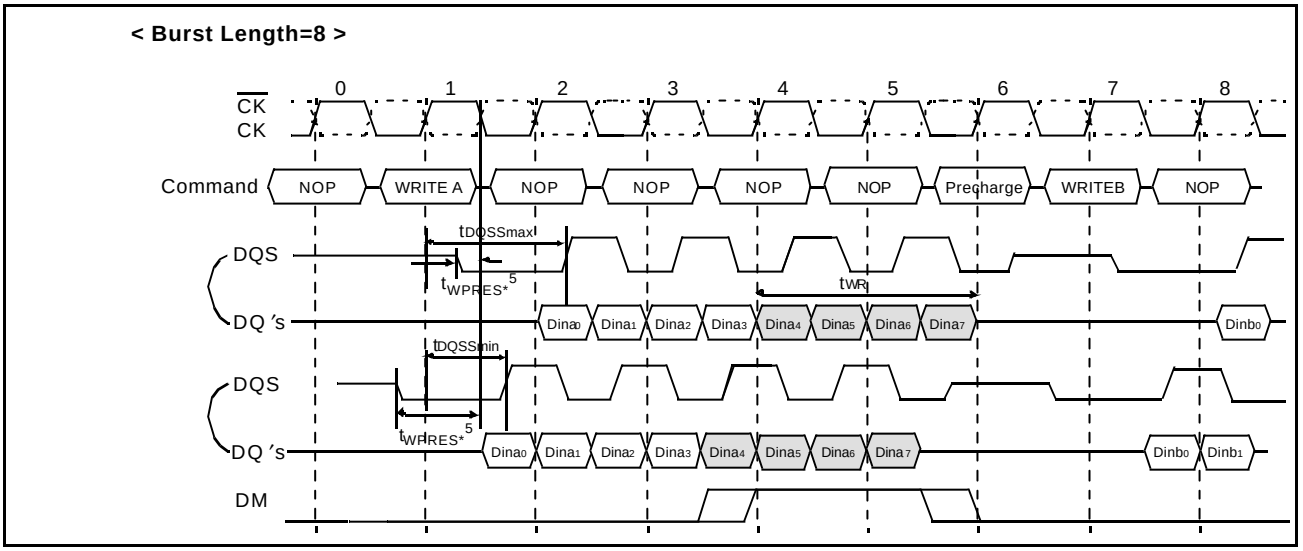


Figure 16. Write interrupted by a precharge and DM timing

Precharge timing for Write operations in DRAMs requires enough time to allow "write recovery" which is the time required by a DRAM core to properly store a full "0" or "1" level before a Precharge operation. For DDR SDRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the SDRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation, i.e., the input clock domain.

tWR starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by tWR.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by tWR.

3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after tWR+tRP where tWR+tRP starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where tRAS(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.
5. Refer to "3.3.2 Burst write operation"

3.3.9 Burst Stop

The burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock(CK). The burst stop command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ latency set in the mode register. The burst stop command, however, is not supported during a write burst operation.

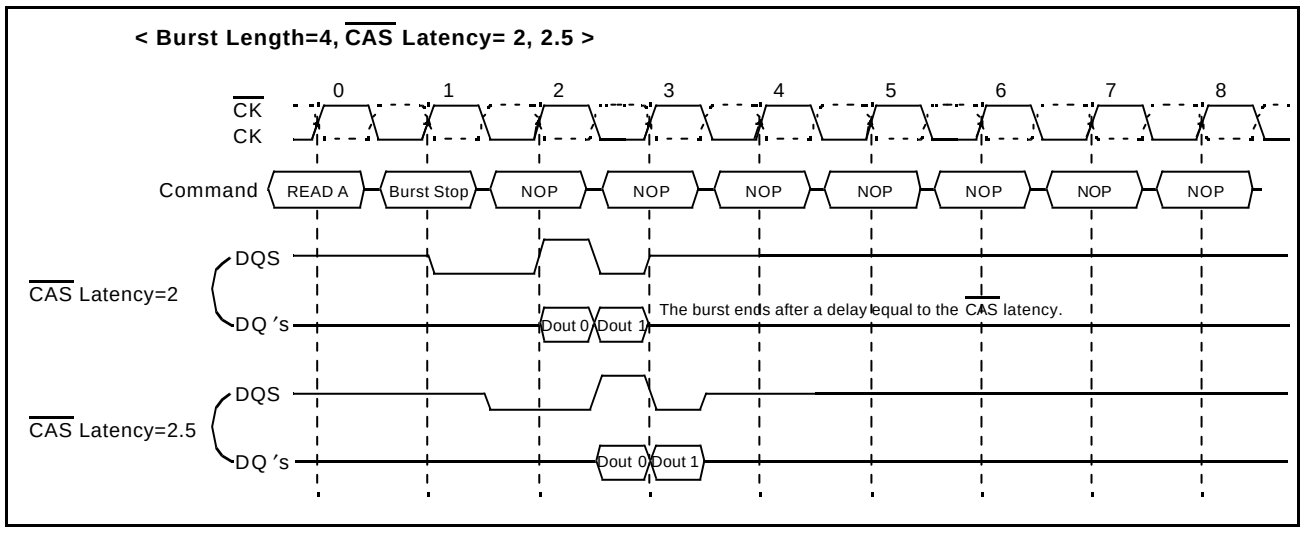


Figure 17. Burst stop timing

The Burst Stop command is a mandatory feature for DDR SDRAMs. The following functionality is required:

1. The BST command may only be issued on the rising edge of the input clock, CK.
2. BST is only a valid command during Read bursts.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.

6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations. This is shown in previous page Figure with examples for $\overline{CAS}$ latency (CL) of 1.5, 2, 2.5, 3 and 3.5 (only selected $\overline{CAS}$ latencies are required by the DDR SDRAM standards, the others are optional).
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).

3.3.10 DM masking

The DDR SDRAM has a data mask function that can be used in conjunction with data write cycle, not read cycle. When the data mask is activated (DM high) during write operation, DDR SDRAM does not accept the corresponding data.(DM to data-mask latency is zero).
DM must be issued at the rising or falling edge of data strobe.

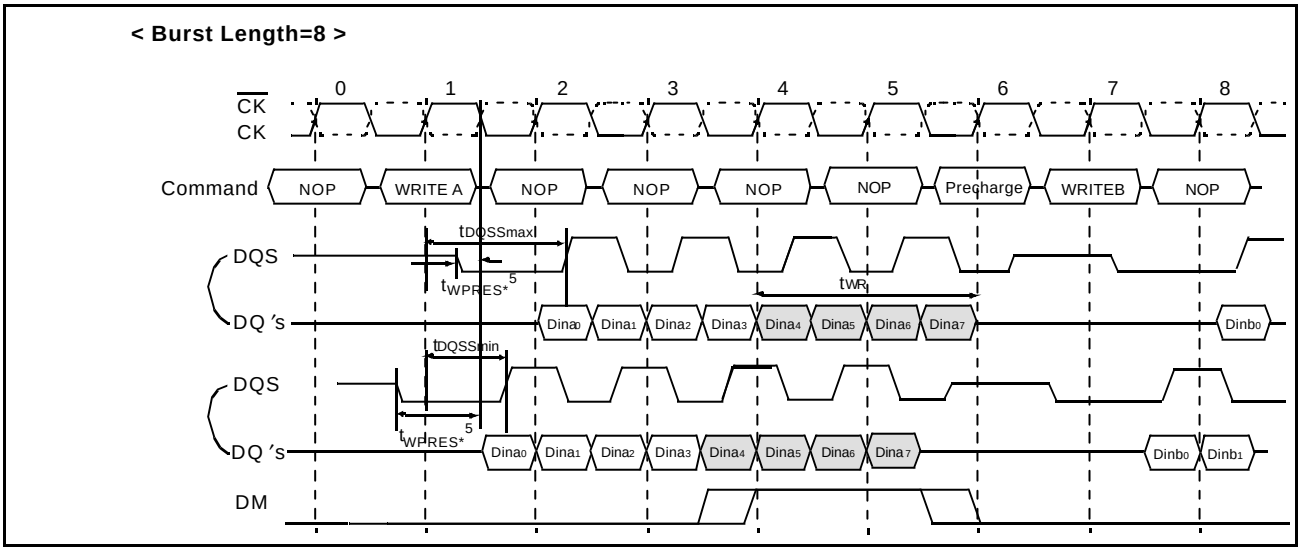


Figure 18. DM masking timing

3.3.11 Read With Auto Precharge

If a read with auto-precharge command is initiated, the DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when tRAS(min) is satisfied. If not, the start point of precharge operation will be delayed until tRAS(min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time(tRP) has been satisfied.

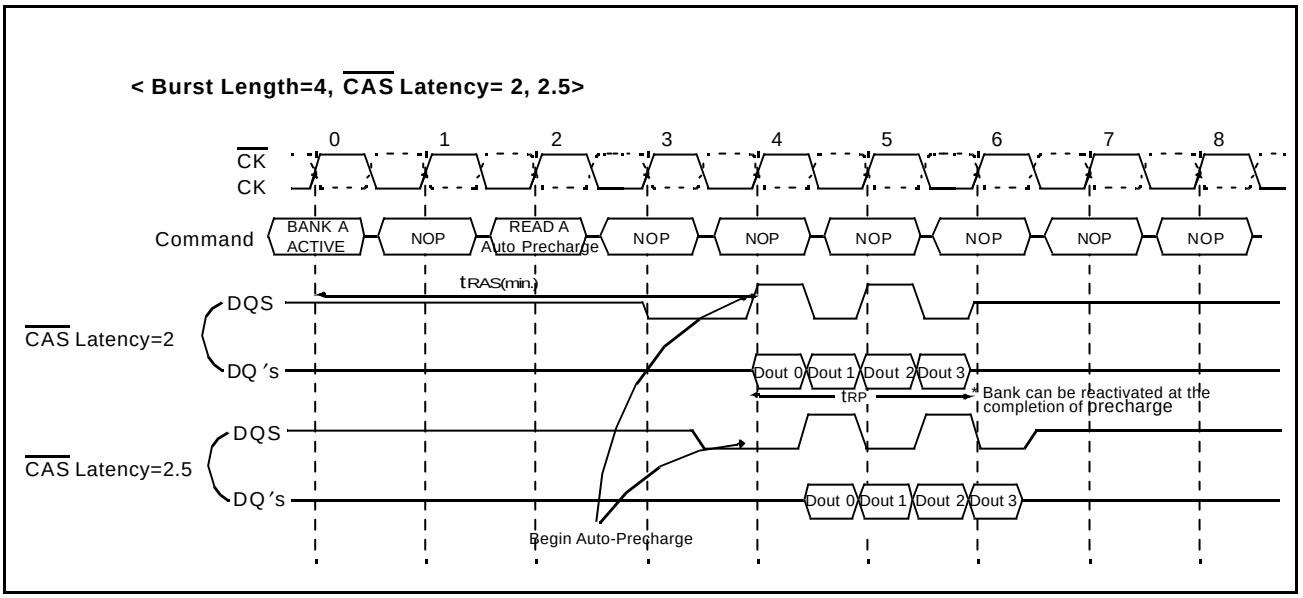


Figure 19. Read with auto precharge timing

When the Read with Auto precharge command is issued, new command can be asserted at 3,4 and 5 respectively as follows,

Asserted command	For same Bank			For Different Bank		
	3	4	5	3	4	5
READ	READ + No AP*1	READ+ No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

*1 : AP = Auto Precharge

Table 6. Operating description when new command asserted while read with auto precharge is issued

3.3.12 Write with Auto Precharge

If A10 is high when write command is issued , the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

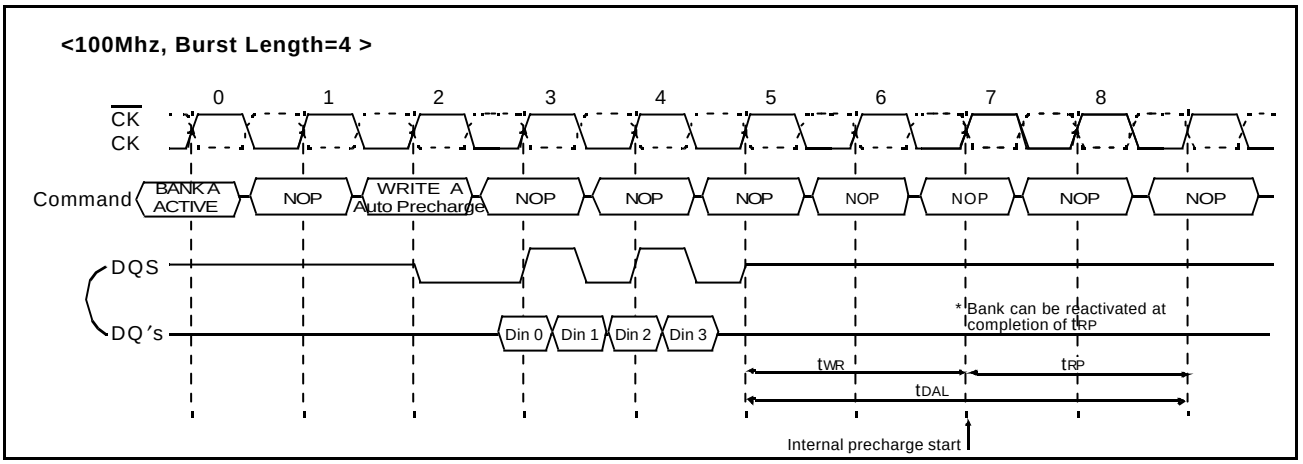


Figure 20. Write with auto precharge timing

Burst length = 4

Asserted command	For same Bank						For Different Bank				
	3	4	5	6	7	8	3	4	5	6	7
WRITE	WRITE+ No AP*1	WRITE+ No AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE+ AP	WRITE+ AP	WRITE+ AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ+NO AP+DM*2	READ+NO AP+DM	READ+ NO AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ+AP	Illegal	READ + AP+DM	READ + AP+DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

*1 : AP = Auto Precharge

*2 : DM : Refer to " *3.3.7 Write Interrupted by a Read & DM* " in page 25.

Table 7. Operating description when new command asserted while write with auto precharge is issued

3.3.13 Auto Refresh & Self Refresh

Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CK). All banks must be precharged and idle for tRP(min) before the auto refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the tRFC(min).

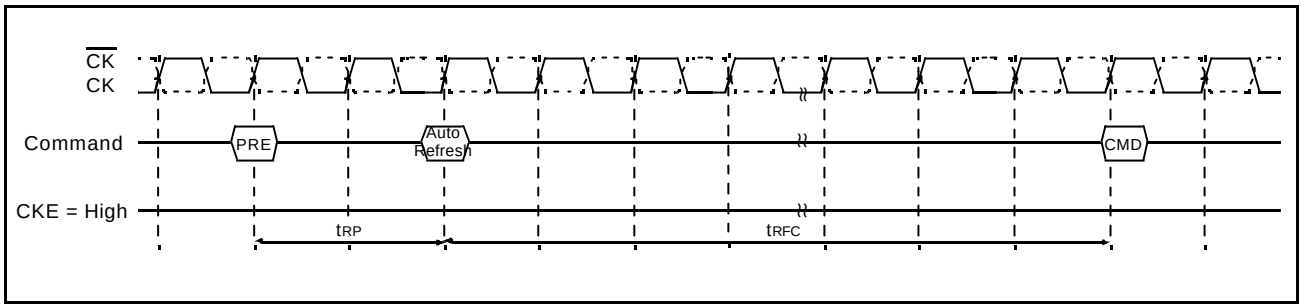


Figure 21. Auto refresh timing

Self Refresh

A self refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock(CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than tXSR for locking of DLL.

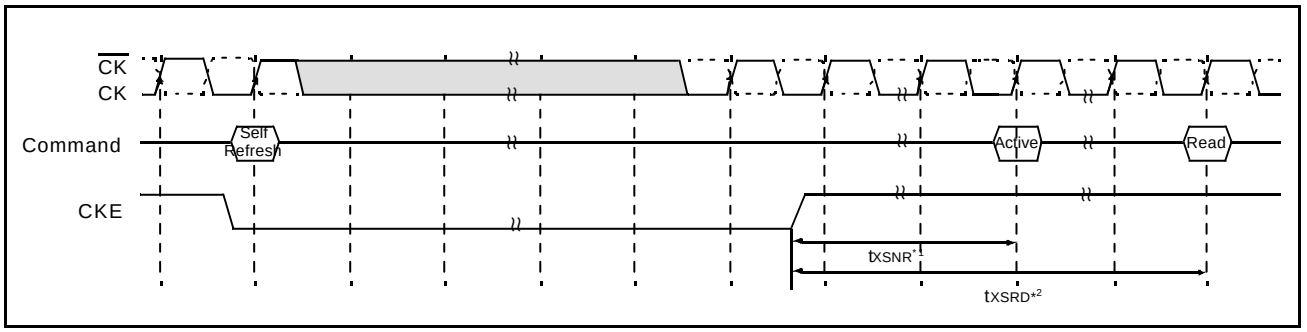


Figure 22. Self refresh timing

1. Exit self refresh to bank active command, a write command can be applied as far as tRCD is satisfied after any bank active command.
2. Exit self refresh to read command

3.3.14 Power down

The power down mode is entered when CKE is low and exited when CKE is high. Once the power down mode is initiated, all of the receiver circuits except clock, CKE and DLL circuit tree are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1tck+tIS prior to row active command . During power down mode, refresh operations cannot be performed, therefore the device cannot be remained in power down mode longer than the refresh period(Data retension time) of the device.

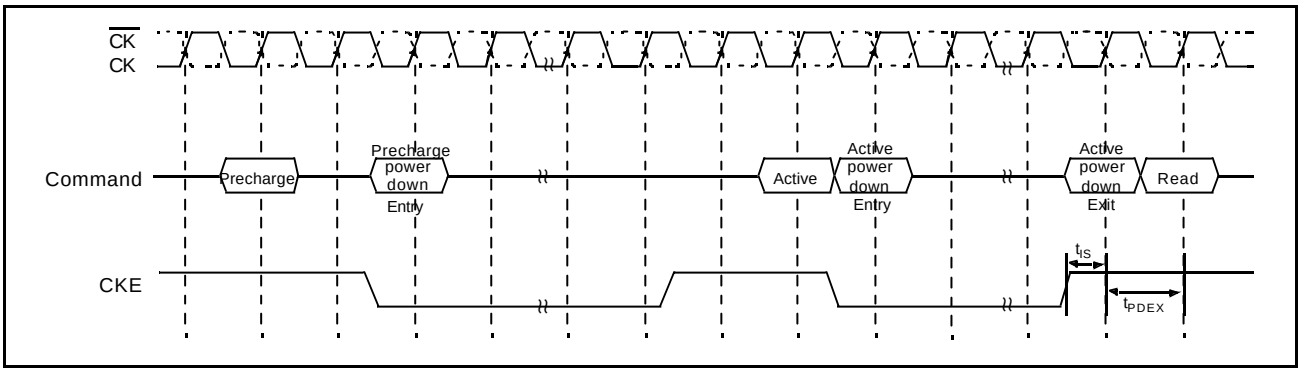


Figure 23. Power down entry and exit timing

4. Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Table 8. Command truth table

1. OP Code : Operand Code. A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

5. Functional Truth Table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARGE STANDBY	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A_{10}	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A_{10}	PRE/PREA	ILLEGAL*4
	L	L	L	H	X	Refresh	AUTO-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ACTIVE STANDBY	L	H	H	L	X	Burst Stop	NOP
	L	H	L	H	BA, CA, A_{10}	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A_{10}	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	L	H	H	L	X	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A_{10}	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A_{10}	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A_{10}	PRE/PREA	Terminate Burst, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Table 9-1. Functional truth table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst With DM=High, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE*6 (READA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	*6
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	*6
	L	L	H	L	BA, A10	PRE/PREA	*6
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO RECHARGE*7 (WRITEA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	*7
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	*7
	L	L	H	H	BA, RA	Active	*7
	L	L	H	L	BA, A10	PRE/PREA	*7
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Table 9-2. Functional truth table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARG-ING (DURING tRP)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING (FROM ROW ACTIVE TO tRCD)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING (DURING tWR OR tCDLR)	L	H	H	L	X	Burst Stop	ILLEGAL*2
	L	H	L	H	BA, CA, A10	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Table 9-3. Functional truth table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
RE-FRESHING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Table 9-4. Functional truth table

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING*8	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOPeration(Maintain Self-Refresh)
POWER DOWN	L	H	X	X	X	X	X	Exit Power Down(Idle after t_{PDEX})
	L	L	X	X	X	X	X	NOPeration(Maintain Power Down)
ALL BANKS IDLE*9	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State=Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table

Table 9-5. Functional truth table

ABBREVIATIONS :

H=High Level, L=Low level, X=Don't Care

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around and write recovery requirements.
4. NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Refer to "3.3.11 Read with Auto Precharge" in page 29 for detailed information.
7. Refer to "3.3.12 Write with Auto Precharge" in page 30 for detailed information.
8. CKE Low to High transition will re-enable CK, $\overline{CK}$ and other inputs asynchronously. A minimum setup time must be satisfied before issuing any command other than EXIT.
9. Power-Down and Self-Refresh can be entered only from All Bank Idle state.

ILLEGAL = Device operation and/or data integrity are not guaranteed.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions & Specifications

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and $\overline{CK}$ inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Notes 1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.

5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

6. These charactericteristics obey the SSTL-2 class II standards.

DDR SDRAM SPEC Items and Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	**IDD0**
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	**IDD1**
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); Vin = Vref for DQ,DQS and DM	**IDD2P**
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	**IDD2F**
Precharge Quiet standby current; CS# > = VIH(min); All banks idle; CKE > = VIH(min); Address and other control inputs stable with keeping >= VIH(min) or =<VIL(max); Vin = Vref for DQ ,DQS and DM	**IDD2Q**
Active power - down standby current ; one bank active; power-down mode; CKE=< VIL (max); Vin = Vref for DQ,DQS and DM	**IDD3P**
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	**IDD3N**
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; 50% of data changing at every burst; Iout = 0 m A	**IDD4R**
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	**IDD4W**
Auto refresh current; tRC = tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz and 12*tCK for DDR333; distributed refresh	**IDD5**
Self refresh current; CKE =< 0.2V; External clock should be on; tCK = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B and 166Mhz for DDR333	**IDD6**
Orerating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	**IDD7A**

IDD spec table

(V_{DD}=2.7V, T = 10°C)

Symbol		K4H560438C-TCB3 (DDR333)	K4H560438C-TCA2 (DDR266A)	K4H560438C-TCB0 (DDR266B)	K4H560438C-TCA0 (DDR200)	Unit	Notes
IDD0		145	122	122	108	mA	
IDD1		165	142	142	133	mA	
IDD2P		6	6	6	6	mA	
IDD2F		60	54	54	46	mA	
IDD2Q		40	36	36	32	mA	
IDD3P		43	35	35	33	mA	
IDD3N		90	77	77	68	mA	
IDD4R		230	190	190	155	mA	
IDD4W		240	200	200	165	mA	
IDD5		225	207	207	183	mA	
IDD6	Normal	6	6	6	6	mA	
IDD7A		390	320	320	285	mA	

< Detailed test conditions for DDR SDRAM IDD1 & IDD7 >

IDD1 : Operating current: One bank operation

1. Typical Case : Vdd = 2.5V, T=25' C
2. Worst Case : Vdd = 2.7V, T= 10' C
3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA
4. Timing patterns
   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst
   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst
   - DDR333(166Mhz, CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRCD=10*tCK, tRAS=7*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst

IDD7A : Operating current: Four bank operation

1. Typical Case : Vdd = 2.5V, T=25' C
2. Worst Case : Vdd = 2.7V, T= 10' C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns
   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
     Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst
   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK,Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst
   -DDR333(166Mhz,CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK,Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Operating Conditions

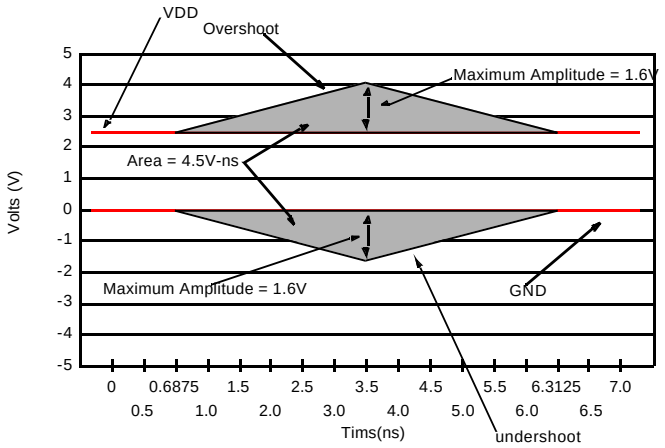
Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note

1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

Overshoot/Undershoot specification for Address and Control Pins

Parameter	Specification	Notes
Maximum peak amplitude allowed for overshoot (See Figure 1):	1.6 V	1,2,3
Maximum peak amplitude allowed for undershoot (See Figure 1):	1.6 V	1,2,3
The area between the overshoot signal and VDD must be less than or equal to (See Figure 1):	4.5 V-ns	1,2,3
The area between the undershoot signal and GND must be less than or equal to (See Figure 1):	4.5 V-ns	1,2,3

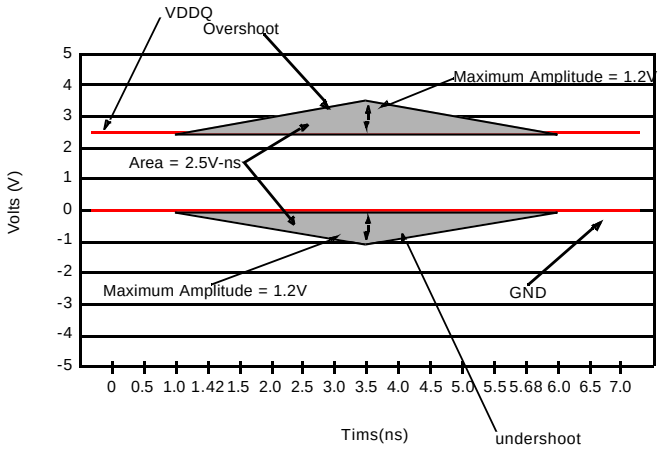


Notes:

1. This specification is intended for only DDR200, DDR266A and DDR266B devices.
2. This specification is intended for only devices with NO clamp protection
3. This compliance is to be verified by design only.

Overshoot/Undershoot specification for Data Pins

Parameter	Specification	Notes
Maximum peak amplitude allowed for overshoot (See Figure 2):	1.2 V	1,2,3
Maximum peak amplitude allowed for undershoot (See Figure 2):	1.2 V	1,2,3
The area between the overshoot signal and VDD must be less than or equal to (See Figure 2):	2.5 V-ns	1,2,3
The area between the undershoot signal and GND must be less than or equal to (See Figure 2):	2.5 V-ns	1,2,3



Notes:

1. This specification is intended for only DDR200, DDR266A and DDR266B devices.
2. This specification is intended for only devices with NO clamp protection
3. This compliance is to be verified by design only.

Stacked 512Mb(x4) DDR SDRAM

AC Timming Parameters & Specifications

Parameter		Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	65		65		70		ns	
Refresh row cycle time		tRFC	75		75		80		ns	
Row active time		tRAS	45	120K	45	120K	48	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	20		20		20		ns	
Row precharge time		tRP	20		20		20		ns	
Row active to Row active delay		tRRD	15		15		15		ns	
Write recovery time		tWR	15		15		15		ns	
Last data in to Read command		tCDLR	1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	10	12	10	12	ns	5
	CL=2.5		7.5	12	7.5	12			ns	5
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.5	-	0.5	-	0.6	ns	5
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		ns	2
DQS-in hold time		tWPRE	0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time(fast)		tIS	0.9		0.9		1.1		ns	6
Address and Control Input hold time(fast)		tIH	0.9		0.9		1.1		ns	6
Address and Control Input setup time(slow)		tIS	1.0		1.0		1.1		ns	6
Address and Control Input hold time(slow)		tIH	1.0		1.0		1.1		ns	6
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Input Slew Rate(for input only pins)		tSL(I)	0.5		0.5		0.5		V/ns	6
Input Slew Rate(for I/O pins)		tSL(IO)	0.5		0.5		0.5		V/ns	7
Output Slew Rate(x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate(x16)		$tSL_{(O)}$	0.7	5	0.7	5	0.7	5	V/ns	10
Output Slew Rate Matching Ratio(rise to fall)		t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter	Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		0.5		0.6		ns	7,8,9
DQ & DM input pulse width	tDIPW	1.75		1.75		2		ns	
Power down exit time	tPDEX	7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		80		ns	4
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	tREF	7.8		7.8		7.8		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

1. Maximum burst refresh of 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.

Table 17. AC timing parameters and specifications(DDR266/200)

6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	ΔtDS	ΔtDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Note>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	ΔtIH/tIS (ps)	ΔtDSS/tDSH (ps)	ΔtAC/tDQSCK (ps)	ΔtLZ(min) (ps)	ΔtHZ(max) (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

8.4 AC Timming Parameters & Specifications(DDR333)

Parameter		Symbol	-TCB3(DDR333)		Unit	Note
			Min	Max		
Row cycle time		tRC	60		ns	
Refresh row cycle time		tRFC	72		ns	
Row active time		tRAS	42	70K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	18		ns	
Row precharge time		tRP	18		ns	
Row active to Row active delay		tRRD	12		ns	
Write recovery time		tWR	15		ns	
Last data in to Read command		tCDLR	1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	ns	4
	CL=2.5		6	12	ns	4
Clock high level width		tCH	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.6	+0.6	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.7	+0.7	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.45	ns	4
Read Preamble		tRPRE	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		ns	2
Write Preamble		tWPRE	0.25		tCK	
Write Postamble		tWPST	0.4	0.6	tCK	3
DQS falling edge to CK rising-setup time		tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		tCK	
DQS-in high level width		tDQSH	0.35		tCK	
DQS-in low level width		tDQSL	0.35		tCK	
Address and Control Input setup/hold time (fast slew rate)		tIS/tIH	0.75		ns	
Address and Control Input setup/hold time (slow slew rate)		tIS/tIH	0.8		ns	
DQ and DM input setup time		tDS	0.45		ns	
DQ and DM input hold time		tDH	0.45		ns	
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.7	+0.7	ps	
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.7	+0.7	ps	

Parameter	Symbol	-TCB3(DDR333)		Unit	Note
		Min	Max		
Mode register set cycle time	tMRD	12		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		ns	
DQ & DM input pulse width(for each input)	tDIPW	1.75		ns	
Exit self refresh to non read command	tXSNR	75		ns	
Exit self refresh to read command	tXSRD	200		tCK	
Refresh interval time	tREFI	7.8		us	1
Output DQS valid window	tQH	tHP-tQHS	-	ns	4
Clock half period	tHP	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.55	ns	
DQS write postamble time	tRAP	tRCD or tRAS min		ns	3
Auto Precharge Write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		tCK	

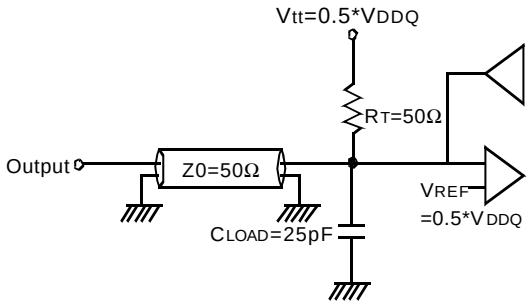
1. Maximum burst refresh of 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DINNs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.

Table 18. AC timing parameters and specifications(DDR333)

AC Operating Test Conditions

(V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V_{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate (for imput only)	0.5	V/ns	
Input slew rate (I/O pins)	0.5	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}-0.31	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Load Circuit		



Input/Output Capacitance

(V_{DD}=2.5, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN1}	4.0	6.0	pF
Input capacitance(CK, $\overline{CK}$)	C_{IN2}	4.0	6.0	pF
Data & DQS input/output capacitance	C_{OUT}	8.0	10.0	pF
Input capacitance(DM)	C_{IN3}	8.0	10.0	pF