256Mbit GDDR3 SDRAM

Revision 1.8

April 2005

Revision History

Revision 1.8 (April 9, 2005)
- Modified note description for the Write Latency on page 47.

Revision 1.7 (Jan. 18 , 2005)
- Added Lead Free package part number in the data sheet.

Revision 1.6 (Dec 2 , 2004)
- Changed ICC2P and ICC6 for all frequency. Separted ICC6 for -GC and -GL.

Revision 1.5 (Oct 5 , 2004)
- Added K4J55323QF-G(V)C15
- Timing diagram corrected on page 28

Revision 1.4 (July 9 , 2004)
- Added K4J55323QF-G(V)L20 which is VDD&VDDQ=1.8V(typical)

Revision 1.3 (June 14 , 2004)
- Changed DC spec value for all the frequency. Refer to the DC characteristics of page 45.
- Removed -GC12 from the spec.

Revision 1.2 (February 18 , 2004)
- Changed VDD/VDDQ from 1.9V± 0.1V to 2.0V± 0.1V in all frequencies.
- DC changes : Refer to the DC characteristics of page 45.

Revision 1.1 (January 29 , 2004)
- Typo corrected

Revision 1.0 (January 15 , 2004)
- Changed VDD/VDDQ of K4J55323QF-GC12 from 2.1V± 0.1V to 1.9V± 0.1V
- Changed VDD/VDDQ of K4J55323QF-GC14/16/20 from 1.8V± 0.1V to 1.9V± 0.1V
- Changed tCK(max) from 3.0ns to 3.3ns
- DC spec finalized. Typo corrected

Revision History

Revision 0.5 (January 7 , 2004) ***- Preliminary spec***

- Added "Dummy MRS" command during the power-up sequence. Typo corrected

Revision 0.4 (December 10 , 2003) ***- Preliminary spec***

- Typo corrected
- Added K4J55323QF-GC12 (800MHz) in the spec
- Key AC parameter changes : Refer to the AC spec table on page 46,47
  . Added tDAL in the AC characteristics table,
  . Added AC parameter of -GC12 in the AC characteristics table,
  . Changed tRC of -GC14 from 31tCK to 30tCK,
  . Changed tRFC of -GC16 from 34tCK to 33tCK,
- DC changes : Refer to the DC characteristics table of page 45.
- Capacitance table change : Refer to the Capacitance table of page 45.

Revision 0.3 (November 13, 2003) ***- Target Spec***

- Typo corrected
- Removed 800MHz from the spec
- Changed ICC6 from 4mA to 7mA
- Key AC parameter changes : Refer to the AC spec table on page 46,47
  . Changed tWR of -GC14 from 6tCK to 9tCK,
  . Changed tWR of -GC16 from 5tCK to 8tCK,
  . Changed tWR of -GC20 from 4tCK to 6tCK
  . Changed tPDEX and tXSR at low power from 100tCK to 300tCK

Revision 0.2 (October 17, 2003) ***- Target Spec***

- Typo corrected

Revision 0.1 (September 26, 2003) ***- Target Spec***

- Typo corrected

Revision 0.0 (September 25, 2003) ***- Target Spec***

2M x 32Bit x 4 Banks Graphic Double Data Rate 3 Synchronous DRAM with Uni-directional Data Strobe

FEATURES

- 2.0V ± 0.1V power supply for device operation
- 2.0V ± 0.1V power supply for I/O interface
- On-Die Termination (ODT)
- Output Driver Strength adjustment by EMRS
- Calibrated output drive
- Pseudo Open drain compatible inputs/outputs
- 4 internal banks for concurrent operation
- Differential clock inputs (CK and $\overline{CK}$)
- Commands entered on each positive CK edge
- CAS latency : 5, 6, 7, 8 and 9 (clock)
- Additive latency (AL): 0 and 1 (clock)
- Programmable Burst length : 4
- Programmable Write latency : 1, 2, 3, 4, 5 and 6 (clock)
- Single ended READ strobe (RDQS) per byte
- Single ended WRITE strobe (WDQS) per byte
- RDQS edge-aligned with data for READs
- WDQS center-aligned with data for WRITEs
- Data Mask(DM) for masking WRITE data
- Auto & Self refresh mode
- Auto Precharge option
- 32ms, auto refresh (4K cycle)
- 144 Ball FBGA
- Maximum clock frequency up to700MHz
- Maximum data rate up to 1.4Gbps/pin
- DLL for outputs

ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4J55323QF-GC14	700MHz	1400Mbps/pin	Pseudo Open Drain	144 - Ball FBGA
K4J55323QF-GC15	667MHz	1334Mbps/pin		
K4J55323QF-GC16	600MHz	1200Mbps/pin		
K4J55323QF-GC20*	500MHz	1000Mbps/pin		

***K4J55323QF-GL20/VL20 : VDD & VDDQ = 1.8V±0.1V(1.7V ~ 1.9V)**
***K4J55323QF-V is the Lead Free package part number**

GENERAL DESCRIPTION

FOR 2M x 32Bit x 4 Bank GDDR3 SDRAM

The 8Mx32 GDDR3 is 268,435,456 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 2,097,152 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 5.6GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION

Normal Package (Top View)

	2	3	4	5	6	7	8	9	10	11	12	13
B	WDQS0	RDQS0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	RDQS3	WDQS3
C	DQ4	DM0	VDDQ	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	VDDQ	DM3	DQ27
D	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
E	DQ7	RFU3	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	RFU4	DQ24
F	DQ17	DQ16	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DQ15	DQ14
G	DQ19	DQ18	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DQ13	DQ12
H	WDQS2	RDQS2	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	RDQS1	WDQS1
J	DQ20	DM2	VDDQ	VSSQ	NC, VSS	NC, VSS	NC, VSS	NC, VSS	VSSQ	VDDQ	DM1	DQ11
K	DQ21	DQ22	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ10
L	DQ23	A3	VDD	VSS	RFU_2	VDD	VDD	RFU_1	VSS	VDD	A4	DQ8
M	VREF	A2	A10	/RAS	RESET	CKE	RFU5	ZQ	/CS	A9	A5	VREF
N	A0	A1	A11	BA0	/CAS	CK	/CK	/WE	BA1	A8/AP	A6	A7

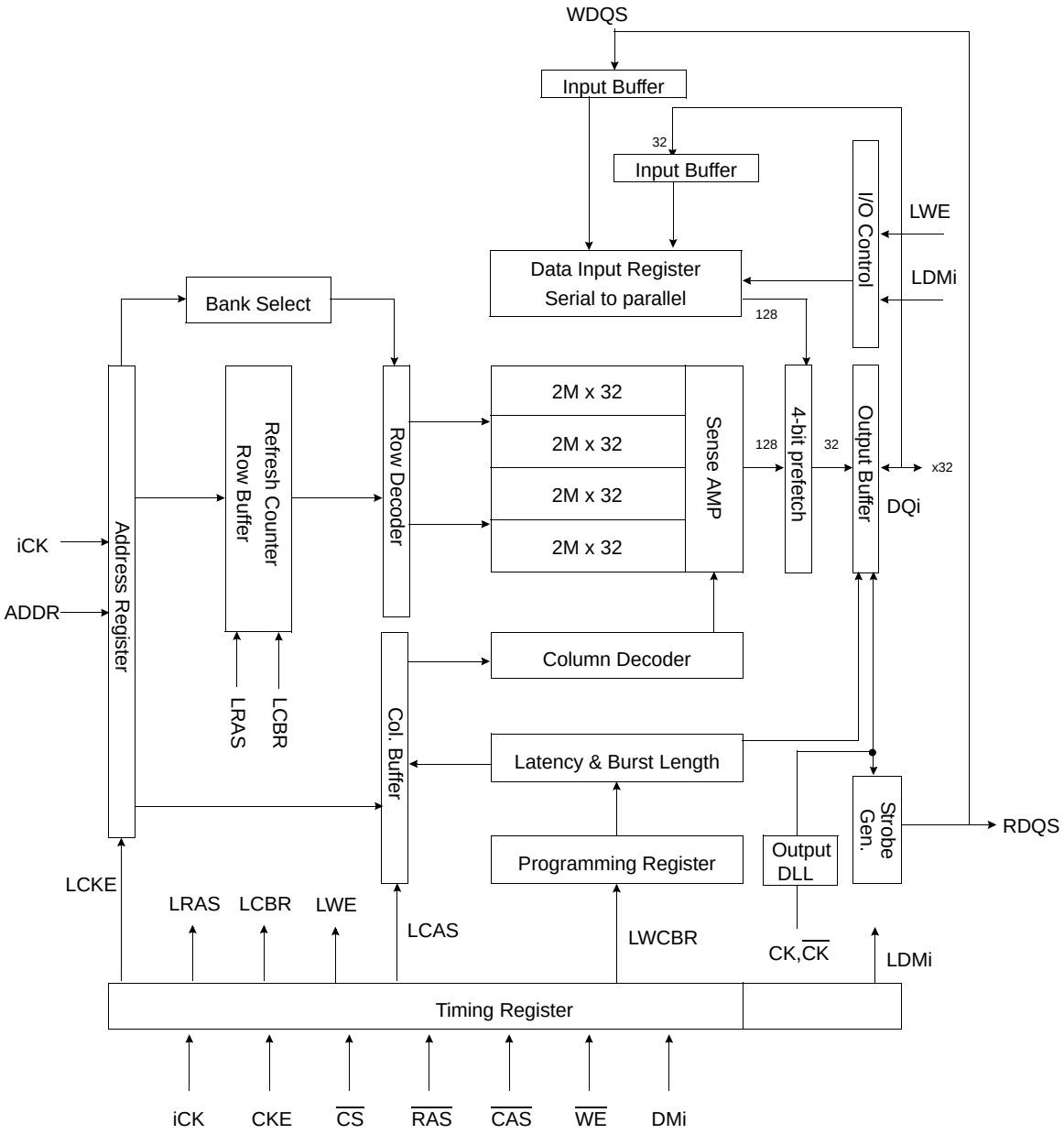
NOTE :

1. RFU1 is reserved for A12
2. RFU2 is reserved for BA2
3. (M,13) VREF for CMD and ADDRESS
4. (M,2) VREF for Data input

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. CMD, ADD inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM0 ~DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of clock. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 ~ A11	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A8 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA7, CA9 . Column address CA8 is used for auto precharge.
DQ0 ~ DQ31	Input/ Output	**Data Input/ Output:** Bi-directional data bus.
RDQS0 ~ RDQS3	Output	**READ Data Strobe:** Output with read data. RDQS is edge-aligned with read data.
WDQS0 ~ WDQS3	Input	**WRITE Data Strobe:** Input with write data. WDQS is center-aligned to the input data.
NC/RFU		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 2.0V ± 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.0V ± 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage:** 0.7*VDDQ , **2 Pins :** (M,2) for Data input , (M,13) for CMD and ADDRESS
ZQ	Reference	Resistor connection pin for On-die termination. The value of Resistor = 240 Ω
RES	Input	**Reset pin:** RESET pin is a VDDQ CMOS input

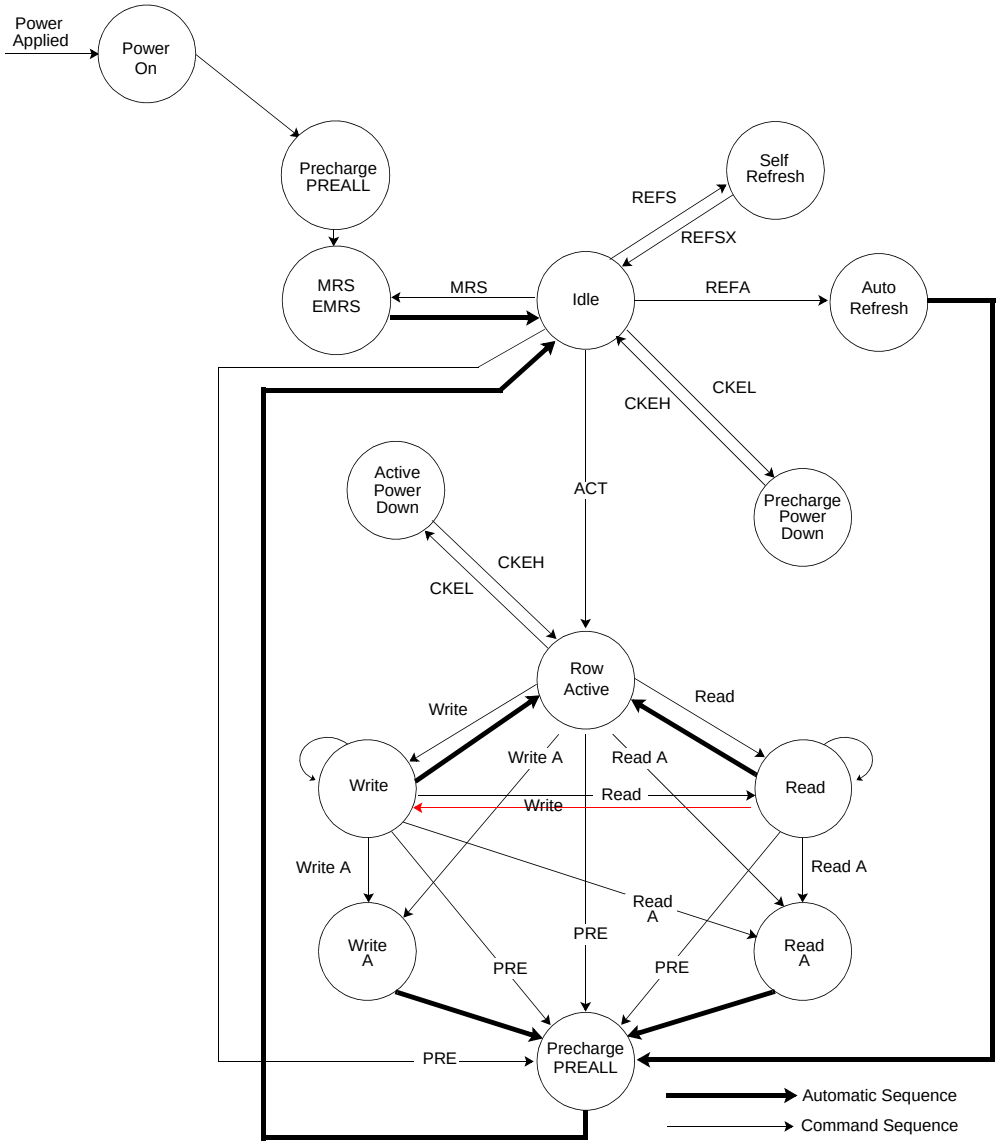
BLOCK DIAGRAM (2Mbit x 32I/O x 4 Bank)



* iCK : internal clock

FUNCTIONAL DESCRIPTION

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

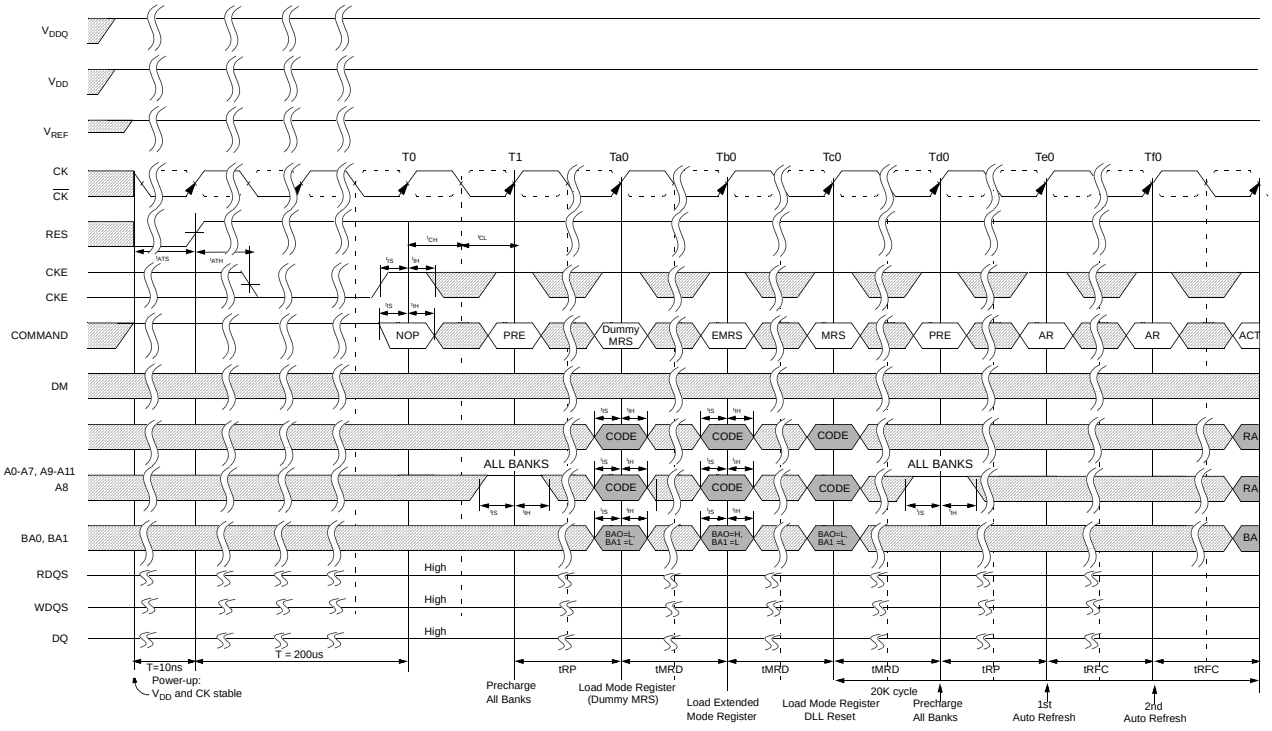
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

INITIALIZATION

GDDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

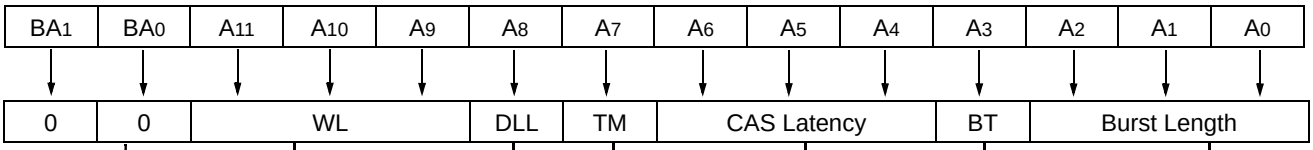
1. Apply power and keep CKE/RESET at low state (All other inputs may be undefined)
   - Apply VDD and VDDQ simultaneously
   - Apply VDDQ before Vref. (Inputs are not recognized as valid until after V_{REF} is applied)
2. Required minimum 100us for the stable power before RESET pin transition to HIGH
   - Upon power-up the address/command active termination value will automatically be set based off the state of RESET and CKE.
   - On the rising edge of RESET the CKE pin is latched to determine the address and command bus termination value.
     If CKE is sampled at a zero the address termination is set to 1/2 of ZQ.
     If CKE is sampled at a one the address termination is set to ZQ.
   - RESET must be maintained at a logic LOW level and CS at a logic high value during power-up to ensure that the DQ outputs will be in a High-Z state, all active terminators off, and all DLLs off.
4. Minimum 200us delay required prior to applying any executable command after stable power and clock.
5. Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, then RESET and CKE should be brought to HIGH,
6. Issue a PRECHARGE ALL command following after NOP command.
7. Issue a dummy MRS command ("000010001000001")
8. Issue a EMRS command (BA1BA0="01") to enable the DLL.
9. Issue MRS command (BA0BA1 = "00") to reset the DLL and to program the operating parameters.
   20K clock cycles are required to lock the DLL.
9. Issue a PRECHARGE ALL command
10. Issue at least two AUTO refresh command to update the driver impedance and calibrate the output drivers.

Following these requirements, the GDDR3 SDRAM is ready for normal operation.



MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of GDDR3 SDRAM. It programs CAS latency, addressing mode, test mode and various vendor specific options to make GDDR3 SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The GDDR3 SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{11} and BA_0, BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum six clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The Burst length uses A_0 ~ A_2. CAS latency (read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_8 is used for DLL reset. A_9 ~ A_{11} are used for Write latency. Refer to the table for specific codes for various addressing modes and CAS latencies.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

Test Mode

A_7	mode
0	Normal
1	Test

Burst Type

A_3	Burst Type
0	Sequential
1	Reserved

DLL

A_8	DLL Reset
0	No
1	Yes

Write Latency

A_{11}	A_{10}	A_9	Write Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

CAS Latency

A_6	A_5	A_4	CAS Latency
0	0	0	8
0	0	1	9
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	5
1	1	0	6
1	1	1	7

Burst Length

A_2	A_1	A_0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER AND ACTIVE TERMINATOR

The GDDR3 SDRAM is equipped with programmable impedance output buffers and Active Terminators. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor(RQ) is connected between the ZQ pin and Vss. The value of the resistor must be six times the desired output impedance.
For example, a 240Ω resistor is required for an output impedance of 40Ω. To ensure that output impedance is one sixth the value of RQ (within 10 %), the range of RQ is 120Ω to 360Ω (20Ω to 60Ω output impedance).
RES, CK and /CK are not internally terminated. CK and /CK will be terminated on the system module using external 1% resisters. The output impedance is updated during all AUTO REFRESH commands and NOP commands when a READ is not in progress to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update. To guarantee optimum output driver impedance after power-up, the GDDR3(x32) needs 20us after the clock is applied and stable to calibrate the impedance upon power-up. The user can operate the part with fewer than 20us, but optimal output impedance is not guaranteed. The value of ZQ is also used to calibrated the internal address/command termination resisters. The two termination values that are selectable at power up are 1/2 of ZQ and ZQ. The value of ZQ is used to calibrate the internal DQ termination resisters. The two termination values that are selectable are 1/4 of ZQ and 1/2 of ZQ.

BURST LENGTH

Read and write accesses to the GDDR3 SDRAM are burst oriented, with the burst length being programmable, as shown in MRS table. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst length of 4 only is available. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2-A*i* when the burst length is set to four (Where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmable burst length applies to both READ and WRITE bursts.

BURST TYPE

Accesses within a given burst must be programmed to be sequential; this is referred to as the burst type and is selected via bit A3. This device does not support the interleaved burst mode found in DDR SDRAM devices. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in below table: Burst Definition

Burst Definition

Burst Length	Starting Column Address		Order of Access within A burst
			Type= Sequential
4	A1	A0	
	0	0	0 - 1 - 2 - 3

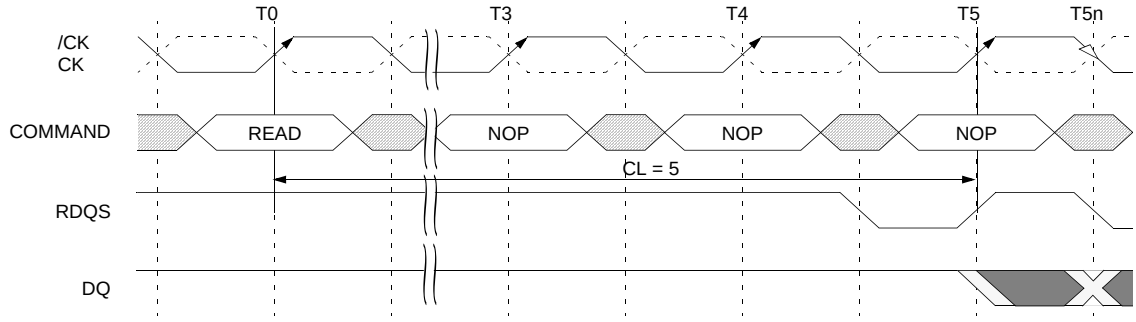
NOTE : 1. For a burst length of four, A2-A7 select the block of four burst; A0-A1 select the starting column within the block and must be set to zero

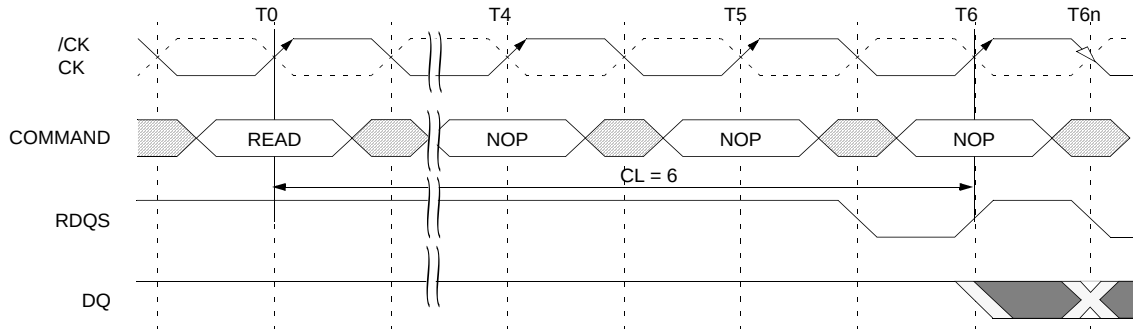
CAS LATENCY (READ LATENCY)

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 5~9 clocks. If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n+m*. Below table indicates the operating frequencies at which each CAS latency setting can be used. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latency

	Allowable operating Frequency (MHz)				
SPEED	**CL=9**	**CL=8**	**CL=7**	**CL=6**	**CL=5**
-12	≤ 800	-	-	-	-
-14	≤ 700	-	-	-	-
-16	-	≤ 600	-	-	-
-20	-	-	≤ 500	-	-





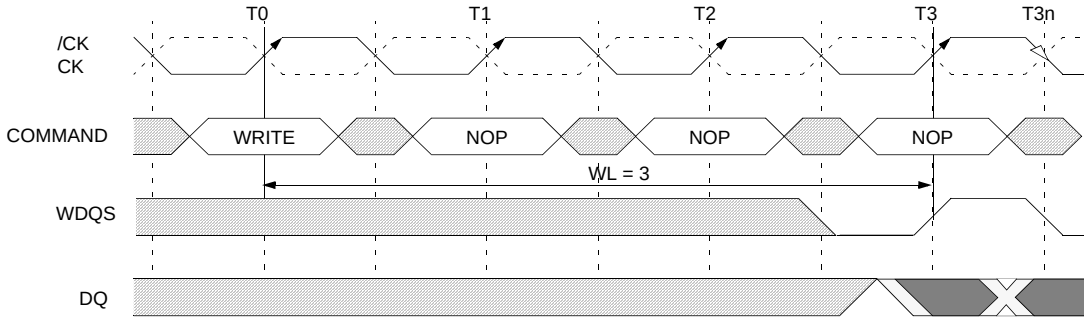
Burst Length = 4 in the cases shown
Shown with nominal t_{AC} and nominal t_{DSDQ}

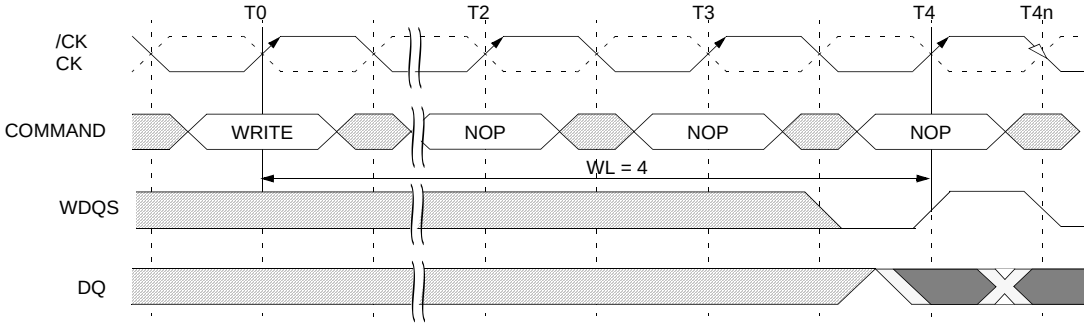
DON'T CARE **TRANSITIONING DATA**

WRITE LATENCY

The Write latency (WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data. The latency can be set from 1 to 6 clocks depending in the operating frequency and desired current draw. When the write latencies are set to 1 or 2 or 3 clocks, the input receivers never turn off when the WRITE command is registered. If a WRITE command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n*+*m*. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

* Maximum frequency of GDDR3 can be limited in WL4, 5 and 6





Burst Length = 4 in the cases shown

DON'T CARE **TRANSITIONING DATA**

TEST MODE

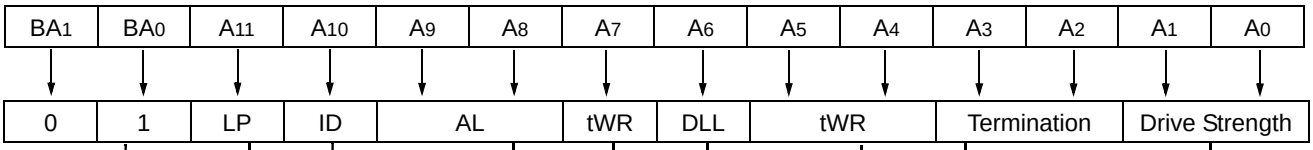
The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7 set to zero, and bits A0-A6 and A8-A11 set to the desired values. Test mode is entered by issuing a MODE REGISTER SET command with bit A7 set to one, and bits A0-A6 and A8-A11 set to the desired values. Test mode functions are specific to each Dram Manufacturer and its exact functions are hidden from the user.

DLL RESET

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A8 set to zero, and bits A0-A7 and A9-A11 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits A0-A7 and A9-A11 set to the desired values. When a DLL Reset is complete the GDDR3 SDRAM reset bit 8 of the mode register to a zero. After DLL Reset MRS, Power down can not be issued during 10 clock.

EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data output driver strength and on-die termination options. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The GDDR3 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11 and BA0 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. Six clock cycles are required to complete the write operation in the extended mode register. 4 kinds of the output driver strength are supported by EMRS (A1, A0) code. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. "High" on BA0 is used for EMRS. Refer to the table for specific codes.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

Vendor ID

A_{10}	Vendor ID
0	Off
1	On

DLL

A_6	DLL
0	Enable
1	Disable

Drive Strength

A_1	A_0	Drive Strength
0	0	Autocal
0	1	30Ω
1	0	40Ω
1	1	50Ω

Additive Latency

A_9	A_8	AL
0	0	0
0	1	1
1	0	Reserved
1	1	Reserved

tWR

A_7	A_5	A_4	tWR
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Termination

A_3	A_2	Termination
0	0	ODT Disabled
0	1	Reserved
1	0	ZQ/4
1	1	ZQ/2

Low Power

A_{11}	Low Power
0	Disable
1	Enable

* ZQ : Resistor connection pin for On-die termination

DLL ENABLE/DISABLE

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after disabling the DLL for debugging or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 20K clock cycles must occur before a READ command can be issued.

DATA TERMINATION

The Data Termination, DT, is used to determine the value of the internal data termination resisters. The GDDR3 SDRAM supports 60Ω and 120Ω termination. The termination may also be disabled for testing and other purposes.

DATA DRIVER IMPEDANCE

The Data Driver impedance (DZ) is used to determine the value of the data drivers impedance. When autocalibration is used the data driver impedance is set to 40Ωs and it's tolerance is determined by the calibration accuracy of the device. When any other value is selected the target impedance is set nominally to the desired impedance. However, the accuracy is now determined by the device's specific process corner, applied voltage and operating temperature.

ADDITIVE LATENCY

The Additive Latency function (AL) is used to optimize the command bus efficiency. The AL value is used to determine the number of clock cycles that is to be added to CL after CAS is captured by the rising edge of CK. Thus the total CAS latency is determined by adding CL and AL.

MANUFACTURERS VENDOR CODE AND REVISION IDENTIFICATION

The Manufacturers Vendor Code, V, is selected by issuing a EXTENDED MODE REGISTER SET command with bits A10 set to one, and bits A0-A9 and A11 set to the desired values. When the V function is enabled the GDDR3 SDRAM will provide its manufacturers vendor code on DQ[3:0] and revision identification on DQ[7:4]

Manufacturer	DQ[3:0]
Reserved	0
Samsung	1
Infineon	2
Elpida	3
Etron	4
Nanya	5

Manufacturer	DQ[3:0]
Hynix	6
Mosel	7
Winbond	8
ESMT	9
Reserved	A
Reserved	B

Manufacturer	DQ[3:0]
Reserved	C
Reserved	D
Reserved	E
Micron	F

LOW POWER MODE

Low power mode can be enabled by A11="H" during the EMRS command and in this case, Precharge Power Down command activates LP mode1 and Self Refresh command activates LP mode2. In case that A11 set to "L" during the EMRS, Low Power mode is disabled and Precharge Power Down command and Self Refresh command will do normal operation.

If a Precharge Power Down command issued under the condition of Low Power mode enabled, a device enters the LP mode1 and it can reduce Precharge Power Down current significantly by disabling DLL during the Precharge Power Down, however it requires more time to exit Power Down. If the power down duration is less than 20us, the required tPDEX is 300tCK. Otherwise, 20000tCK required for the tPDEX.

If a Self Refresh command issued under the condition of Low Power mode enabled, a device enters the LP mode2 and it can reduce tXSR while slightly increase the Self Refresh current. If the Self Refresh duration is less than 20us, the required tXSR is 300tCK. Otherwise, 20000tCK required for the tXSR.

Low Power / Command	Disabled (A11="L" @ EMRS)	Enabled (A11="H" @ EMRS)	Comments
Precharge Power Down	Precharge Power Down	LP Mode1	. DLL disabled for the purpose of current saving (ICC2P minimized) . tPDEX increased - 300tCK@ power down exit within 20us - 20KtCK@ power down exit after 20us
Self Refresh	Self Refresh	LP Mode2	. Short tXSR - 300tCK@ Self Refresh exit within 20us - 20KtCK@ Self Refresh exit after 20us

COMMANDS

Below Truth table-COMMANDs provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the operation section : these tables provide current state/next state information.

TRUTH TABLE - COMMANDs

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	8, 11
NO OPERATION (NOP)	L	H	H	H	X	8
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2
DATA TERMINATOR DISABLE	X	H	L	H	X	

TRUTH TABLE - DM Operation

Name (Function)	DM	DQS	NOTES
Write Enable	L	Valid	
Write Inhibit	H	X	10

Note :
1. CKE is HIGH for all commands except SELF REFRESH.
2. BA0~BA1 select either the mode register or the extended mode register (BA0=0, BA1=0 select the mode register; BA0=1, BA1=0 select extended mode register; other combinations of BA0~BA1 are reserved). A0~A11 provide the op-code to be written to the selected mode register.
3. BA0~BA1 provide bank address and A0~A11 provide row address.
4. BA0~BA1 provide bank address; A0~A7 and A9 provide column address; A8 HIGH enables the auto precharge feature (nonpersistent) , and A8 LOW disables the auto precharge feature.
5. A8 LOW : BA0~BA1 determine which bank is precharged.
   A8 HIGH : All banks are precharged and BA0~BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; ll inputs and I/Os are "Don't Care" except for CKE.
8. DESELECT and NOP are functionally interchangeable.
9. Cannot be in powerdown or self-refresh state.
10. Used to mask write data ; provided coincident with the corresponding data.
11. Except DATA Termination disable.

DESELECT

The DESELECT function (/CS high) prevents new commands from being executed by the DDR(x32). The GDDR3(x32) SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct selected GDDR3(x32) to perform a NOP (/CS LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0-A11. See mode register descriptions in the Register Definition section. The Load Mode Register command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0,BA1 inputs selects the bank, and the address provided on inputsA0-A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on inputs A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW. the corresponding data will be written to memory; If the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one banks are to be precharged, inputs BA0,BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command will be treated as a NOP if there is no open row is already in the process of precharging.

AUTO PRECHARGE

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A8 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enable or disabled for each individual READ or WRITE command. Auto precharge ensures that the precharge is initiated at the earliest valid state within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating $t_{RAS(min)}$, as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time(t_{RP}) is completed.

AUTO REFRESH

Auto Refresh is used during normal operation of the GDDR3 SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an Auto Refresh command. The 256Mb(x32) DDR2(x32) requires Auto Refresh cycles at an average interval of 7.8us (maximum). A maximum of eight Auto Refresh commands can be posted to any given GDDR3(x32) SDRAM, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9 x 7.8us(70.2us). This maximum absolute interval is to allow GDDR3(x32) SDRAM output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR3(x32) SDRAM ,even if the rest of the system is powered down. When in the self refresh mode,the GDDR3(x32) SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. The active termination is also disabled upon entering Self Refresh and enabled upon exiting Self Refresh. (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH. The procedure for exiting self refresh requires a sequence of commands. First, CK and /CK must be stable prior to CKE going back HIGH. Once CKE is HIGH,the GDDR3(x32) must have NOP commands issued for tXSNR because tine is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 200 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

DATA TERMINATOR DISABLE (BUS SNOOPING FOR READ COMMAND)

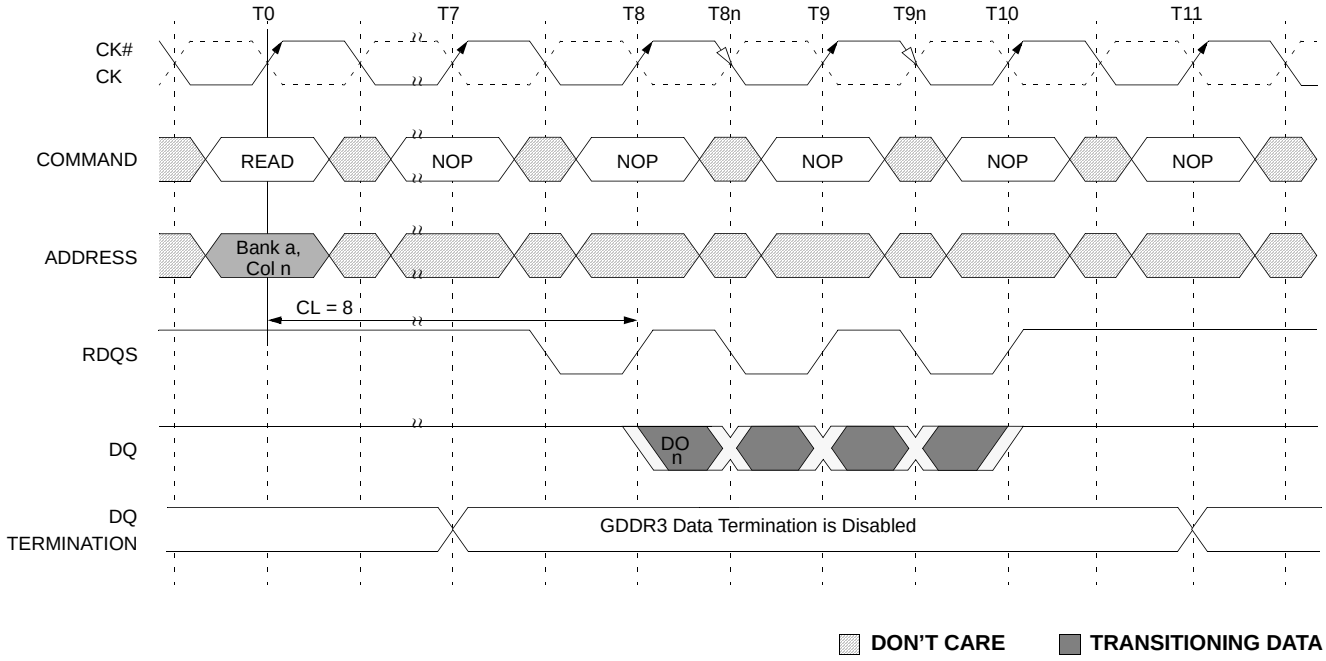
The DATA TERMINATOR DISABLE COMMAND is detected by the device by snooping the bus for READ commands excluding /CS. The GDDR3 DRAM will disable its Data terminators when a READ command is detected. The terminators are disable CL-1 Clocks after the READ command is detected. In a two rank system both dram devices will snoop the bus for READ commands to either device and both will disable their terminators if a READ command is detected. The command and address terminators and always enabled.

ON-DIE TERMINATION

Bus snooping for READ commands other than /CS is used to control the on-die termination. The GDDR3 SDRAM will disable the on-die termination when a READ command is detected, regardless of the state of /CS. The on-die termination is disabled x clocks after the READ command where x equals CL-1 and stay off for a duration of BL/2 + 2, as below figure, Data Termination Disable Timing. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on-die termination if a READ command is detected. The on-die termination for all other pins on the device are always on for both a single-rank system and a dual-rank system.

The on-die termination value on address and control pins is determined during power-up in relation to the state of CKE on the first transition of RESET. On the rising edge of RESET, if CKE is sampled LOW, then the configuration is determined to be a single-rank system. The on-die termination is then set to one-half ZQ for the address pins. On the rising edge of RESET, if CKE is sampled HIGH, then the configuration is determined to be a dual-rank system. The on-die termination for the DQs, WDQS, and DM pins is set in the EMRS.

Data Termination Disable Timing



Note : 1. DO *n* = data-out from column *n*.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the specified order following DO *n*.
4. Shown with nominal t_{AC} and t_{DQSQ}.
5. RDQS will start driving high one-half cycle prior to the first falling edge.
6. The Data Terminators are disabled starting at CL-1 and the duration is BL/2 + 2
7. READS to either rank disable both ranks' termination regardless of the logic level of /CS.

OPERATIONS

BANK/ROW ACTIVATION

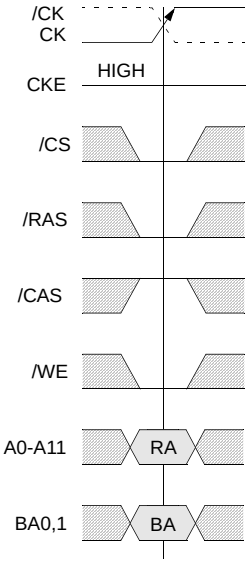
Before any READ or WRITE commands can be issued to a banks within the GDDR3 SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. $t_{RCD(min)}$ should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command in which a READ or WRITE command can be entered. For example, a t_{RCD} specification of 16ns with a 450MHz clock (2.2ns period) results in 7.2 clocks rounded to 8. This is reflected in below figure, which covers any case where $7<t_{RCD(min)}/t_{CK}\leq 8$.

The same procedure is used to convert other specification limits from tome units to clock cycles).

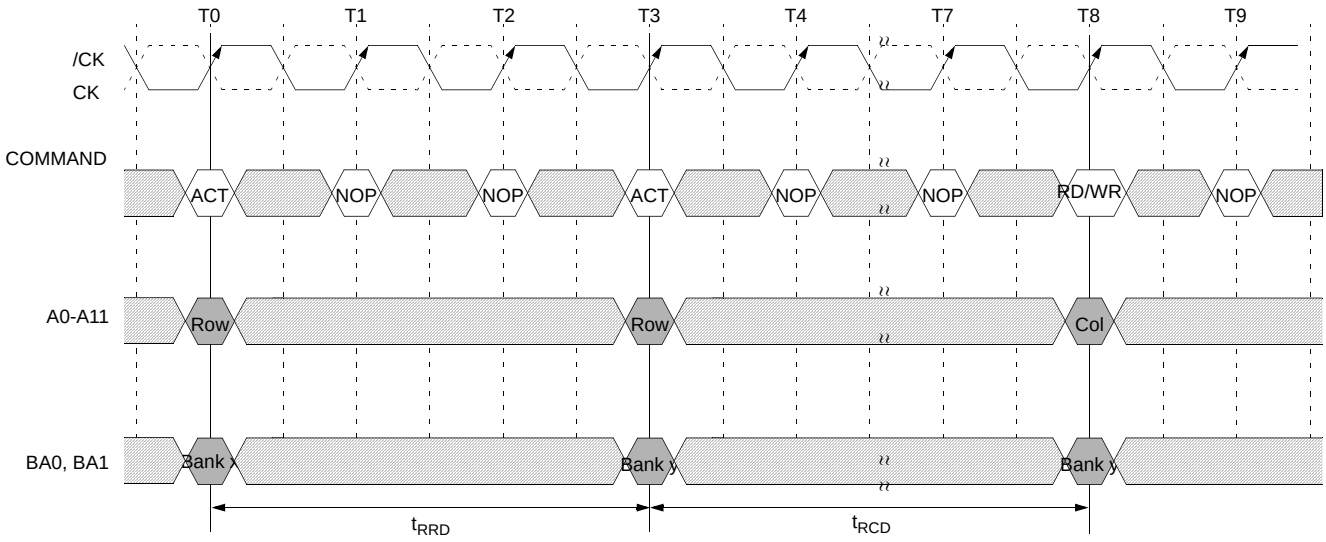
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed"(precharged). The minimum time interval between successive ACTIVE commads to the same bank is defined by t_{RC}.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.



Activating a Specific Row in a Specific Bank

Example : Meeting t_{RCD}



READs

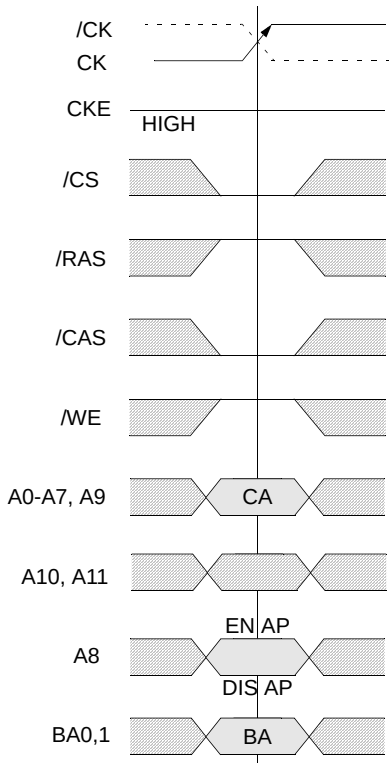
READ bursts are initiated with a READ command, as below figure. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is prechrged at the completion of the burst after $t_{RAS(min)}$ has been met. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS Latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative strobe edge. READ burst figure shows general timing for 2 of the possible CAS latency settings. The GDDR3(x32) drives the output data edge aligned to the crossing of CK and /CK and to RDQS. The initial HIGH transitioning LOW of RDQS is known as the read preamble ; the half cycle coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of t_{DQSQ} (valid data-out skew), t_{DV} (data-out window hold), the valid data window are depicted in Data Output Timing (1) figure. A detailed explanation of t_{AC} (DQS and DQ transition skew to CK) is shown in Data Output Timing (2) figure.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued x cycles after the first READ command, where x equals the number of data element nibbles (nibbles are required by the 4*n*-prefetch architecture) depending on the burst length. This is shown in consecutive READ bursts figure. Nonconsecutive read data is shown for illustration in nonconsecutive READ bursts figure. Full-speed random read accesses within a page (or pages) can be performed as shown in Random READ accesses figure. Data from a READ burst cannot be terminated or truncated.

During READ commands the GDDR3 Dram disables its data terminators.

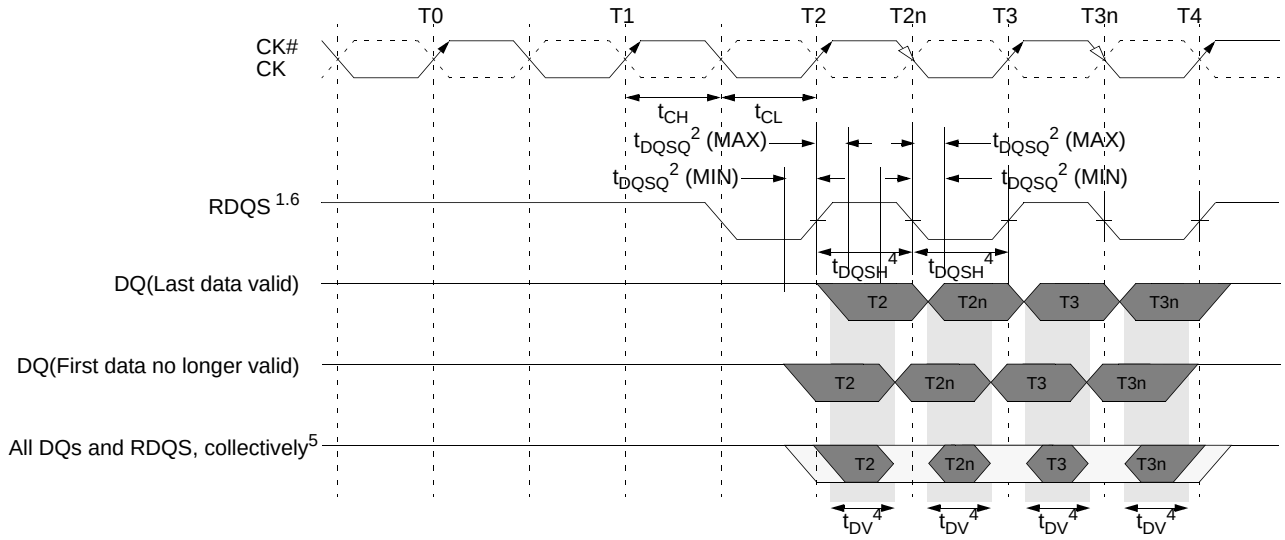


CA = Column Address
BA = Bank Address
EN AP = Enable Auto Precharge
DIS AP = Disable Auto Precharge

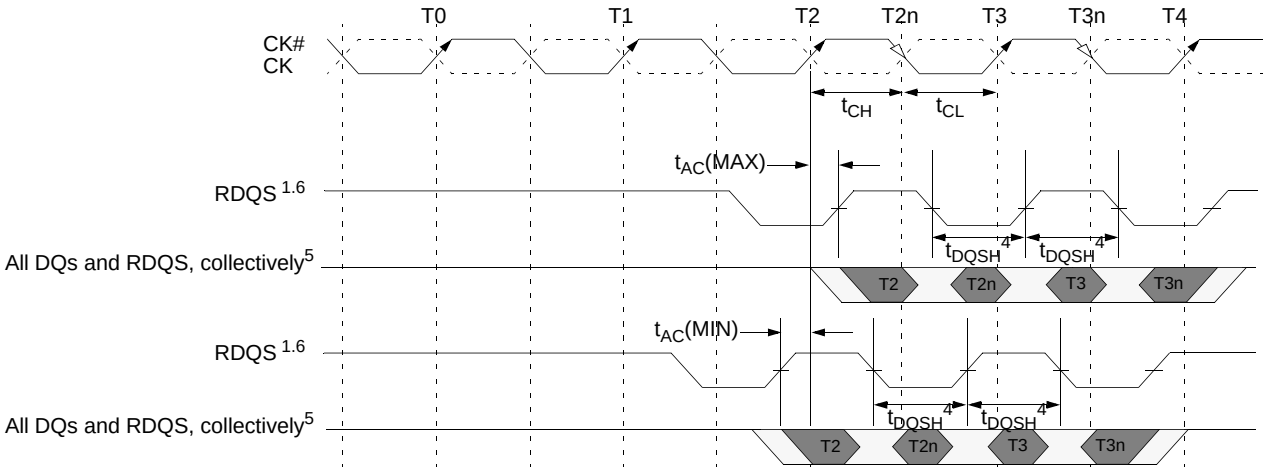
DON'T CARE

READ Command

Data Output Timing (1) - t_{DQSQ}, t_{QH} and Data Valid Window

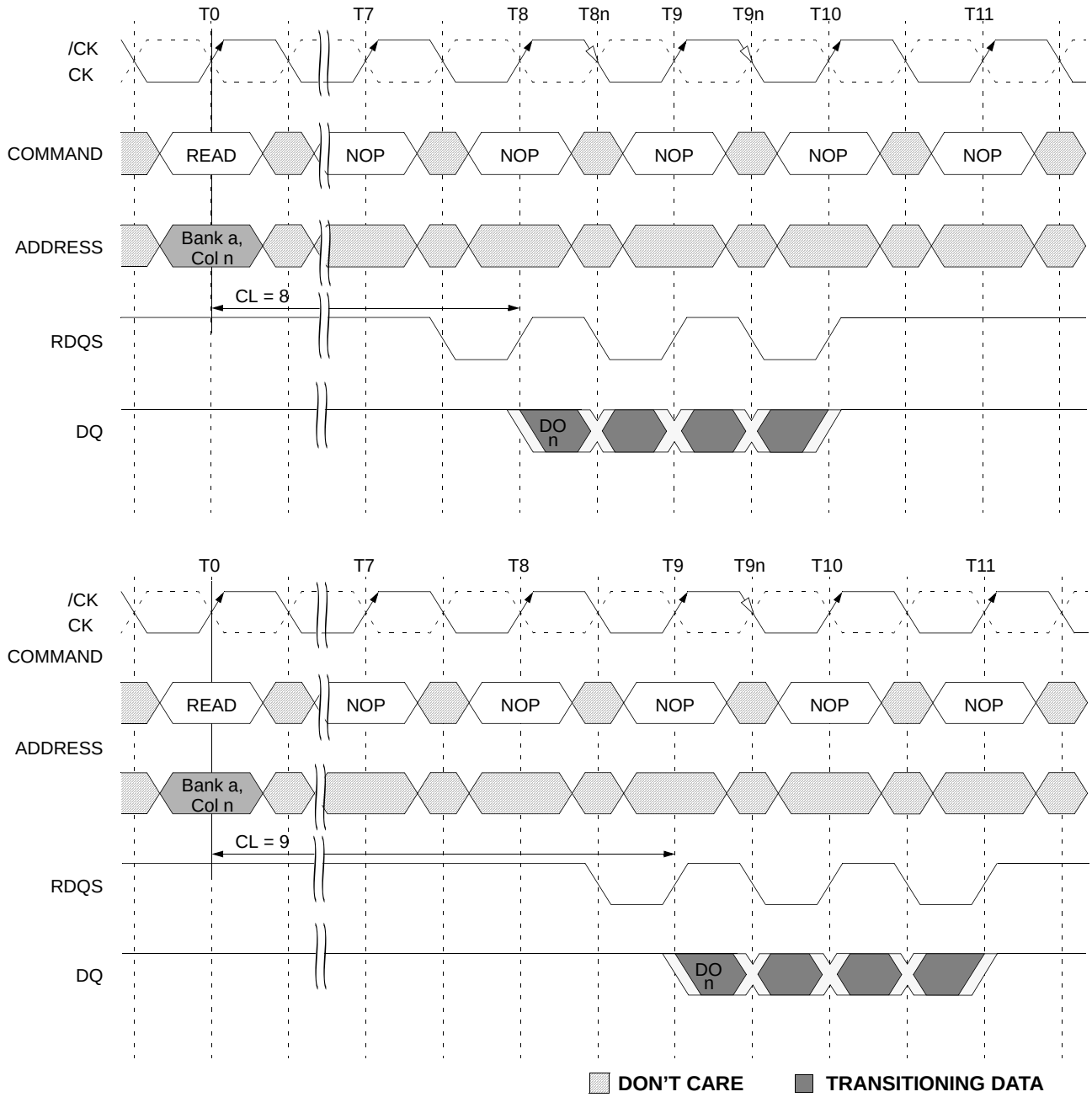


Data Output Timing (2) - t_{DQSQ}, t_{QH} and Data Valid Window



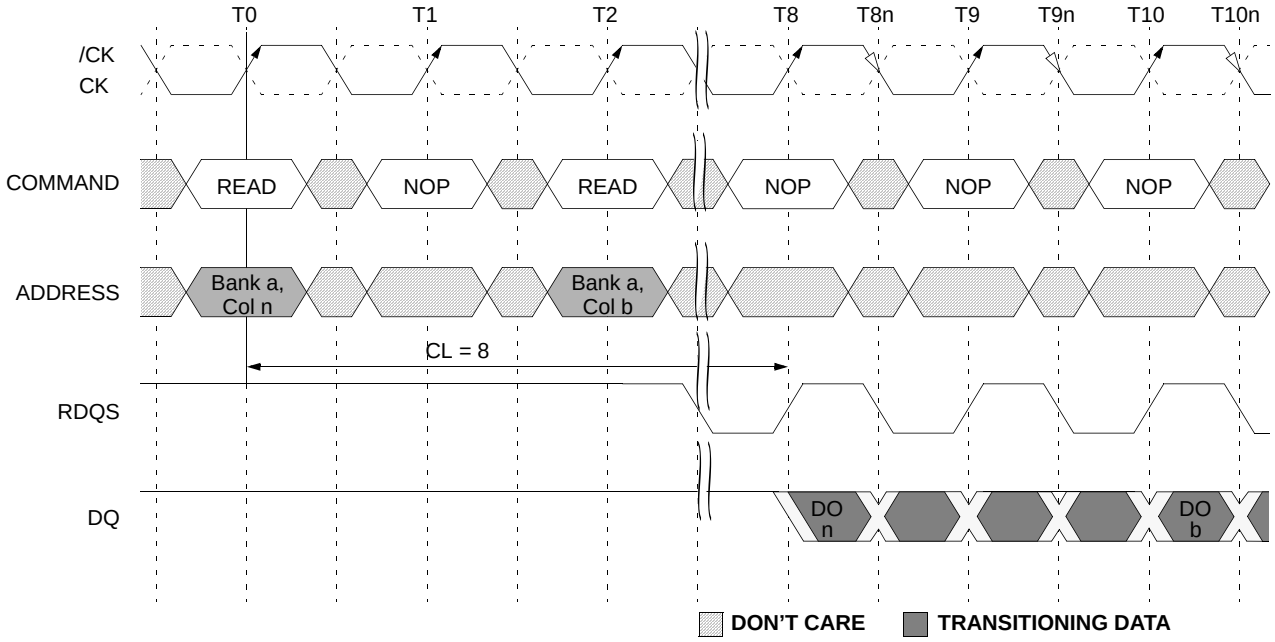
Note : 1. t_{DQSQ} represents the skew between the 8 DQ lines and the respective RDQS pin.
2. t_{DQSQ} is derived at each RDQS clock edge and is not cumulative over time and begins with first DQ transition and ends with the last valid transition of DQs.
3. t_{AC} is show in the nominal case
4. t_{DQHP} is the lesser of tDQSL or tDQSH strobe transition collectively when a bank is active.
5. The data valid window is derived for each RDQS transitions and is defined by t_{DV}.
6. There are 4 RDQS pins for this device with RDQS0 in relation to DQ0-DQ7, RDQS1 in relation DQ8-DQ15, RDQS2 in relation to DQ16-24 and RDQS3 in relation to DQ25-DQ31.
7. This diagram only represents one of the four byte lanes.
8. t_{AC} represents the relationship between DQ, RDQS to the crossing of CK and /CK.

READ Burst



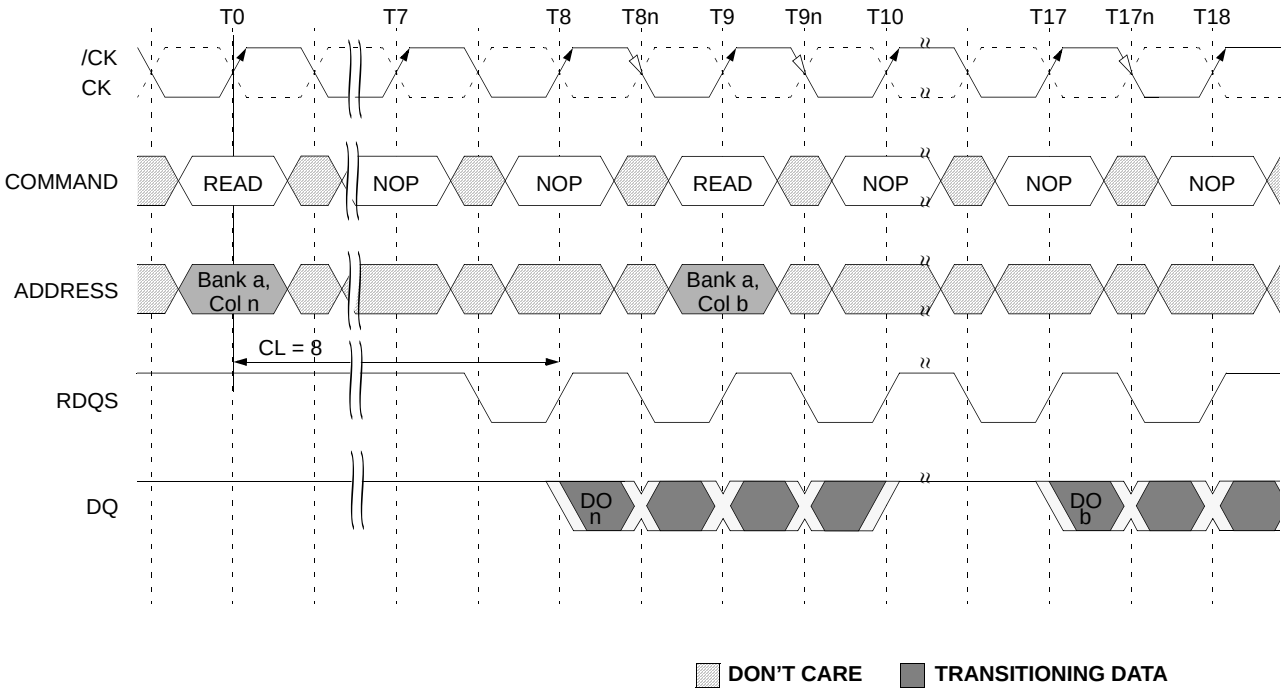
NOTE :
1. DO *n*=data-out from column *n*.
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Shown with nominal t_{AC} and t_{DQSQ}.
5. RDQS will start driving high 1/2 clock cycle prior to the first falling edge.

Consecutive READ Bursts



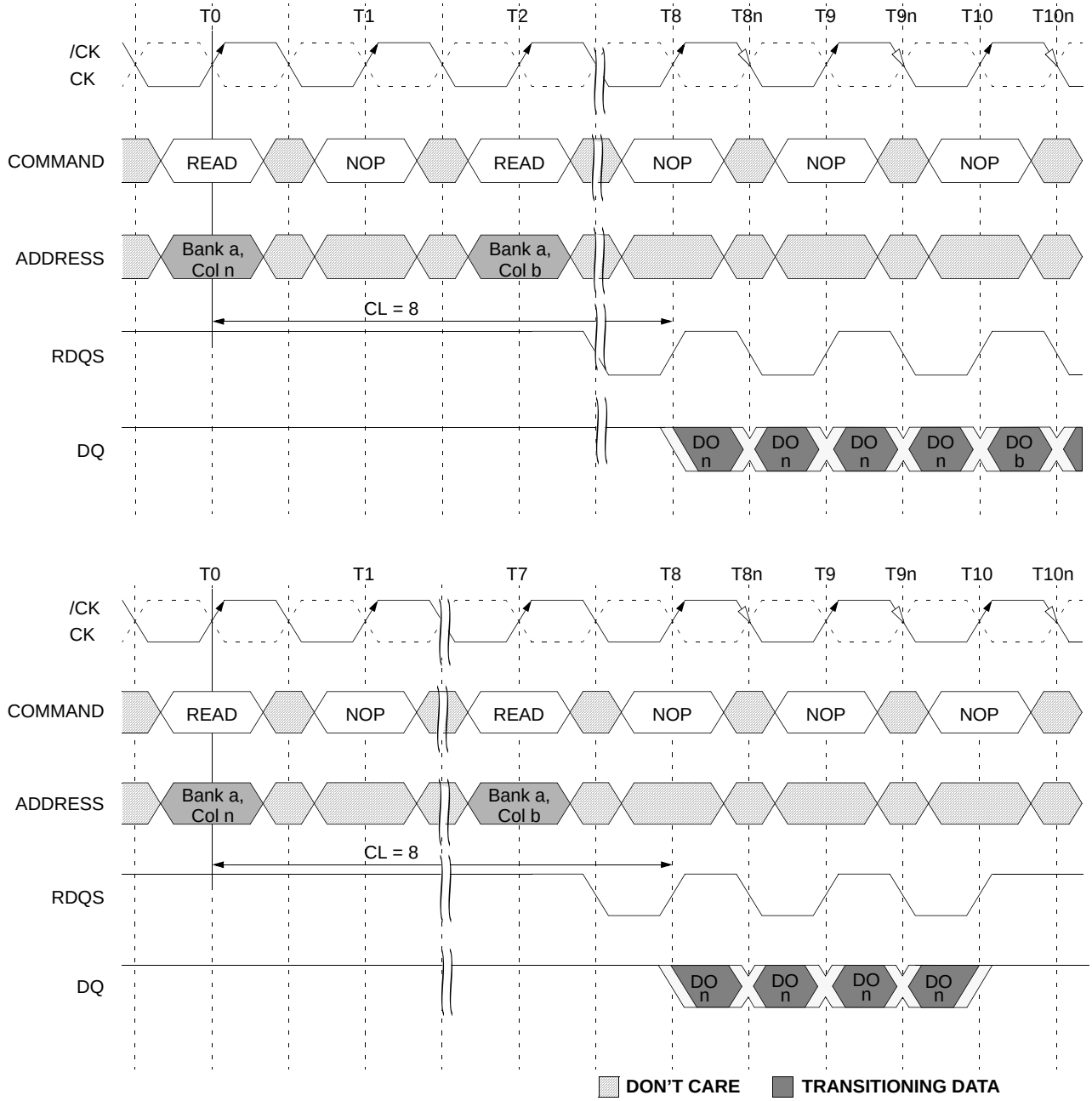
NOTE : 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Three subsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

Nonconsecutive READ Bursts



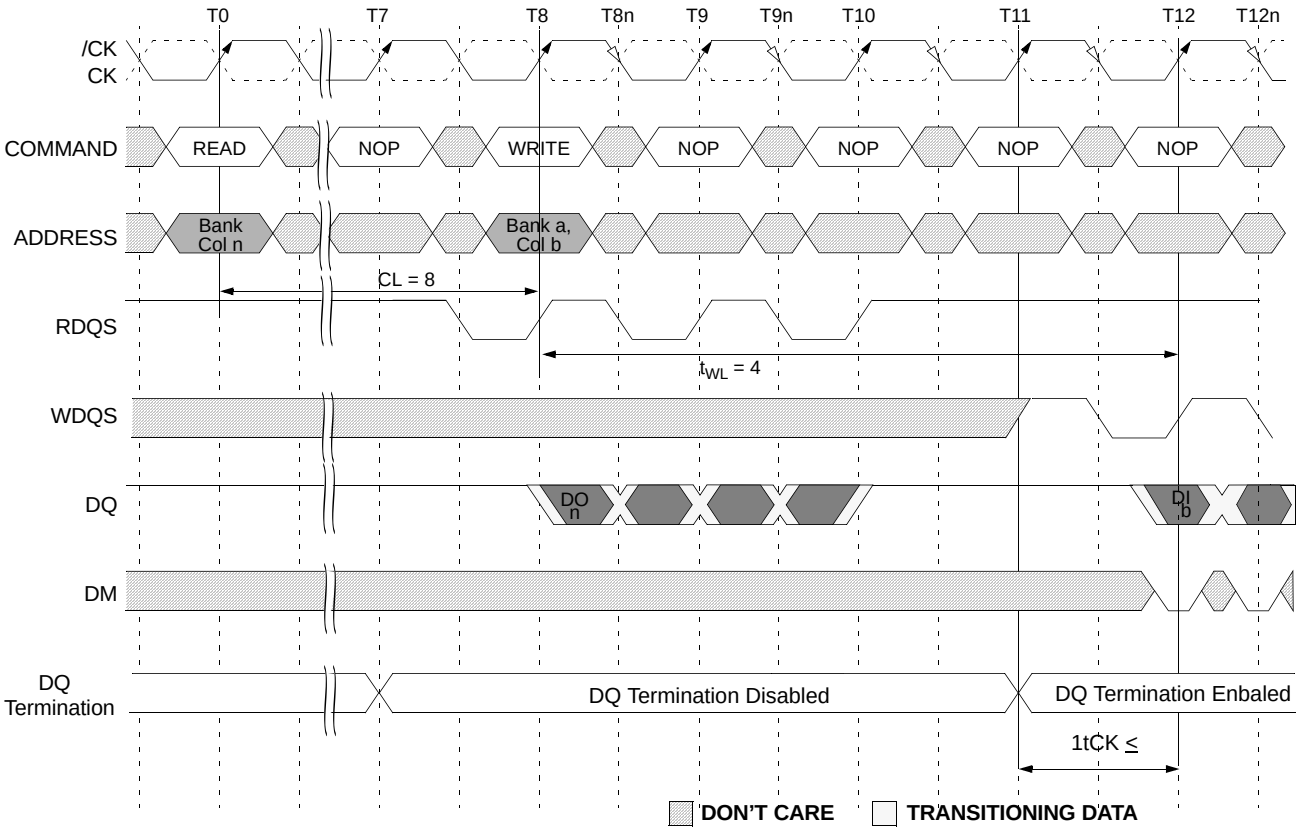
NOTE : 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Three subpsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

Random READ Accesses



NOTE :
1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *x* or column *b* or column *g*).
2. Burst length = 4
3. *n*' or x or *b*' or *g*' indicates the next data-out following DO *n* or DO *x* or DO *b* OR DO *g*, respectively
4. READs are to an active row in any bank.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

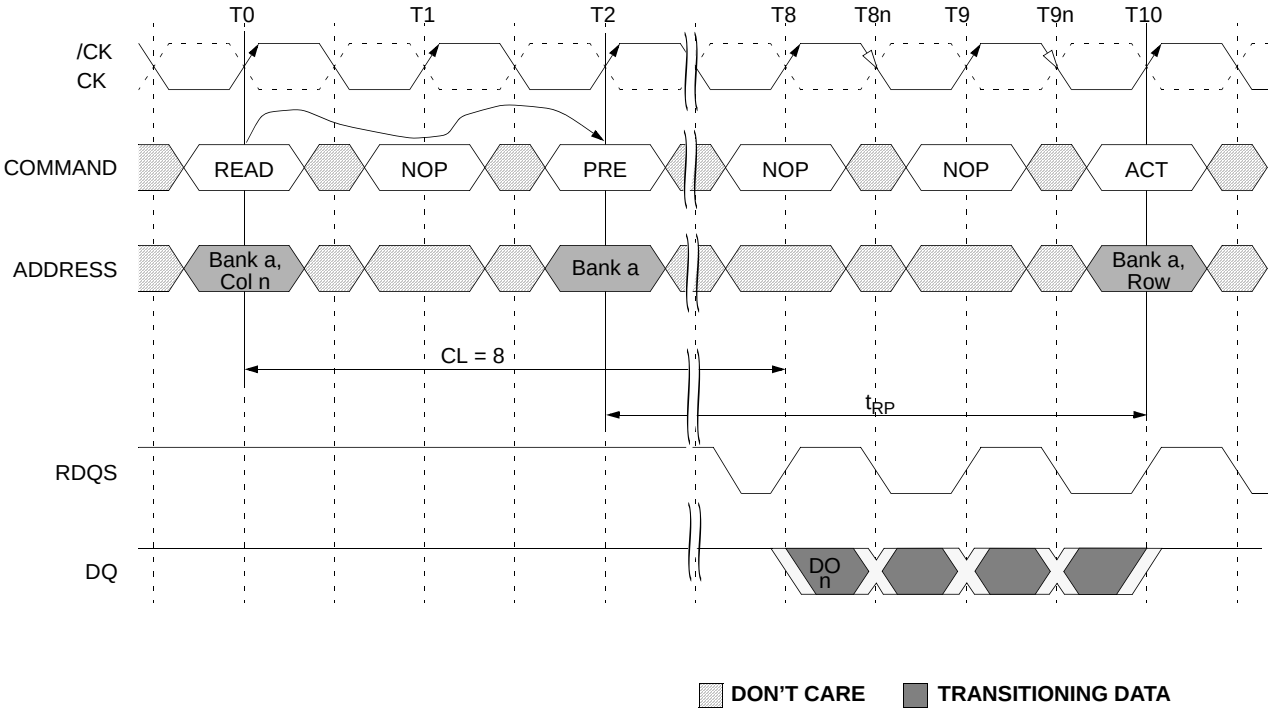
READ to WRITE



NOTE :

1. DO *n* = data-out from column *n*.
2. DI *b* = data-in from column *b*.
3. Burst length = 4
4. One subsequent element of data-out appears in the programmed order following DO *n*.
5. Data-in elements are applied following DI *b* in the programmed order.
6. Shown with nominal t_{AC} and t_{DQSQ}.
7. t_{DQSS} in nominal case.
8. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.
9. The gap between data termination enable to the first data-in should be greater than 1tCK

READ to PRECHARGE



NOTE :
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n.*
4. Read to precharge equals two clocks, which enables two data pairs of data-out.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

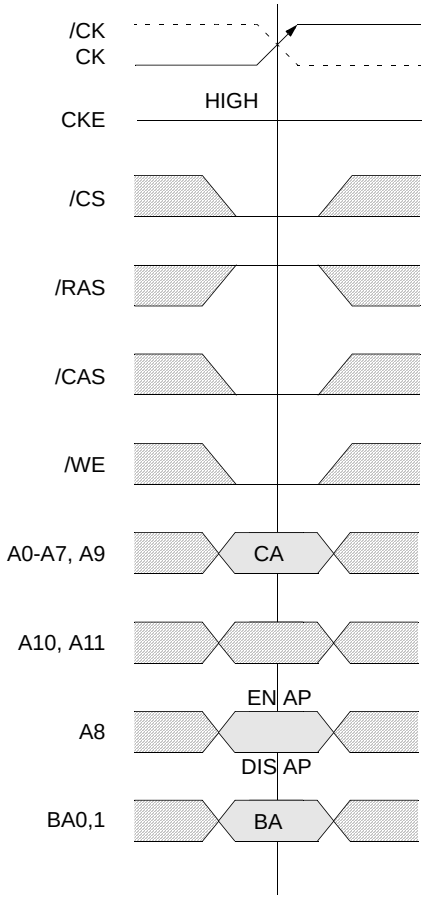
During WRITE bursts, the first valid data-in element will be registered in a rising edge of WDQS following the WRITE latency set in the mode register and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS edge a half cycle is needed and specified as the WRITE Preamble; the half cycle in WDQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first valid falling edge of WDQS (t_{DQSS}) is specified with a relative to the write latency. All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., $t_{DQSS(min)}$ and $t_{DQSS(max)}$) might not be intuitive, they have also been included. Write Burst figure shows the nominal case and the extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command after the burst has completed. The new WRITE command should be issued *x* cycles after the first WRITE command should be equals the number of desired nibbles (nibbles are required by 4n-prefetch architecture).

An example of nonconsecutive WRITEs is shown in Nonconsecutive WRITE to READ figure. Full-speed random write accesses within a page or pages can be performed as shown in Random WRITE cycles figure. Data for any WRITE burst may be followed by a subsequent READ command.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE the WRITE burst, t_{WR} should be met as shown in WRITE to PRECHARGE figure.

Data for any WRITE burst can not be truncated by a subsequent PRECHARGE command.

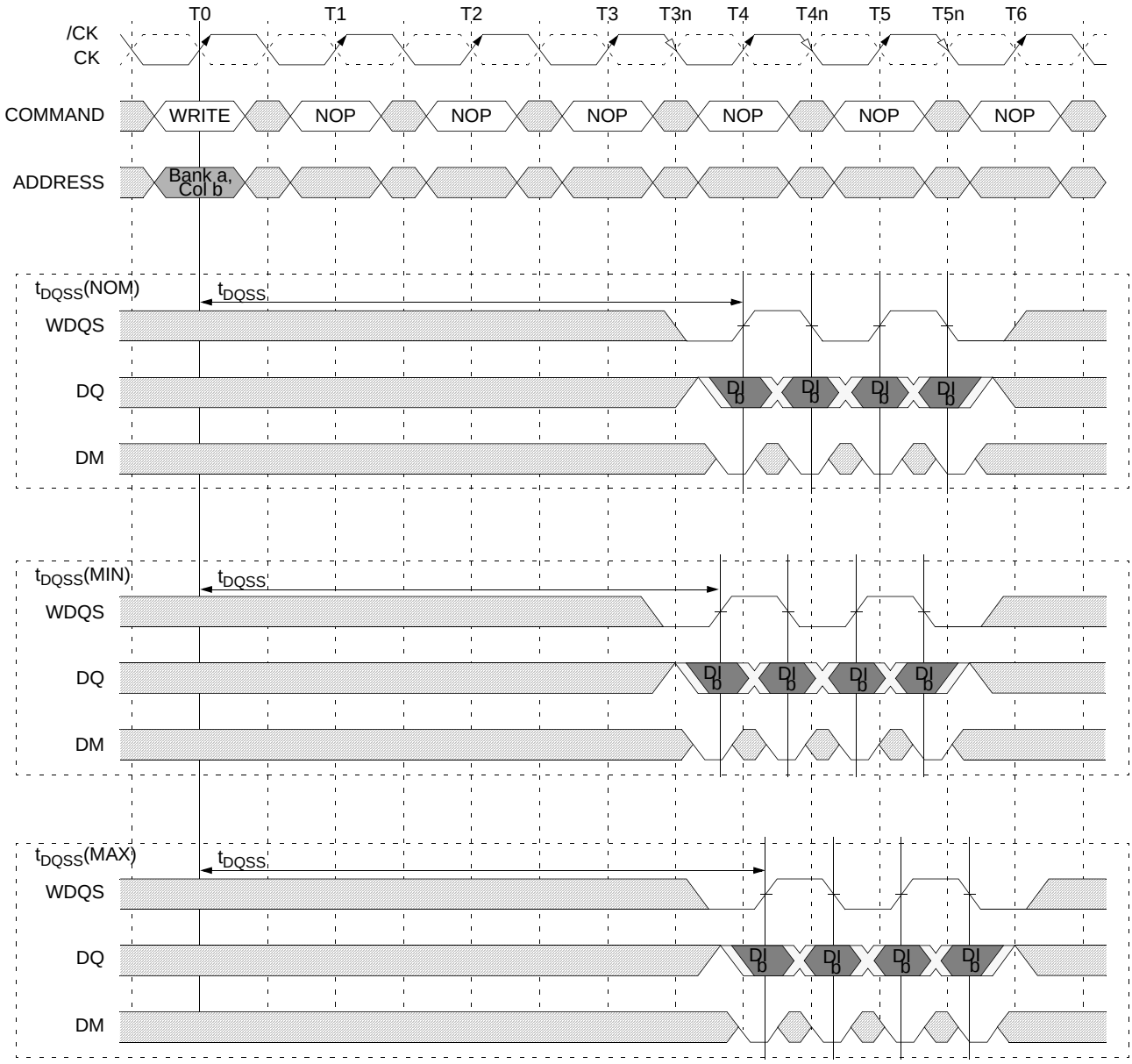


CA = Column Address
BA = Bank Address
EN AP = Enable Auto Precharge
DIS AP = Disable Auto Precharge

DON'T CARE

WRITE Command

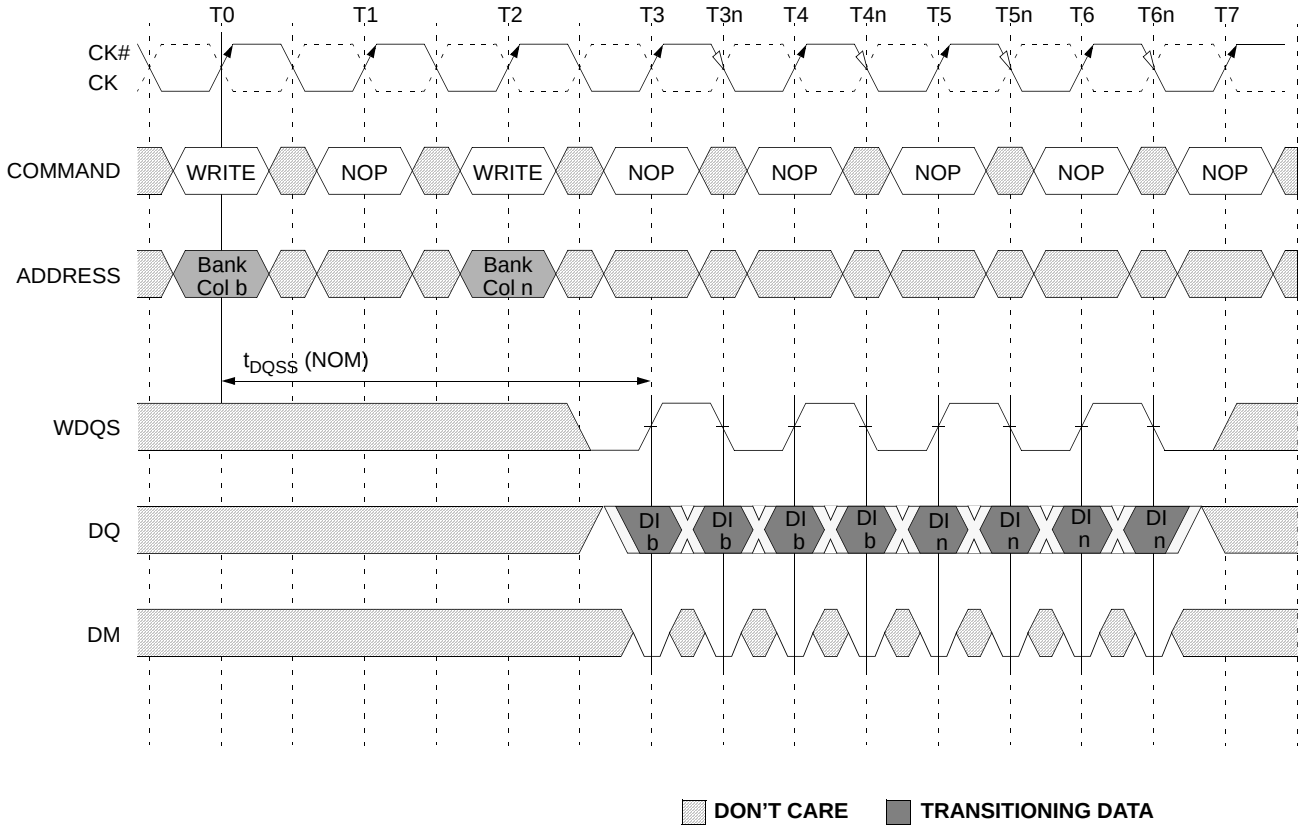
WRITE Burst



DON'T CARE TRANSITIONING DATA

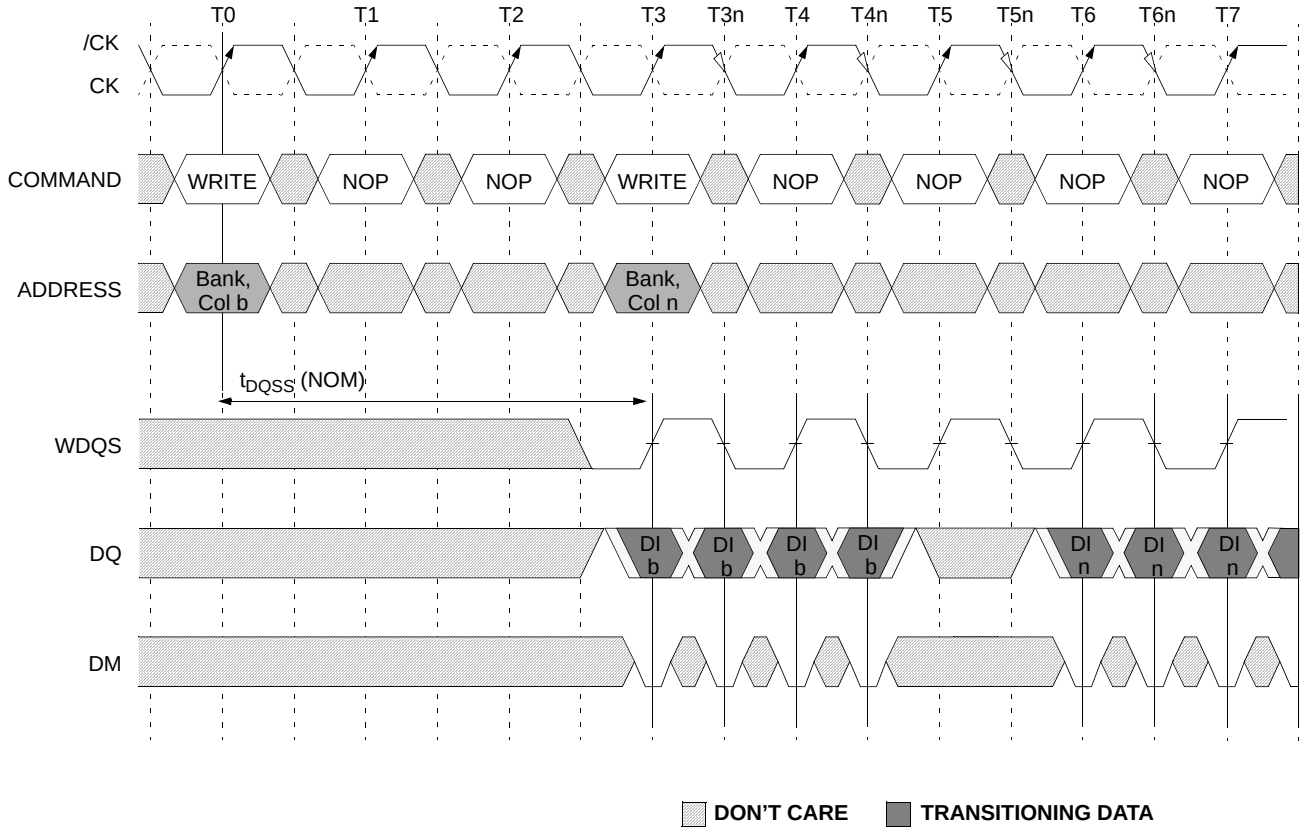
NOTE :
1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. Write latency is set to 4

Consecutive WRITE to WRITE



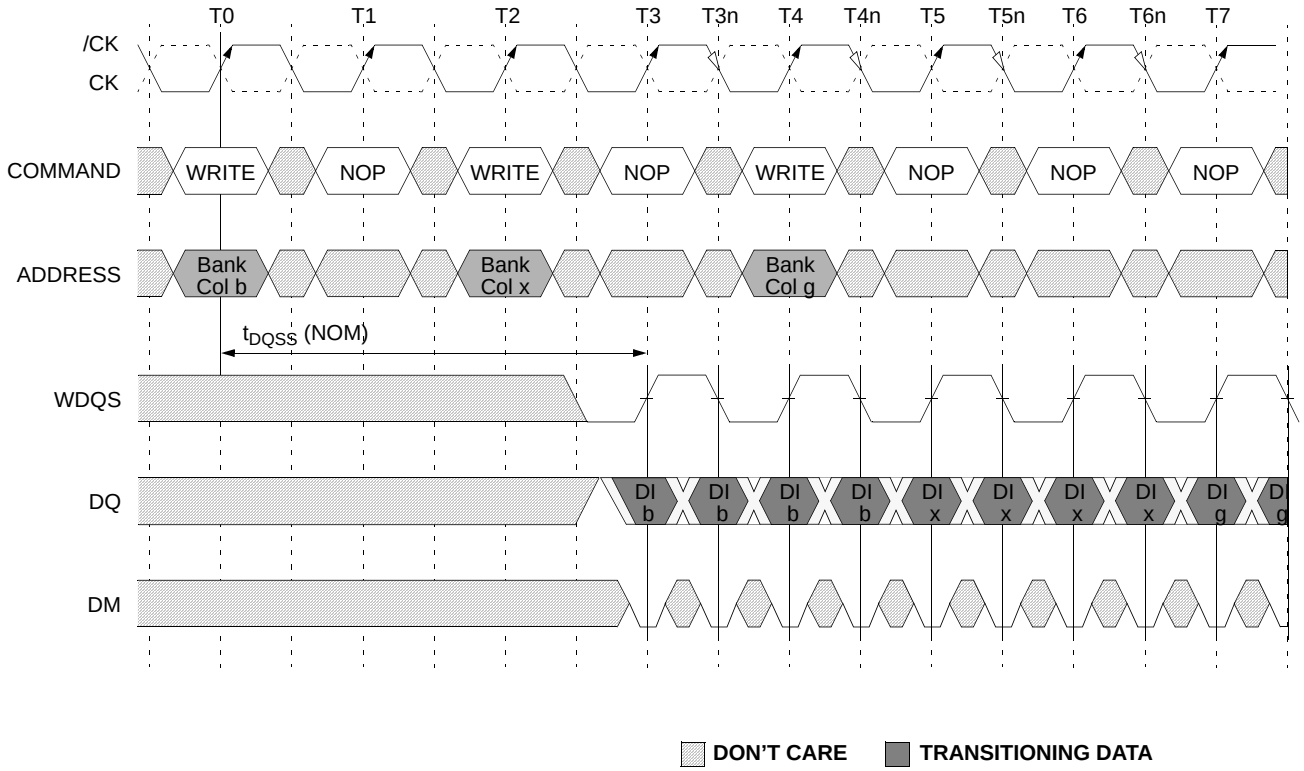
NOTE :
1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. Burst of 4 is shown.
5. Each WRITE command may be to any bank of the same device.
6. Write latency is set to 3

Nonconsecutive WRITE to WRITE



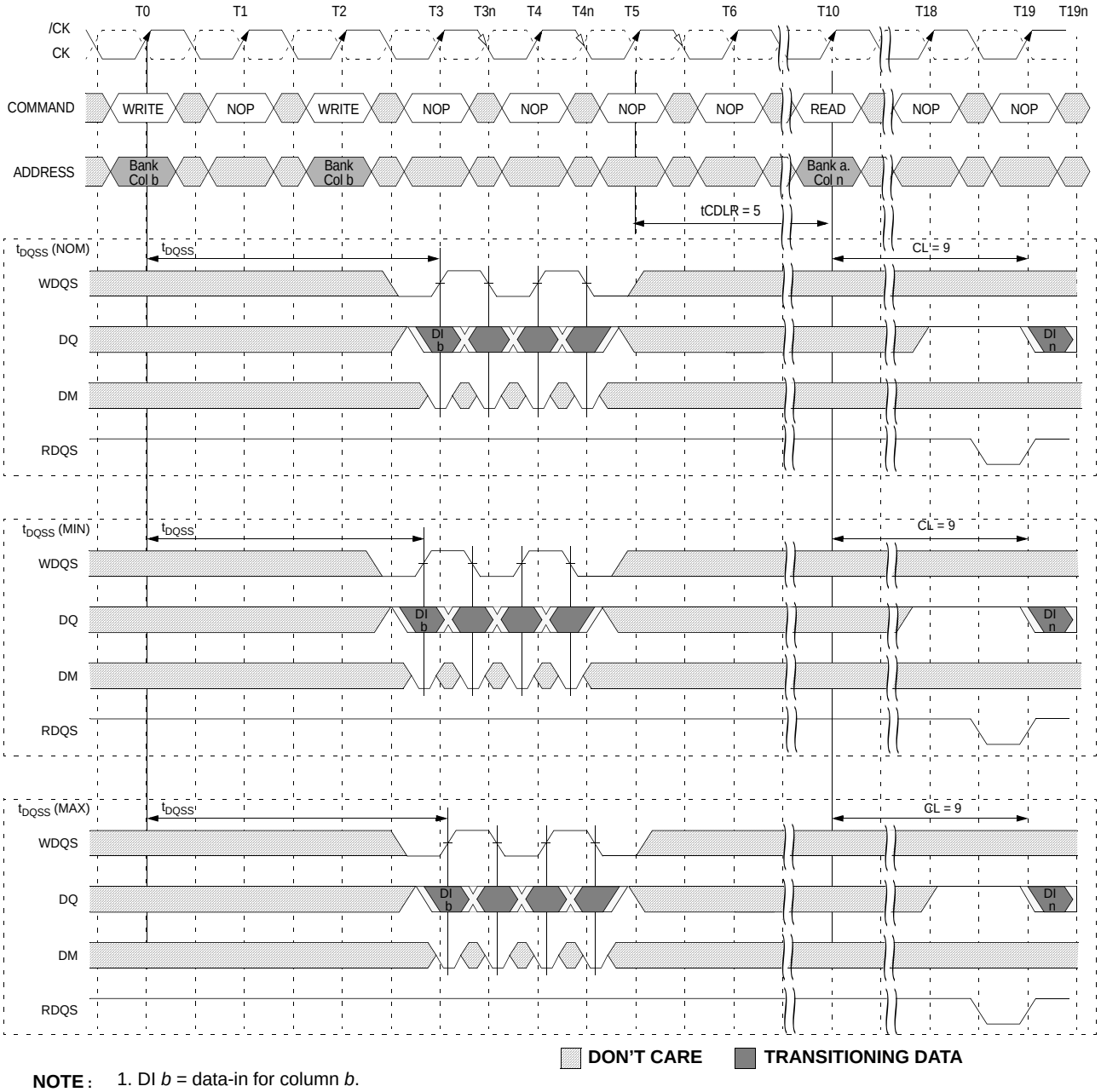
NOTE :
1. DI b, etc. = data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. burst of 4 is shown.
5. Each WRITE command may be to any bank.
6. Write latency is set to 3

Random WRITE Cycles



NOTE :
1. DI b, etc. = data-in for column b, etc.
2. b: etc. = the next data - in following DI b. etc., according to the programmed burst order.
3. Programmed burst length = 4 cases shown.
4. Each WRITE command may be to any bank.
5. Last write command will have the rest of the nibble on T8 and T8n
6. Write latency is set to 3

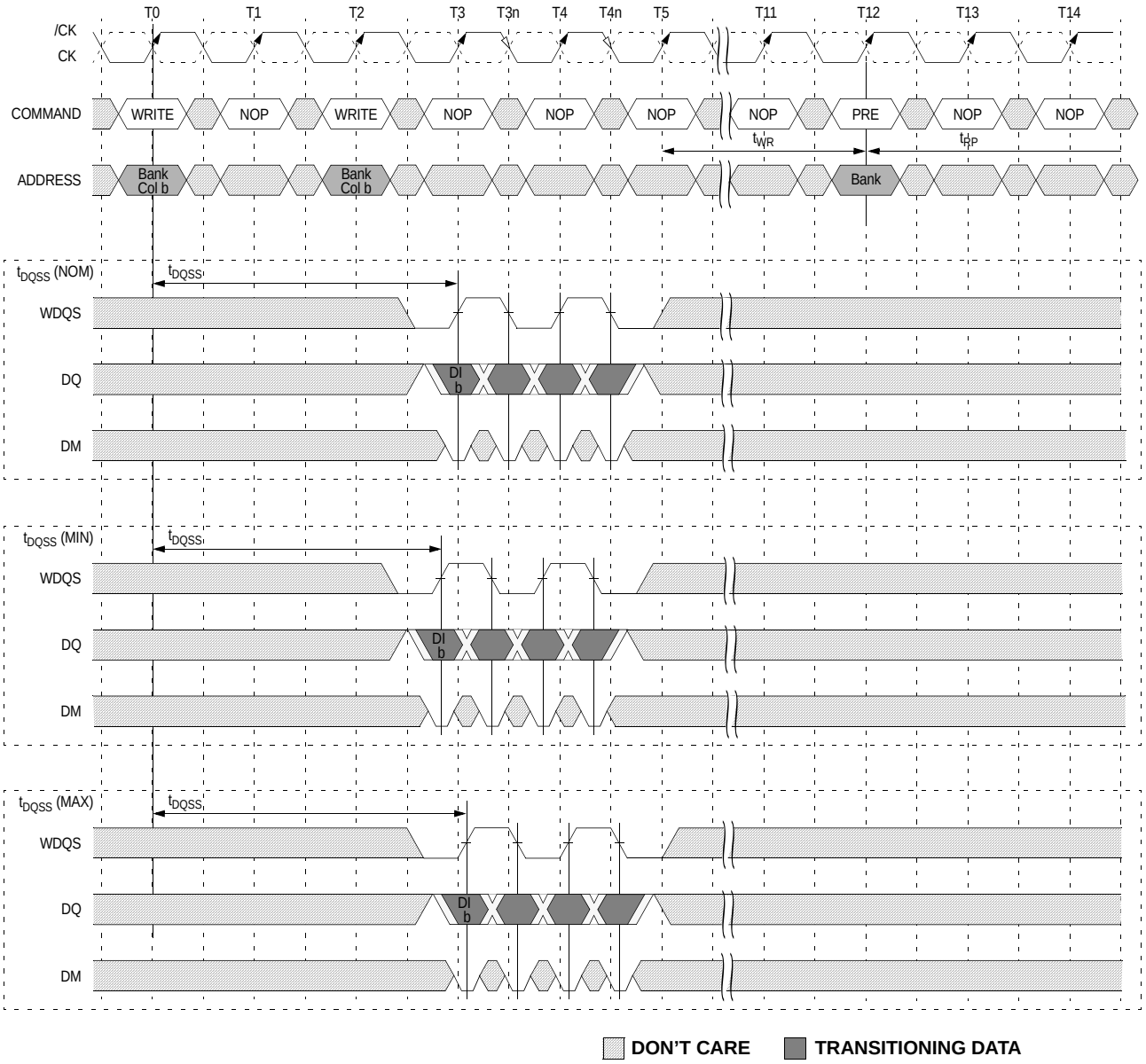
WRITE to READ



NOTE :

1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in the programmed order following DI *b.*
3. A burst of 4 is shown.
4. t_{CDLR} is referenced from the first positive CK edge after the last data-in pair.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case t_{CDLR} is not required and the READ command could be applied earlier.
6. A8 is LOW with the WRITE command (auto precharge is disabled).
7. WRITE latency is set to 3

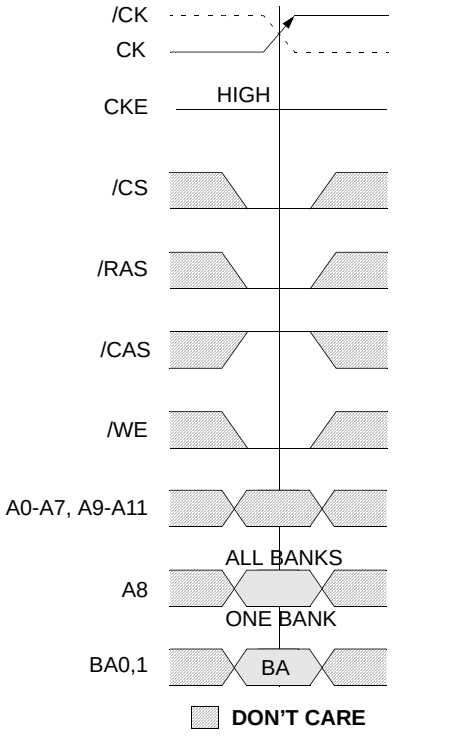
WRITE to PRECHARGE



NOTE : 1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in the programmed order following DI *b*.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. WRITE latency is set to 3

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to the bank.



BA=Bank Address
(if A8 is LOW; otherwise "Don't Care")

PRECHARGE Command

POWER-DOWN (CKE NOT ACTIVE)

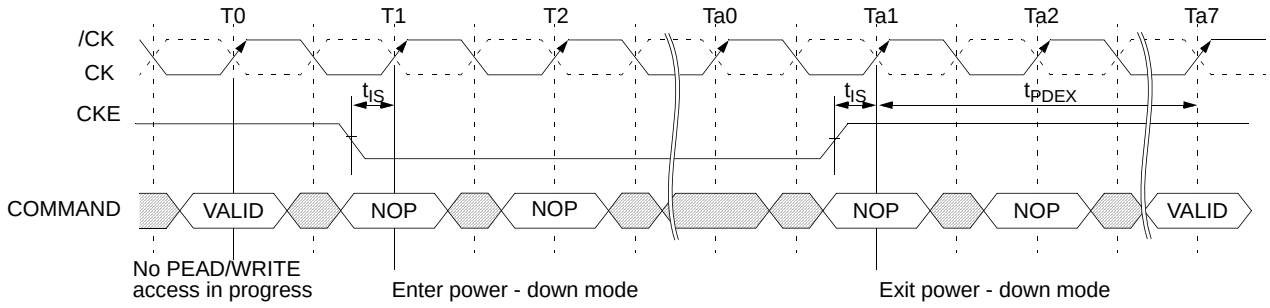
Unlike SDRAMs,GDDR3(x32) SDRAM requires CKE to be active at all times an access is in progress; from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined BL/2 cycles after the Write Postamble is satisfied.

Power-down is entered when CKE is registered LOW. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK,/CK and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. However, power-down duration is limited by the refresh requirements of the device, so in most applications,the self-refresh mode is preferred over the DLL-disabled power-down mode.

When in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the GDDR3 SDRAM, while all other input signals are "Don't Care."

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied six clock cycle later.

Power-Down



TRUTH TABLE - Clock Enable (CKE)

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	

NOTES :

1. CKEn is the logic state of CKE at clock edge *n*; CKEn-1was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2(x32) immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n*, and ACTION*n* is a result of COMMAND*n*
4. All state and sequence not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XSA} period.

TRUTH TABLE - CURRENT STATE BANK *n* - COMMAND TO BANK *n*

CURRENT STATE	/CS	/RAS	/CAS	/WE	COMMAND/ ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/ continue previous operation)	13
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATOR DISABLE	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
Row Active	L	L	L	L	LOAD MODE REGISTER	7
	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select Column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (Auto-Precharge Disable)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (Only after the READ burst is complete)	8
Write (Auto-Precharge Disabled)	L	H	L	H	READ (Select column and start READ burst)	10, 11
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Only after the WRITE burst is complete)	8, 11

NOTES :

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see CKE Truth Table) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions :

Idle : The bank has been precharged, and t_{RP} has been met.

Row Active : A row in the bank has been activated, and t_{RCD} has been met.
No data bursts/accesses and no register accesses are in progress.

Read : A READ burst has been initiated, with auto precharge disabled.

Write : A WRITE burst has been initiated, with auto precharge disabled.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and truth table- current state bank *n* - command to bank *n*. and according to truth table - current state bank *n* -command to bank *m.*

Precharging : Starts with registration of a PRECHARGE command and ends when t_{RP} is met.
Once t_{RP} is met, the bank will be in the idle state.

Row Activating : Starts with registration of an ACTIVE command and ends when t_{RCD} is met.
Once t_{RCD} is met, the bank will be in the :row active" state.

Read w/ Auto-Precharge Enabled : Starts with registration of an READ command with auto precharge enabled and ends when tRP has been met. Once t_{RP} is met, the bank will be in the idle state.

Write w/ Auto-Precharge Enabled : Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command ; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing : Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the DDR2(x32) will be in the all banks idle state.

Accessing Mode Register : Starts with registration of a LOAD MODE REGISTER command and ends when t_{MRD} has been met. Once t_{MRD} is met, the GDDR3(x32) SDRAM will be in the all banks idle state.

Precharge All : Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.

READ or WRITE : Starts with registration of the ACTIVE command and ends the last valid data nibble.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific ; If multiple banks are to be precharged, each must be in a valid state for precharging.
9. Left blank
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst.
13. Except data termination disable.

TRUTH TABLE - CURRENT STATE BANK n - COMMAND TO BANK m

CURRENT STATE	/CS	/RAS	/CAS	/WE	COMMAND/ ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/ continue previous operation)	8
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATOR DISABLE	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Prechrging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	6
	L	H	L	L	WRITE (Select Column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disable)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	6
	L	H	L	L	WRITE (Select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	6, 7
	L	H	L	L	WRITE (Select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	6
	L	H	L	L	WRITE (Select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	6
	L	H	L	L	WRITE (Select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	

NOTES :

1. This table applies when CKE*n-1* was HIGH and CKE*n* is HIGH (see TRUTH TABLE- CKE) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions :

Idle : The bank has been precharged, and t_{RP} has been met.

Row Active : A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

Read : A READ burst has been initiated, with auto precharge disabled.

Write : A WRITE burst has been initiated, with auto precharge disabled.

Read w/ Auto-Precharge Enabled : See following text

Write w/ Auto-Precharge Enabled : See following text

3a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts : the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR command and ends where the precharge period (or t_{RP}) begins.
During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related Limitations apply (e.g., contention between read data write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE w/AP	READ or READ w/AP	[WL + (BL/2)] tCK + tCDLR
	WRITE or WRITE w/AP	(BL/2) * tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK
READ w/AP	READ or READ w/AP	(BL/2) * tCK
	WRITE or WRITE w/AP	[CL_{RU} + (BL/2)] + 1 - WL * tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. All states and sequences not shown are illegal or reserved.
6. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
7. Requires appropriate DM masking.
8. Except data termination disable

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ V_{DDQ} + 0.5V	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-0.5 ~ 2.5	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-0.5 ~ 2.5	V
MAX Junction Temperature	T_J	+125	°C
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	TBD	W
Short Circuit Output Current	I_{OS}	50	mA

Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure periods may affect reliability.

POWER & DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to 0°C ≤ Tc ≤ 85°C ; VDD=2.0V ± 0.1V, VDDQ=2.0V ± 0.1V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	1.9	2.0	2.1	V	1
Output Supply voltage	V_{DDQ}	1.9	2.0	2.1	V	1
Reference voltage	V_{REF}	0.69*V_{DDQ}	-	0.71*V_{DDQ}	V	3
DC Input logic high voltage	V_{IH} (DC)	V_{REF}+0.15	-	-	V	4
DC Input logic low voltage	V_{IL} (DC)	-	-	V_{REF}-0.15	V	4
Output logic low voltage	V_{OL}(DC)	-	-	0.76	V	
AC Input logic high voltage	V_{IH}(AC)	V_{REF}+0.25	-	-	V	4,5,6
AC Input logic low voltage	V_{IL}(AC)	-	-	V_{REF}-0.25	V	4,5,6
Input leakage current Any input 0V-<V_{IN} -< V_{DDQ} (All other pins not under test = 0V)	I_I	-5	-	5	uA	
Output leakage current (DQs are disabled ; 0V-<V_{OUT} -< V_{DDQ})	I_{IOZ}	-5	-	5	uA	

Note : 1.Under all conditions, VDDQ must be less than or equal to VDD.

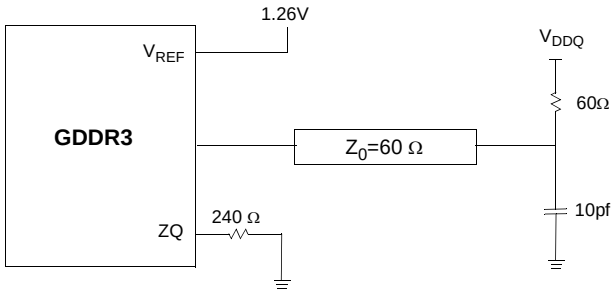
3. VREF is expected to equal 70% of VDDQ for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed ± 2 percent of the DC value. Thus, from 70% of VDDQ, VREF is allowed ± 25mV for DC error and an additional ±25mV for AC noise.
4. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge and the driver should achieve the same slew rate through the AC values.
5. Input and output slew rate =3V/ns. If the input slew rate is less than 3V/ns, input timing may be compromised. All slew rate are measured between Vih and Vil.
   DQ and DM input slew rate must not deviate from DQS by more than 10%. If the DQ,DM and DQS slew rate is less than 3V/ns, timing is longer than referenced to the mid-point but to the VIL(AC) maximum and VIH(AC) minimum points.
6. VIH overshoot : VIH(max) = VDDQ + 0.5V for a pulse width ≤ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.
   VIL undershoot : VIL(min)=0.0V for a pulse width ≤ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.

CLOCK INPUT OPERATING CONDITIONS

Recommended operating conditions (0°C ≤ Tc ≤85°C ; VDD=2.0V ± 0.1V, VDDQ=2.0V ± 0.1V)

Parameter/ Condition	Symbol	Min	Max	Unit	Note
Clock Input Mid-Point Voltage ; CK and /CK	$V_{MP(DC)}$	1.16	1.36	V	1,2,3
Clock Input Voltage Level; CK and /CK	$V_{IN(DC)}$	0.42	V_{DDQ} + 0.3	V	2
Clock Input Differential Voltage ; CK and /CK	$V_{ID(DC)}$	0.22	V_{DDQ} + 0.5	V	2,4
Clock Input Differential Voltage ; CK and /CK	$V_{ID(AC)}$	0.22	V_{DDQ} + 0.3	V	4
Clock Input Crossing Point Voltage ; CK and /CK	$V_{IX(AC)}$	V_{REF} - 0.15	V_{REF} + 0.15	V	3

Note : 1. This provides a minimum of 1.16V to a maximum of 1.36V, and is always 70% of VDDQ
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of VIX is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
4. VID is the magnitude of the difference between the input level in CK and the input level on /CK.
5. The CK and /CK input reference level (for timing referenced to CK and /CK) is the point at which CK and /CK cross; the input reference level for signals other than CK and /CK is VREF.
6. CK and /CK input slew rate must be ≥ 3V/ns



Output Load Circuit

Note : 1 . Outputs measured into equivalent load of 10pf at a driver impedance of 40 Ω.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted, 0°C ≤ Tc ≤85°C)

Parameter	Symbol	Test Condition	Version				Unit
			-14	-15	-16	-20	
Operating Current (One Bank Active)	I_{CC1}	Burst Length=4 $t_{RC} \geq t_{RC}$(min). I_{OL}=0mA, t_{CC}= t_{CC}(min). DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock cycle	505	500	495	485	mA
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	140	140	135	130	mA
Precharge Standby Current in Non Power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min),t_{CC}= t_{CC}(min) Address and control inputs changing once per clock cycle	220	215	200	185	mA
Active Standby Current power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	175	170	160	145	mA
Active Standby Current in in Non Power-down mode	I_{CC3N}	CKE ≥ VIH(min), CS ≥ VIH(min), t_{CC}= t_{CC}(min) DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock cycle	385	380	350	265	mA
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA ,t_{CC}= t_{CC}(min), Page Burst, All Banks activated. DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock.	940	935	865	750	mA
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RFC}$	440	435	420	390	mA
Self Refresh Current	I_{CC6} -GC	CKE ≤ 0.2V	20				mA
	I_{CC6} -GL		5				mA
Operating Current (4Bank interleaving)	I_{CC7}	Burst Length=4 $t_{RC} \geq t_{RC}$(min). I_{OL}=0mA, t_{CC}= t_{CC}(min). DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock cycle	1060	1055	970	950	mA

Note : 1. Measured with outputs open and ODT off
2. Refresh period is 32ms
3. Measured current at VDD & VDDQ = 2.0V

CAPACITANCE (V_{DD}=2.0V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK, $\overline{CK}$)	C_{IN1}	2.0	3.0	pF
Input capacitance (A_0~A_{11}, BA_0~BA_1)	C_{IN2}	2.0	3.0	pF
Input capacitance (CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN3}	2.0	3.0	pF
Data & DQS input/output capacitance(DQ_0~DQ_{31})	C_{OUT}	3.5	4.5	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	3.5	4.5	pF

AC CHARACTERISTICS - I

Parameter		Symbol	-14		-15		-16		-20		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
DQS out access time from CK		t_{DQSCK}	-0.26	+0.26	-0.26	+0.26	-0.29	+0.29	-0.35	+0.35	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK cycle time	CL=9	t_{CK}	1.4	3.3	1.4	3.3	-	-	-	-	ns	
	CL=8		-	-	-	-	1.6	3.3	-	-	ns	
	CL=7		-	-	-	-	-	-	2.0	3.3	ns	
WRITE Latency		t_{WL}	5	-	5	-	5	-	4	-	tCK	1
DQ and DM input hold time relative to DQS		t_{DH}	0.18	-	0.18	-	0.20	-	0.25	-	ns	
DQ and DM input setup time relative to DQS		t_{DS}	0.18	-	0.18	-	0.20	-	0.25	-	ns	
Active termination setup time		t_{ATS}	10	-	10	-	10	-	10	-	ns	
Active termination hold time		t_{ATH}	10	-	10	-	10	-	10	-	ns	
DQS input high pulse width		t_{DQSH}	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
DQS input low pulse widthl		t_{DQSL}	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
Data strobe edge to Dout edge		t_{DQSQ}	-	0.160	-	0.160	-	0.180	-	0.225	ns	
DQS read preamble		t_{RPRE}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write command to first DQS latching transition		t_{DQSS}	WL-0.2	WL+0.2	WL-0.2	WL+0.2	WL-0.2	WL+0.2	WL-0.2	WL+0.2	tCK	
DQS write preamble		t_{WPRE}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
DQS write preamble setup time		t_{WPRES}	0	-	0	-	0	-	0	-	ns	
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Half strobe period		t_{HP}	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCK	
Data output hold time from DQS		t_{QH}	t_{HP}-0.16	-	t_{HP}-0.16	-	t_{HP}-0.18	-	t_{HP}-0.225	-	ns	
Data-out high-impedance window from CK and /CK		t_{HZ}	-0.3	-	-0.3	-	-0.3	-	-0.3	-	ns	4
Data-out low-impedance window from CK and /CK		t_{LZ}	-0.3	-	-0.3	-	-0.3	-	-0.3	-	ns	4
Address and control input hold time		t_{IH}	0.35	-	0.35	-	0.4	-	0.5	-	ns	
Address and control input setup time		t_{IS}	0.35	-	0.35	-	0.4	-	0.5	-	ns	
Address and control input pulse width		t_{IPW}	1.0	-	1.0	-	1.1	-	1.3	-	ns	

Note : 1. The WRITE latency can be set from 1 to 7 clocks. When the WRITE latency is set to 1 or 2 or 3 clocks(this case can be used regardless of fre quency), the input buffers are turned on during the ACTIVE commands reducing the latency but added power. When the WRITE latency is set to 4 ~7 clocks , the input buffers are turned on during the WRITE commands for lower power operation. The WRITE latency which is over 4 clocks can be used only in case that Write Latency*tCK is greater than 7ns.

2. A low to high transition on the WDQS line is not allowed in the half clock prior to the write preamble.

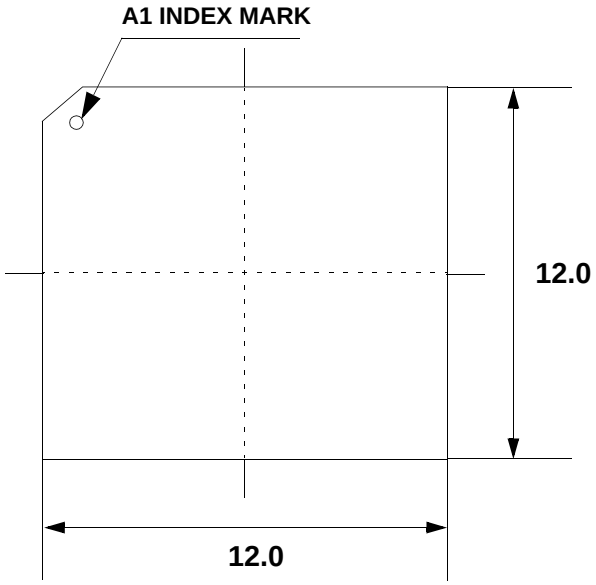
3. The last rising edge of WDQS after the write postamble must be riven high by the controller. WDQS can not be pulled high by the on-die termination alone.

4. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

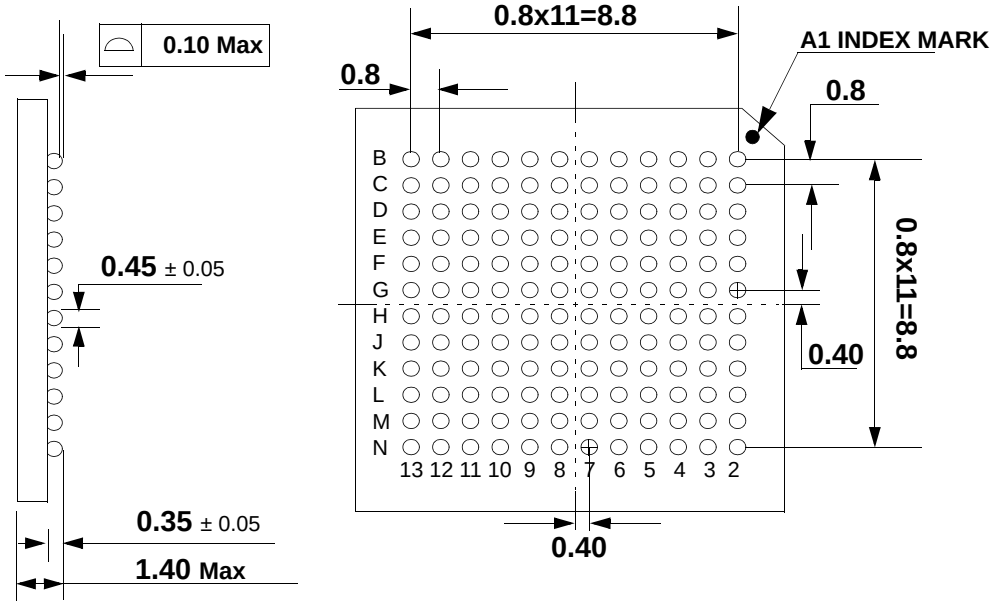
AC CHARACTERISTICS - II

Parameter	Symbol	-14		-15		-16		-20		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Row active time	t_{RAS}	22	100K	22	100K	19	100K	15	100K	tCK	
Row cycle time	t_{RC}	31	-	31	-	27	-	21	-	tCK	
Refresh row cycle time	t_{RFC}	39	-	39	-	33	-	27	-	tCK	
RAS to CAS delay for Read	t_{RCDR}	10	-	10	-	9	-	7	-	tCK	
RAS to CAS delay for Write	t_{RCDW}	6	-	6	-	5	-	4	-	tCK	
Row precharge time	t_{RP}	9	-	9	-	8	-	6	-	tCK	
Row active to Row active	t_{RRD}	8	-	8	-	7	-	5	-	tCK	
Last data in to Row precharge @ Normal pre-charge	t_{WR}	9	-	9	-	8	-	7	-	tCK	
Last data in to Row precharge @ Auto precharge	t_{WR_A}	7		7		7		7		tCK	
Last data in to Read command	t_{CDLR}	5	-	5	-	4	-	3	-	tCK	
Mode register set cycle time	t_{MRD}	6	-	6	-	5	-	4	-	tCK	
Auto precharge write recovery time + Precharge	t_{DAL}	18	-	18	-	16	-	13	-	tCK	
Exit self refresh to Read command	t_{XSR}	20000	-	20000	-	20000	-	20000	-	tCK	
Power-down exit time	t_{PDEX}	6tCK +tIS	-	6tCK +tIS	-	6tCK +tIS	-	4tCK +tIS	-	tCK	
Refresh interval time	t_{REF}	-	7.8	-	7.8	-	7.8	-	7.8	us	

PACKAGE DIMENSIONS (FBGA)



<Top View>



<Bottom View>

Unit : mm